SEPTEMBER 2025

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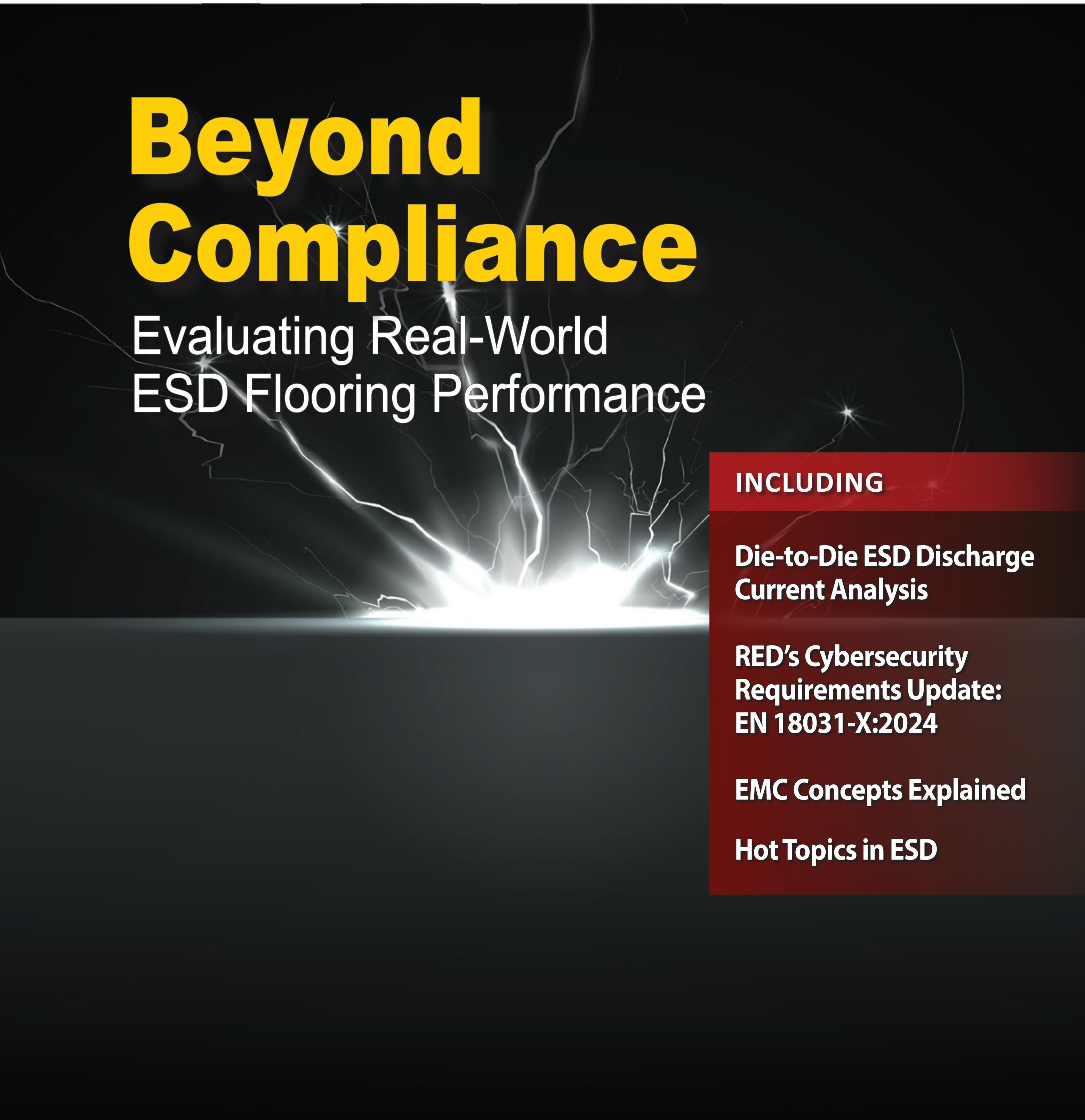

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## The EERC™

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white paper

### Fundamentals of Electrical Safety Testing

This white paper explores the evolution and critical role of advanced hipot testers in ensuring product safety. It details how modern testers perform dielectric withstand, insulation resistance, and ground bond tests, complying with global standards like IEC and UL. The paper emphasizes the necessity of reliable, accurate testing in manufacturing and certification processes.

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guide

### VSWR Explained

This resource traces VSWR from telegraph linemen using light bulbs to detect transmission line faults to modern RF measurements. It explains how improper line termination creates reflected signals that combine with forward waves, forming standing wave patterns. The evolution demonstrates how VSWR became a standard parameter for measuring reflected power in RF systems.

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white paper

### How To Work Safely With High-Voltage Test & Measurement Equipment

When working with high-voltage test and measurement equipment, electrical and test engineers strive to achieve precise readings while also maintaining a safe work area. They employ external probes such as high-voltage dividers, but these instruments have drawbacks and are prone to errors. This white paper describes an alternative approach to high voltage calibration.

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# SEPTEMBER 2025

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## FEATURE ARTICLES



## SPECIAL COVERAGE



## COLUMN



## DEPARTMENTS

## FCC Takes More Actions Under Its "Delete, Delete, Delete" Initiative

The U.S. Federal Communications Commission (FCC) is continuing efforts to streamline its regulations under its "Delete, Delete, Delete" initiative.

In the latest round, the Commission voted to remove 11 outdated and "useless" rule provisions from its regulations. The FCC says that this round of changes covers 39 "regulatory burdens," 7194 words, and 16 pages.

Specifically, the changes repeal restrictions on phone booth enclosures and captioning on analog TV receivers, as well as auction provisions that reportedly expired 20 years ago and references to telegraph rules that were repealed decades earlier.

The FCC's actions under its "Delete, Delete, Delete" initiative are based on a Proceeding it issued in March of this year (see GN Docket No. 25-133), under which the Commission intends to eliminate what it believes to be unnecessary or overly burdensome rules.

## FDA Launches Regulatory Accelerator for Digital Health Devices

The U.S. Food and Drug Administration (FDA) has announced a new initiative to support the more efficient development of digital health devices.

Managed by the Center for Devices and Radiological Health (CDRH), the FDA's Regulatory Accelerator initiative offers developers of digital health and software-based medical devices access to several new online resources. These resources include:

- A "Resource Index" that features a visual guide to currently available tools, guidances, and engagement opportunities (e.g., webinars) designed to support innovators through every stage of device development, including the regulatory review and approval process;
- "Orientation Meetings" that provide developers with an overview and additional information on the submission process for FDA market approval; and
- A "Medical Device Software Guidance Navigator" that identifies specific FDA guidances applicable to particular digital health device and their alignment with the agency's electronic Submission Template and Resource (eSTAR).

The FDA says that the intention behind its Regulatory Accelerator initiative is to help developers of innovative digital health devices learn more about FDA requirements and the FDA review process. The goal is to help foster a more efficient review of FDA submissions, allowing developers to bring innovative digital devices to market more quickly.

## EU Commission Takes Steps to Ensure National Transposition of EU Directives

The Commission of the European Union (EU) is taking legal action to ensure that EU Member States transpose EU directives into national laws.

According to a recent article posted on the Commission's website, formal notices have been sent to a number of Member States that have failed to transpose any of six specific EU directives into national law by the required dates. In some cases, the Commission has also opened infringement proceedings against some Member States that have failed to communicate with the Commission about their transposition efforts.

Of particular note is the Commission's actions in connection with its Directive (EU) 2023/2413 intended to accelerate the deployment of renewable energy in all sectors of the economy, including building environments and the transportation industry. EU Member States were required to complete the transposition of the provisions of the directive into national law by the end of May of this year. However, 26 Member States have failed to notify the Commission of the status of their transposition efforts.

In response, the Commission has sent letters of formal notice to each of the 26 Member States, giving them two months to complete their transposition of the Directive and to notify the Commission of their actions. Failure to act could result in further legal action by the Commission.

## Parties to Pay $100 Million for Fraud Related to Lifeline Program

A Florida-based telecommunications carrier and its owner have agreed to pay more than $100 million to settle criminal charges and civil allegations in connection with their participation in a program that provided discounted phone services to qualified consumers.

The company, Q Link Wireless of Dania Beach, Florida, and its owner Issa Asad will pay $110,637,057 in connection with its participation in the Lifeline Program, an FCC initiative intended to provide low-income consumers with discounted rates for their telecommunications services.

Specifically, Q Link and Asad reportedly submitted fraudulent payment claims under the Lifeline Program for customers who failed to use their cellphones consistent with the Program's minimum usage requirements (at least once every 30 days), receiving more than $38 million in payments from Lifeline.

As part of its settlement with the FCC, Q Link and Asad pled guilty to charges that they conspired to commit wire fraud and theft of government funds.

Further, according to the FCC, the parties provided "false and fabricated" records to support their fraudulent claims of customers' phone use and the payments due to them.

As part of its settlement with the FCC, Q Link and Asad pled guilty to charges that they conspired to commit wire fraud and theft of government funds. The parties also pleaded guilty to money laundering. Finally, Q Link and Asad agreed to cooperate with the FCC in transitioning its Lifeline customers to other Lifeline telecommunications service providers and not to participate in any program administered by the FCC.

MILITARY AND AEROSPACE EMC

# High Intensity Radiated Fields Part 2

By Patrick André

In Part 1, we discussed some of the sources of and the historical basis for HIRF testing. With the increased use of "Fly by wire" controls of aircraft, the high intensity of radio frequency transmitters caused interference with these controls, at times with very serious effects. Test levels had to be increased, and methodology changed for components and subsystems, as well as complete systems and the full aircraft. RTCA's DO-160B, which was in effect until 1989, had as its highest radiated susceptibility level 'Category Z,' which was 1 V/m from 35 MHz to 1215 MHz, with a bump to 2 V/m from 118-136 MHz. The lowest level in DO-160C (December 1989) would be 5 V/m, with a new maximum of 200 V/m up to 18 GHz.[1]

In 1988, the SAE "was requested to develop guidance for designers' aircraft, aircraft engine, and electronics components on how to maximize protection of airborne avionics and electronic systems from the adverse effects of high energy RF fields through which aircraft may fly."[2] The SAE would create three groups, or Panels, to address the subject. Panel 1 would validate the HIRF environment. Panel 2 would support the FAA by writing the high-level advisory material for their rule making effort. Panel 3 would write the recommended practices to meet the environments they would identify. This work was focused on environments found in the Continental U.S. and its territories. A similar effort was underway in Europe through EUROCAE with Working Group 33, members of which participated in SAE's AE4R HIRF Subcommittee. To assure uniformity and completeness, the Electromagnetic Effects Harmonization Working Group, or EEHWG, would assemble the data and information generated by the groups involved.

It was found that the environment for rotorcraft (helicopters) was different than that of commercial or private fixed wing aircraft. Helicopters are cleared for lower flight and closer approach to transmitters than fixed wing aircraft. Helicopters also have a more open

flight deck than most aluminum skin aircraft. Thus, the resulting fields experienced had the potential to be higher. Other considerations were addressed for fixed wing aircraft as well. The result was the generation of four HIRF environments:

- Fixed Wing Aircraft Severe HIRF (not used in FAA HIRF guidance AC 20-158B)
- HIRF Environment I - Aircraft Certification
- HIRF Environment II - Aircraft Normal
- HIRF Environment III - Rotorcraft Severe HIRF

The predicted levels of HIRF had to be validated. To support this, the FAA conducted some flights in their S-76 helicopter. This 1993 work resulted in a three-volume report entitled “FAA Technical Center Final Report DOT/FAA/CT-93/5-I, S-76 High Intensity Radiated Fields”. This helped to establish and validate the rotorcraft environment. NASA would fly a 757 near several transmitters and measured fields in the flight deck and electrical equipment bays. The NASA data was compared to computer models. Earlier studies were performed by Ohio University Avionics Engineering Center under contract with the FAA. In 1988, a DC-3 with RF field measuring equipment flew near four sites:[3]

- 100 kHz: Loran-C, Carolina Beach, North Carolina.
- 15.195 and 11.939 MHz: Voice of America, HF Broadcast, Greenville, North Carolina.
- 21.5 MHz: Over-the-Horizon Radar (OTH-B), Moscow, Maine.
- 3 GHz: TPS-75 Radar, Baltimore, Maryland.

Many other sources were considered, especially any significant transmitter within a five-mile radius of the airport or landing craft. These included airport-based transmitters (VOR, Glide Slope, several radars, communications and telemetry, marker beacons, and the like). Also included were all other transmitters, such as television, radio, public and private licensed transmitters, radars, communication systems - both terrestrial and space, and any other emitters of various types. The largest U.S. airports with the most significant emitters were studied first, focusing on emitters over 100 Watts.

Some transmitters were continuous wave (CW) or amplitude or frequency modulated (AM or FM). Others, such as radars and some communication systems, were pulse modulated with different amplitude signatures. As a result, peak field levels and average field levels were defined. These levels may not have been from the same transmitter since peak fields from a pulse modulated source with a very low duty cycle may have a very low average field strength compared to other sources.

In the next article, the field levels.

## ENDNOTES

1. It should be noted that the power requirements from 2 V/m to 200 V/m increased by 10,000 times, power increases as the square of the voltage. Almost overnight, test labs required radical changes in the equipment needed to perform these tests.
2. Fred Heather, High intensity radiated field external environments for civil aircraft operating in the United States of America, Report No.: NAWCADPAX--98-156-TM, (Naval Air Warfare Center, Aircraft Division, 1988), 3.
3. Ibid, 5.

PRACTICAL ENGINEERING

# Odds and Ends: Navigating the Nuances of Compliance Engineering

By Don MacArthur

Compliance engineering is a field that demands meticulous attention to detail, a proactive mindset, and a deep understanding of regulatory landscapes. In this practical engineering article, we explore some of the lesser-discussed aspects of compliance engineering—those "odds and ends" that can make a significant difference in ensuring products meet stringent standards and regulations.

## THE IMPORTANCE OF MATERIAL SELECTION

One often overlooked aspect of compliance engineering is the selection of materials. The choice of materials can significantly impact the safety and compliance of a product. For instance, the material group of components affects the required creepage distances in safety-certified products. Ensuring that the materials used are appropriate for the intended application and meet regulatory requirements is crucial. This involves not only selecting materials that can withstand the operational environment but also those that comply with specific industry standards.

## DOCUMENTATION: THE BACKBONE OF COMPLIANCE

Accurate and comprehensive documentation is the backbone of compliance engineering. This includes maintaining detailed records of test reports, compliance certificates, and technical files. Well-organized documentation is essential for audits and regulatory submissions. It provides a clear trail of evidence that a product meets all necessary standards. Engineers should prioritize documentation from the early stages of product development to avoid last-minute scrambles and potential non-compliance issues.

## PROACTIVE ENGAGEMENT WITH DEVELOPMENT TEAMS

Engaging with product development teams from the initial design stages is a proactive approach that can prevent costly rework and delays later. By providing guidance and recommendations upfront, compliance engineers can help ensure that products are designed with compliance in mind. This collaborative approach fosters a culture of compliance within the organization and helps identify potential issues early in the development process.

## CONTINUOUS LEARNING AND ADAPTABILITY

The regulatory landscape is constantly evolving, with new standards and regulations being introduced regularly. Compliance engineers must stay current with industry standards, regulations, and technological advancements. Continuous learning through workshops, conferences, and training sessions is essential. Additionally, engineers must be adaptable and ready to adjust to changes in regulations and market demands. Embracing change as an opportunity to learn and innovate is key to thriving in the field of compliance engineering.

## ETHICAL CONDUCT AND INTEGRITY

Maintaining the highest standards of integrity and professionalism is non-negotiable in compliance engineering. Compliance decisions should be based on objective evidence and not influenced by external pressures or biases. Ethical conduct ensures that products are safe and reliable, and it builds trust with regulatory bodies and customers. Engineers should always prioritize safety and compliance over shortcuts or cost-saving measures that could compromise product integrity.

## EFFECTIVE COMMUNICATION

Effective communication is vital in compliance engineering. Engineers must be able to convey complex technical information to both technical and non-technical stakeholders. This includes collaborating with cross-functional teams to ensure compliance requirements are understood and

Compliance engineering is a multifaceted field that requires a blend of technical expertise, ethical conduct, and effective communication. By focusing on the "odds and ends"–the often overlooked but critical aspects of compliance–engineers can ensure that products meet regulatory standards and are safe for consumers.

met. Clear and concise communication helps bridge the gap between different departments and ensures everyone is aligned with compliance goals.

## PROBLEM-SOLVING MINDSET

Compliance engineering often involves navigating complex challenges and finding practical solutions that align with regulatory requirements. A problem-solving mindset is essential for developing strategies to mitigate risks and ensure compliance. Engineers should approach challenges with creativity and a solution-oriented attitude, looking for ways to achieve compliance without compromising product quality or functionality.

## BUILDING A PROFESSIONAL NETWORK

Building a strong professional network is beneficial for compliance engineers. Engaging with industry experts, regulatory bodies, and other compliance professionals provides knowledge-sharing and mentorship opportunities. A robust network can offer support and insights, helping engineers stay informed about industry trends and best practices. Participating in professional organizations and attending industry events can also enhance an engineer's knowledge and career prospects.

## CONTINUOUS IMPROVEMENT

Embracing a mindset of continuous improvement is crucial for compliance engineering. Regularly reviewing and assessing compliance processes helps identify areas for optimization. Implementing enhancements to streamline workflows and boost efficiency can lead to better compliance outcomes. Engineers should be open to feedback and continuously seek ways to improve their practices and processes.

## CONCLUSION

Compliance engineering is a multifaceted field that requires a blend of technical expertise, ethical conduct, and effective communication. By focusing on the "odds and ends"—the often overlooked but critical aspects of compliance—engineers can ensure that products meet regulatory standards and are safe for consumers. Continuous learning, proactive engagement, and a commitment to integrity and excellence are the cornerstones of a successful compliance engineering career.

In summary, the nuances of compliance engineering are what set good products apart from great ones. By paying attention to these details, engineers can navigate the complexities of regulatory requirements and contribute to the development of safe, reliable, and compliant products.

STANDARDS PRACTICE

# Tailoring Guidance

By Karen Burnham

Some requirements are set in stone. But many of them need to be tailored for your specific hardware. If you apply standards blindly, you'll run into all kinds of schedule-delaying problems: test methods and setups that don't make sense, test failures that aren't important and need to be waived, and missing problems that will pop up later during integration and checkout. Some standards, such as MIL-STD-464 and MIL-STD-461, are explicit that they must be tailored. When a standard needs to be so general that it can cover everything from a walkie-talkie to an aircraft carrier, you need to make sure that you're applying it in a way that makes sense for-your hardware.

So, when you're sitting down to tailor your program requirements down to a specific set of hardware to be tested, where should you start? Here are some suggestions.

1. The document itself. It's worth the time to sit down and read, in detail, as much of the original text as possible. It may have a table showing which requirements apply to different applications (such as Table V of MIL-STD-461 Rev G). There may be notes or footnotes that mention exceptions or specific configuration types to include or avoid.
2. The appendices of the document. As I've said many times in many venues, it's always worth the time to read informative as well as normative appendices and annexes. They often have context and guidance that

can help you work out how a specific standard applies to your project.

3. Parent documents. Sometimes, you're looking at a document derived from another source. For instance, in the automotive sector, you might be looking at an OEM spec that has been lightly modified from ECE Reg 10, CISPR 25, or ISO 11452. Tracing a requirement back to a parent and seeing how (and with luck, understanding why) it has been modified can give you valuable insight. The parent document may also have additional context or rationale to help you understand the "why" behind the requirement's purpose, allowing you to apply it most effectively.
4. Other documents tackling similar projects. There are some standards out there that are already-tailored versions of their parents. Seeing how (and why) they did their tailoring can be invaluable. Here are a few examples:
    a. GSFC-STD-7000 is a version of MIL-STD-461 specifically tailored to small science satellites. Its "app notes" section (functioning as an appendix) has a wealth of information about exactly why they made the modifications they did. I found their commentary on LISN selection particularly enlightening, among others.
    b. AIAA-S-121, SMC-S-008, and SMC-T-008 are tailored versions of MIL-STD-464 for space systems. (Just a note, that's MIL-STD-464 covering the broad range of electromagnetic environmental effects requirements, not just EMC.) I recommend particularly looking at SMC-S-008. It has technically been superseded by SMC-T-008, but the S version is much easier to read. In addition, the SMC documents are freely available, while the S-121 document must be purchased from AIAA.
    c. MIL-STD-461 CS118 and JLR-EMC-CS CI 280 are lightly tailored versions of IEC 61000-4-2.

Being a die-hard standards geek, tailoring requirements is one of my favorite things to do professionally. It may not be everyone's idea of beach reading, but I've learned that every time I've put in the effort to read a standard or its appendices closely, I've found useful nuggets that help make my testing more efficient and effective.

## WHERE SHOULD YOU START?

1. **The document itself.** It's worth the time to sit down and read, in detail, as much of the original text as possible.
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# BEYOND COMPLIANCE: EVALUATING REAL-WORLD ESD FLOORING PERFORMANCE

## When Confidence Masquerades as Competence

Dave is the CEO and founder of Staticworx, Inc., a U.S. leader in static control flooring. Backed by 30 years of work in electrostatics and concrete substrate diagnostics, he turns lab-grade science into field-proven solutions for mission-critical spaces—ranging from semiconductor test labs to 911 call centers. Dave's blend of deep technical fluency and hands-on problem-solving helps clients achieve compliance and long-term risk mitigation. He can be reached at dave@staticworx.com.

By David Long

The Dunning–Kruger effect[1] explains how overestimating one's technical reach can narrow ESD evaluations to the decades-old floor resistance-to-ground (Rtg) test—an essential metric since the 1950s, yet blind to system interactions. Three case studies show that skipping resistance tests of mobile technical elements (casters, chairs, carts) that depend on the floor as a series path to ground leads to false confidence and missed risks.

This article advocates pilot floor installations plus insitu body voltage, probability analysis of charge generation data, and mobileelement resistance tests to validate system-level performance and secure long-term staticrisk mitigation.

## WHEN THE ELEMENTS PASS, BUT THE SYSTEM FAILS

In a recent discussion with a cleanroom design team, we encountered a scenario that, while surprisingly common, illustrates a significant gap in understanding.

Their client was offered the chance to conduct an in-house pilot evaluation comparing conductive and dissipative ESD flooring options. However, she declined, reasoning that another division had already selected an appropriate product. She considered her evaluation complete after reviewing supplier literature and performing standard resistance-to-ground and flooring/footwear resistance tests according to ANSI/ESD STM7.1 and STM97.1.

Notably absent from her evaluation were body voltage measurements required by ANSI/ESD S20.20 and evaluations specified in ANSI/ESD TR53, including seating (Section 7.3.10.1), shelving (Section 7.3.12.1), and mobile workstations (Section 7.3.13.1). These steps are critical for validating the flooring's effectiveness as the primary grounding path for chairs, shelving units, and mobile workstations, and for comprehensively assessing the system's real-world performance. Nevertheless, she considered compliance adequately verified and viewed the matter as resolved.

This scenario exemplifies the Dunning–Kruger effect, a cognitive bias wherein individuals with limited expertise significantly overestimate their own understanding. This effect has contributed to numerous well-documented technical and financial failures, including the 2007–2008 Subprime Mortgage Crisis, the Theranos Scandal, the 1986 Challenger Disaster, and fatal programming errors in the mid-1980s associated with the Therac-25 radiation machine. In each instance, misplaced confidence and incomplete assumptions overshadowed expert analysis, leading to serious, avoidable outcomes.

In the specialized field of static control, such overconfidence poses easily avoided risks. Historically, the role of an ESD coordinator or engineer was a dedicated, full-time position within electronics manufacturing. Today, however, many organizations have integrated these responsibilities into broader quality functions, reducing ESD management to routine compliance checks rather than treating it as a rigorous, proactive discipline. This shift is reflected in declining attendance at critical events like the annual ESD Symposium, despite rising ESD sensitivities in components and increasing associated liabilities.

Commonly, individuals mistake basic achievements, such as completing ANSI/ESD TR53 training or quarterly resistance measurements, as sufficient evidence of expertise in static control. Yet static electricity is a silent threat, causing degradation and damage to sensitive electronics without obvious immediate indicators. As our reliance grows on microelectronics, used to operate aircraft, weapons systems, medical imaging devices, autonomous vehicles, and sophisticated AI technologies, organizations must move beyond superficial testing and incomplete knowledge to effectively manage ESD risks.

Until recently, advancements in microelectronics closely followed the prediction of Intel co-founder Gordon Moore, who forecast that transistor density would approximately double every two years. Despite these significant technological advancements, many organizations continue to rely on outdated practices, insufficient training, and institutional overconfidence in their static control programs. Given the transformative potential of artificial intelligence and autonomous technologies, organizations cannot afford simplistic approaches to adequately protect the sophisticated electronics upon which these innovations depend.

Today, ESD flooring is broadly adopted in diverse mission-critical environments far beyond traditional electronics and aerospace sectors, including SCIFs, data centers, MRI suites, air traffic control towers, operational control rooms, and emergency dispatch facilities. Given this widespread adoption, one might reasonably assume technical specifications for ESD flooring have grown more rigorous. However, the opposite often occurs.

Many professionals responsible for specifying ESD flooring still lack clarity on fundamental distinctions between conductive, dissipative, and antistatic classifications. For instance, during a recent meeting at a multinational architectural firm, a senior industry leader mistakenly stated that his project did not require ESD-grade flooring, proposing that a "dissipative" solution would suffice. This individual was unaware that dissipative flooring is, in fact, a specific subset within the broader category of ESD flooring. Such misconceptions underscore the critical need for thorough, technically accurate guidance when specifying static control solutions.

## MISPLACED PRIORITIES: WHEN INITIAL QUESTIONS MISS THE MARK

In our extensive experience working alongside architects, designers, engineers, general contractors, and facilities teams, we have observed a consistent pattern in initial inquiries when specifying and evaluating ESD flooring. Regardless of the project's scale or application, initial questions typically focus on the following aspects:

1. What is the cost per square foot of the flooring?
2. Is the flooring conductive or dissipative?
3. Will the flooring require waxing or polishing?
4. What colors are available?

While these initial questions are practical and understandable, focusing primarily on cost, color, or general categories such as conductive versus dissipative often leads to significant oversights. These early inquiries frequently neglect more critical technical and operational considerations, resulting in unforeseen challenges and expenses later in the project.

The actual complexity and total cost associated with effectively implementing ESD flooring extend far beyond initial material pricing and aesthetic preferences. Crucial considerations that are often overlooked include:

- Concrete moisture emission testing and site-specific preparation requirements.
- Failing to distinguish between point and distributed loads of existing mobile equipment.[2]
- Specific aesthetic and uniformity standards for the installation environment.
- Sensitivity levels of the ESD-sensitive devices and equipment handled in the area.
- Installation logistics, such as whether operations can continue during installation or if downtime is required.
- The flooring's practical ability to effectively ground mobile equipment like carts, chairs, and shelving units, which previously required dedicated grounding methods.
- Anticipated occupancy duration and maintenance requirements for the facility.

Ted Dangelmayer, a recognized expert in ESD control, consistently emphasizes approaching static control as an integrated system. In a recent conversation, he told me that "In addition to TR53 auditing, you need a strategic sampling audit of all the elements of the program, including the system, in order to evaluate the quality of the overall system."

Therefore, a recommended and practical approach is to conduct a pilot installation and subject it to a rigorous,

| Operator | Walking Series 1 | Walking Series 2 | Walking Series 3 | Average |
|---|---|---|---|---|
| 1 | 39 | 34 | 32 | 35 |

Table 1: Charge generation results based on single subject 3 peak voltage analysis

real-world audit. This pilot installation should replicate actual operating conditions, including rolling chairs, moving equipment, realistic point loads, and typical maintenance activities, to identify potential issues not evident during standard product evaluations or vendor demonstrations. Careful observation and thorough auditing of this pilot setup can proactively uncover hidden factors, thereby enabling informed decision-making and ensuring that the selected flooring solution genuinely fulfills the facility's operational and technical requirements.

## LESSONS LEARNED FROM AUDITS: WHY ONE TEST SUBJECT IS NEVER ENOUGH

Ron Gibson from Advanced Static Control Consulting (ASCC) critically assessed the reliability of the widely used ANSI/ESD STM97.2 body voltage walking test in a factory located in the Pacific Rim. Typically, compliance evaluations involve a single test subject performing three walking cycles, measuring only peak voltages. If the average peak voltages remain below 100 volts, the flooring-footwear combination is deemed compliant under ANSI/ESD S20.20 standards for Human Body Model (HBM) protection.

Gibson's thorough analysis highlighted significant limitations of this commonly accepted approach. He initially tested seven individuals, all wearing identical ESD footwear, walking on the same conductive vinyl flooring within a factory environment at normal relative humidity (approximately 30-50%). When analyzing this data using only peak voltage averages (as per the standard), the results suggested general compliance.

However, upon further statistical analysis that involved applying a rigorous three-sigma method to the entire voltage waveform data rather than peak voltages alone, the risks appeared considerably greater.

Specifically, Gibson's comprehensive statistical review identified significant variability among subjects:

- Three individuals demonstrated a high probability of exceeding the 100-volt threshold, indicating clear non-compliance concerns.
- Two individuals showed probable voltages close to the threshold, providing minimal margin.
- Only two individuals presented a high probability of voltage generation below 100 volts.

The critical distinction emerged when Gibson shifted from traditional peak-voltage analysis to full-waveform analysis with a three-sigma calculation. By calculating the mean voltage and standard deviation from the complete data set and adding three standard deviations to this mean, he effectively quantified a realistic worst-case scenario. This thorough statistical approach clearly illustrated that actual body voltages could significantly exceed values derived from simple peak-voltage measurements, increasing the potential for damaging ESD events.

Moreover, this risk assessment remains conservative since Gibson's data was collected under typical factory humidity conditions (around 30-50%). Had the tests been performed under the lower relative humidity conditions (e.g., 12% RH) used in standard STM 97.2 qualification tests, the resulting voltages likely would have been significantly higher, amplifying the risk even further. Additionally, the inherent subjectivity of the walking test, including variability arising from individual electrical capacitance, hydration levels, foot size, footwear types, walking style, speed, and body movements, introduces further uncertainty and underscores the inadequacy of relying on a single-subject evaluation.

Earlier research by Jeremy Smallwood and David Swenson (2011) strongly supports Gibson's conclusions. In their study "Evaluation of performance of footwear and flooring systems in combination with personnel using voltage probability analysis,"[3] Smallwood and Swenson explicitly noted that traditional methods focusing only on peak voltage measurements fail to adequately evaluate the likelihood of exceeding critical voltage thresholds. They recommended comprehensive waveform analysis involving multiple test subjects to quantify operational risks accurately. This judgment is particularly vital, recognizing that in environments such as control rooms and flight towers, ESD protection is fundamentally a task of risk prevention and management.

Together, these findings underscore the importance of adopting comprehensive testing methodologies for effective ESD protection. Organizations must move beyond simplistic or limited peak-voltage measurements and implement full waveform testing coupled with rigorous statistical analysis. Ideally, this should include pilot installations conducted under realistic operational conditions, using actual equipment, chairs, carts, and multiple personnel. Evaluating flooring in situ provides the most reliable insight into real-world performance, ensuring robust and effective static control throughout the facility.

| Operator | Walking Series 1 | Walking Series 2 | Walking Series 3 | 9 Pk - Average |
|---|---|---|---|---|
| 1 | 39 | 34 | 32 | 35 |
| 2 | 77 | 67 | 65 | 70 |
| 3 | 85 | 73 | 65 | 74.3 |
| 4 | 75 | 69 | 53 | 65.7 |
| 5 | 61 | 59 | 52 | 57.3 |
| 6 | 51 | 43 | 39 | 44.3 |
| 7 | 73 | 64 | 43 | 60 |
| | | | Overall Average | 58.1 |
| | | | STDDEV | 15.4 |
| | | | 3x STDDEV | 46.1 |
| | | | **Maximum V** | **104.2** |
| | | | Minimum V | 11.9 |

Table 2: Probabilistic charge generation analysis of peak voltages across multiple test subjects

## STILL TETHERING: WHEN CONDUCTIVE FLOORING DOESN'T ENSURE TRUE MOBILITY

In principle, installing conductive ESD flooring should eliminate the need for tethered wrist straps during standing or walking activities and remove the necessity for grounding wires attached to mobile equipment. Yet many facilities find themselves continuing to tether carts, chairs, and mobile workstations even after installing flooring that meets standard compliance criteria. Why does this situation persist?

Post-installation audits frequently reveal that the anticipated mobility benefits of compliant flooring are not realized, not due to a lack of inherent floor conductivity, but because mobile equipment cannot reliably maintain electrical contact with the floor's conductive surface.

Sometimes the root cause is attributed to faulty grounding components, such as ineffective drag chains, inappropriate casters, or shelving sleeves that electrically isolate shelves from their posts. However, in most instances, the underlying issue lies with the flooring itself. For example, certain Generation 2 epoxy coatings incorporate a conductive layer beneath the surface but lack sufficient surface-level conductivity. Similarly, poorly designed conductive tiles with inadequate or unevenly distributed conductive granules compromise the effectiveness of grounding performance.

| Operator | 9 PK - Average | 0.13% Probability |
|---|---|---|
| 1 | 35 | 63 |
| 2 | 70 | **133** |
| 3 | 74.33 | 98 |
| 4 | 65.67 | 99 |
| 5 | 57.33 | **103** |
| 6 | 44.33 | 61 |
| 7 | 60 | **107** |
| Overall Average | 58.1 | 95 |

Table 3: Probabilistic charge generation analysis of entire voltage curve across multiple test subjects

In a previous article[4], we examined this critical yet frequently overlooked gap in standard compliance practices. Specifically, we challenged the common assumption that successfully passing the ANSI/ESD STM7.1 resistance-to-ground test automatically ensures compliance with all other ANSI/ESD S20.20 resistance criteria. However, this assumption is fundamentally flawed. In our case study, we demonstrated a notable 16% failure rate when measuring resistance from carts to ground, even though the measurements were taken on flooring previously verified as conductive according to STM7.1.

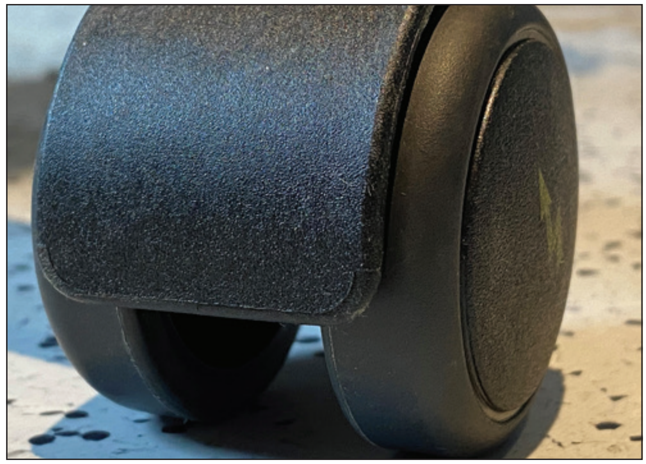

Figure 1: Conductive chair caster on an ESD floor

The ANSI/ESD STM7.1 standard evaluates a floor's conductivity using a controlled laboratory scenario, a five pound probe with a 2.5 inch diameter (4.91" area). In real-world operations, however, mobile objects like carts, chairs, shelves, and equipment racks often make contact with the floor through significantly smaller surfaces, such as the thin outer edge of a caster or a small metal leveling foot. A typical five caster chair probably makes less than one square inch of total contact.

As detailed in [4], passing the STM7.1 compliance test confirms general floor conductivity but does not guarantee effective grounding or bonding in practical conditions. True grounding performance depends entirely on whether these small, real-world contact points consistently engage conductive elements within the flooring material. If casters or leveling feet rest on insulative fillers, non-conductive surface textures, or gaps between conductive granules, the equipment remains electrically isolated, regardless of nominal compliance on paper.

The practical consequence of this oversight is that casters, shelves, and similar mobile equipment effectively become electrically isolated, or "floating," unable to dissipate static charges reliably. This scenario leaves operators susceptible to static shocks, exposes sensitive electronic components to damage, and negates the anticipated advantages of mobile grounding.

This issue arises frequently because many engineers and facility managers evaluating ESD flooring for the first time may inadvertently overlook critical supplementary requirements, such as those outlined in ANSI/ESD STM4.1. Typically, these problems only come to light during detailed audits or after operational failures linked to static discharge events occur.

To ensure robust static control under realistic operating conditions, specifiers must look beyond basic resistance compliance tests. A thorough and effective evaluation of ESD flooring should involve:

- Testing mobile equipment, including carts, chairs, and shelving, under realistic operational loads.
- Verifying electrical continuity, specifically at caster-to-floor and leveling foot-to-floor interfaces.
- Carefully examining the flooring's surface construction to confirm consistent and reliable conductive pathways.
- Conducting body voltage and charge decay tests to evaluate real-world static dissipation performance comprehensively.

In summary, effective static control demands more than simply meeting isolated resistance compliance tests. Conducting a carefully planned pilot installation and performing a rigorous, system-level evaluation under actual operational conditions can proactively identify grounding issues before full-scale deployment. Such real-world testing ensures reliable grounding performance for all types of equipment, both mobile and stationary, and provides genuine, comprehensive protection for sensitive electronics. A pilot approach thus helps organizations avoid the common pitfalls associated with relying solely on isolated compliance data or superficial testing methods.

## WHEN REDUNDANCY FAILS: ENSURING SYSTEM-LEVEL RELIABILITY IN ESD CONTROL

In strictly controlled manufacturing environments, adherence to static control protocols, including the consistent use of heel straps, wrist straps, personnel grounding verification, and comprehensive system grounding methods, is typically rigorous, regularly audited, and well documented. However, in critical settings such as SCIFs, research labs, data centers, and academic facilities, static control measures often become self-regulated, inconsistently applied, or overlooked, potentially introducing significant unnoticed vulnerabilities.

To counteract these deficiencies, some facilities implement passive redundancy measures, such as using conductive flooring combined with static control seating. But does this redundancy reliably achieve effective ESD protection?

A recent internal audit conducted at a semiconductor laboratory highlighted inherent risks associated with relying on passive grounding strategies, even when redundancy appeared sufficient on paper. In this instance, an engineer proactively installed a pilot area consisting of interlocking conductive flooring paired with conductive ESD chairs featuring metal casters. The flooring used was notable for its relatively low surface density of conductive granules.

According to supplier test reports, the flooring met ANSI/ESD S20.20 compliance criteria based on ANSI/ESD STM7.1 resistance-to-ground and ANSI/ESD STM97.2 body voltage measurements. The ESD chairs individually passed ANSI/ESD STM12.1 resistance tests, verifying their individual compliance.

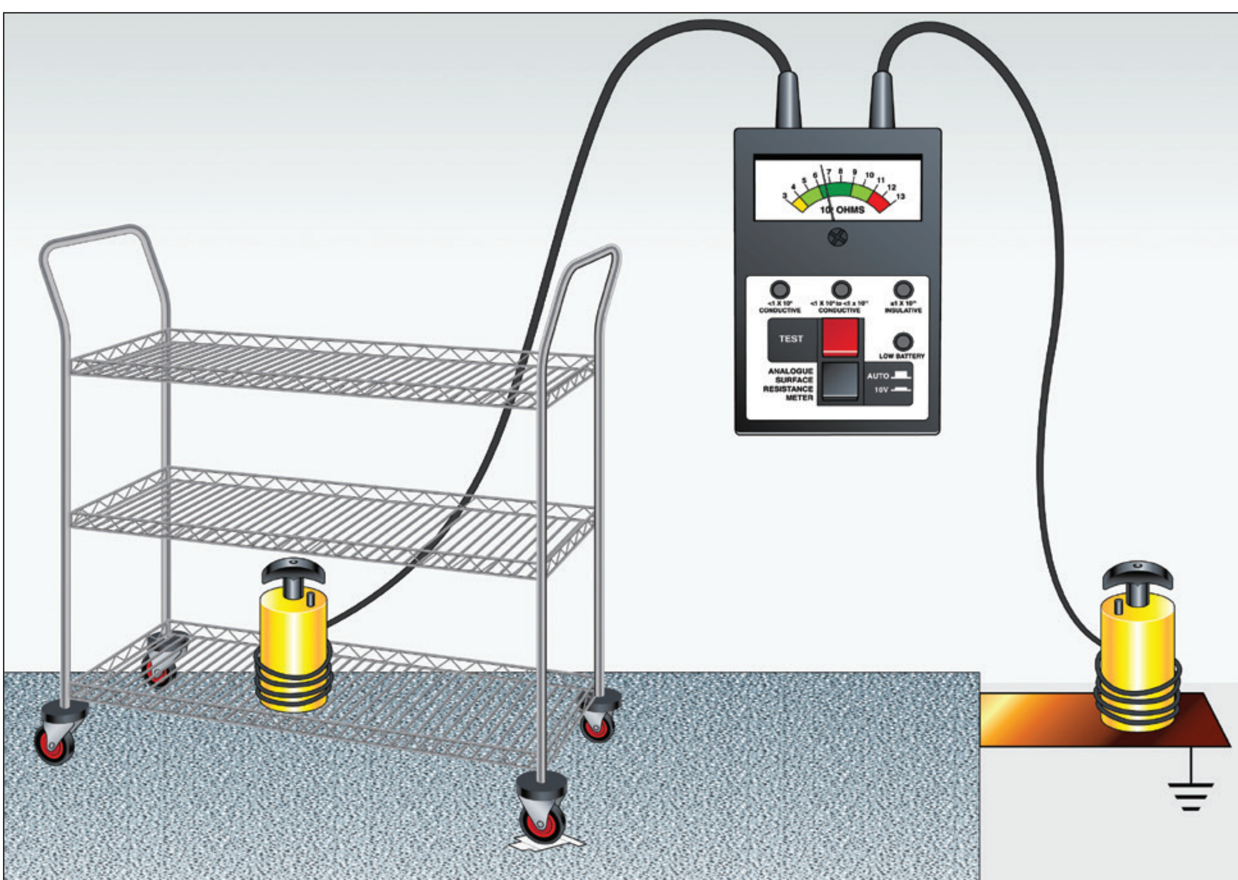


Figure 2: Resistance to ground measurement in series through conductive floor to groundable point

However, when tested as an integrated system, with chairs grounded through caster contact with the conductive flooring, the performance deteriorated significantly. Resistance measurements between the chair casters and the floor frequently exceeded the ANSI/ESD S20.20 threshold of <1.0 × $10^9$ ohms. Real-world testing using a portable charge plate monitor, where the engineer moved around in an ESD chair without supplementary grounding methods such as wrist straps or ESD footwear, revealed body voltage levels ranging dramatically from approximately -188 volts to +142 volts, significantly surpassing acceptable thresholds. This has critical implications for environments like SCIFs and data centers, where additional static control measures may not be practical or enforceable.

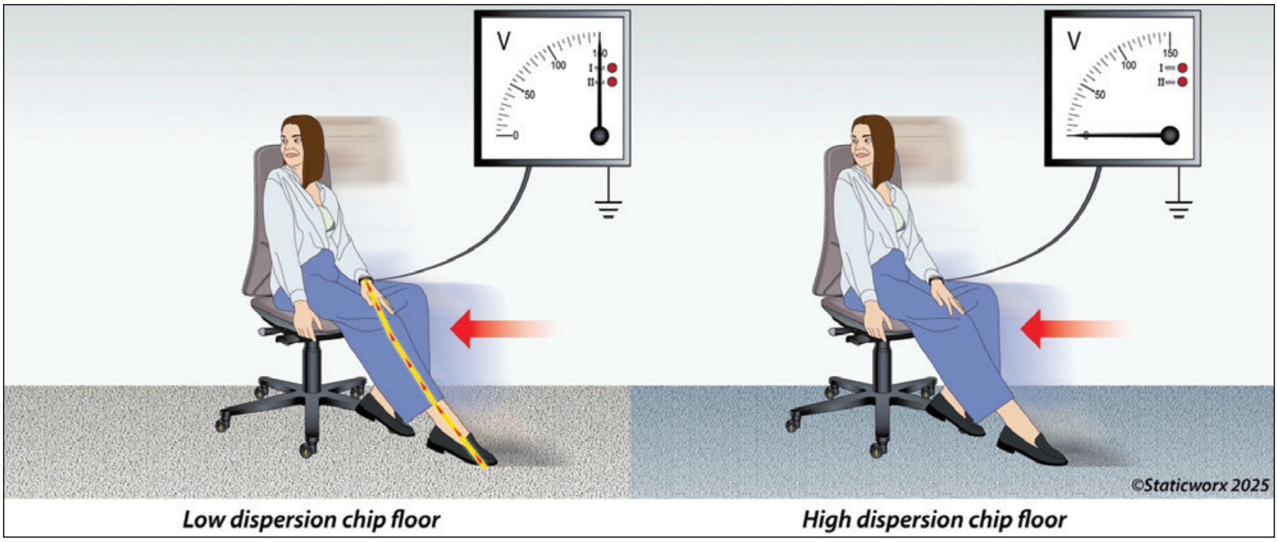


Figure 3: Resistance to ground and body voltage generation on a person rolling a caster chair across a conductive floor (old tile-low dispersion, black speckles; new tile-high dispersion, black speckles)

| | **Resistance to Ground 5lb weight on TILE** | | **Resistance to Ground 5lb weight on CHAIR** | | **Body Voltage Sitting On Chair No Wrist Strap or Foot Grounders Use One Foot to Roll Chair For 30s** | | | |
|---|---|---|---|---|---|---|---|---|
| Repeatability Test/ Tile Location | Old Tile | New Tile | Chair on Old Tile | Chair on New Tile | Old Tile Min V | Old Tile Max V | New Tile Min V | New Tile Max V |
| 1 | 9.47E+05 | 1.76E+05 | **2.45E+11** | 1.16E+06 | **-188** | 49 | 0 | 0 |
| 2 | 1.45E+06 | 1.42E+05 | 5.00E+07 | 1.13E+06 | -78 | **135** | 0 | 0 |
| 3 | 7.64E+06 | 2.23E+05 | **2.48E+10** | 1.08E+06 | -15 | 72 | 0 | 0 |
| 4 | 9.74E+05 | 2.04E+05 | 1.21E+08 | 1.09E+06 | -45 | **142** | 0 | 1 |
| 5 | 1.40E+06 | 3.70E+05 | 2.18E+06 | 1.01E+06 | **-161** | **103** | 0 | 0 |
| 6 | 7.77E+06 | 3.41E+05 | 2.92E+06 | 1.05E+06 | -61 | 94 | 0 | 0 |
| 7 | 1.77E+06 | 3.27E+05 | **2.44E+11** | 3.61E+06 | **-120** | 70 | 0 | 0 |
| 8 | 2.64E+06 | 2.43E+05 | **1.73E+11** | 1.00E+06 | -10 | 96 | 0 | 0 |
| 9 | 5.01E+06 | 3.98E+05 | 3.47E+07 | 1.03E+06 | **-153** | 92 | 0 | 0 |
| 10 | 1.07E+07 | 2.94E+05 | **2.91E+11** | 1.19E+06 | **-121** | 71 | 0 | 0 |

Table 4: Floor-to-ground resistance (floor only), chair to ground resistance measured through each floor, body voltage generated when a seated person pushes off each floor

To explore the issue further, the engineer replaced a small pilot area of the low-density conductive flooring with an alternative interlocking floor system featuring a higher dispersion and density of conductive surface granules. Repeating the same tests under identical conditions yielded dramatically improved results:

- On the original low-density flooring, resistance from chair to ground varied significantly, from acceptable levels (~$10^6$ ohms) to highly non-compliant values (~$10^{11}$ ohms).
- Corresponding body voltage readings were unacceptably high, ranging from -188 volts to +142 volts.
- On the replacement flooring with higher conductive granule density, resistance measurements stabilized consistently below $1.2 \times 10^6$ ohms, and body voltage readings remained near zero volts.

This practical evaluation underscores several crucial insights:

1. *ESD flooring does not operate in isolation:* It serves as the critical grounding interface for chairs, carts, shelves, and all mobile equipment.
2. *Compliance of individual components alone does not ensure reliable system-level performance:* Interfaces between components—such as the contact between casters and conductive flooring elements—are critical.
3. *Passing basic resistance tests (ANSI/ESD STM7.1) alone is insufficient:* Effective grounding performance in real-world scenarios relies on the actual, consistent contact between small contact points (e.g., caster wheels) and conductive granules on the floor surface.
4. *Without enforced additional grounding methods like wrist straps or footwear, the flooring becomes the sole grounding mechanism*, significantly increasing dependence on its functional effectiveness.

The engineer's proactive installation of a carefully monitored pilot area emphasizes the importance of rigorous, real-world testing in identifying and resolving system-level issues. This strategic approach allowed early identification of integration problems, clearly differentiating compliance on paper from genuine operational reliability. By conducting this pilot, the engineer pinpointed the weakest link in the ESD control system, enabling the implementation of a highly effective passive static control solution. This solution successfully mitigated compliance issues typically associated with inconsistent use of wrist straps and ESD footwear.

Drawing from physicist Richard Feynman's insights, true understanding of any system involves the capacity to clearly and simply articulate how each component integrates into the overall system. Merely confirming compliance through isolated tests or technical datasheets is insufficient. Instead, organizations must rigorously test pilot installations under realistic operating conditions, involving actual chairs, carts, material-handling equipment, and realistic daily operational activities. Such proactive validation uncovers critical issues that isolated compliance tests alone might miss.

Aligned with industry best practices, a comprehensive evaluation beyond basic compliance standards is essential. Organizations must move beyond simply asking, "Does the flooring meet the standard?" to more crucial questions such as, "Does it perform reliably in our environment, with our actual equipment, under realistic operational conditions?" By adopting this rigorous and holistic approach, organizations ensure robust static control reliability, effectively safeguarding sensitive electronic components from unintended risks and vulnerabilities.

## ENDNOTES


1. Justin Kruger and David Dunning, "Unskilled and Unaware of It: How Difficulties in Recognizing One's Own Incompetence Lead to Inflated Self-Assessments," *Journal of Personality and Social Psychology*, 1999, Vol. 77, No. 6, pp. 1121-1134.
2. Jordan Tlumak, "Point Load vs. Distributed Load," *OneRack* website, May 27, 2024.
3. Jeremy Smallwood and David E. Swenson, "Evaluation of performance of footwear and flooring systems in combination with personnel using voltage probability analysis," *Journal of Physics: Conference Series*, 301 012064.
4. David Long, "Caster Contact: The Achilles Heel of ESD Floors," *In Compliance Magazine*, September 2021.

# DIE-TO-DIE ESD DISCHARGE CURRENT ANALYSIS

By Pasi Tamminen and Toni Viheriäkoski

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Advanced system on a chip (SoC) components use multi-die package technologies where single silicon chips are assembled on top of each other, beside each other on a larger interposer, or by combining various 3D packaging methods together. Connections between chips are formed by utilizing multiple technologies such as flip chips, substrates, interposers, silicon bridges, bond wires, micro bumps, and through-silicon-vias (TSV).

A single SoC can have hundreds to thousands of external connections between a component package and a printed circuit board (PCB). These connections require certain robustness against external electrical stress and can often tolerate electrostatic discharge (ESD) withstand voltages of more than 250 V charged board model (CDM) and 500 V human body model (HBM) during qualification tests. Each of these on-chip protection structures requires surface area from the silicon, but due to a limited number of connections, this is still feasible.

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There are more die-to-die (D2D) interconnections inside an SoC than between the package and PCB, and it is estimated that the number of interconnections increases with future technologies [1][2]. Most interconnections are well protected after the SoC is assembled and don't need the same level of ESD robustness as the external interfaces. A certain basic ESD robustness is still required for frontend and backend processes, even though these are made inside a well-controlled cleanroom environment, fulfilling electrostatic protective area (EPA) precautions.

D2D assembly process phase in the backend can have CDM-like ESD risks. Here, bare dies are joined together with an automated handler so that interconnection surfaces directly contact each other. Handlers are well grounded, and ionizers mitigate electrostatic charge buildup. However, it is challenging to control die charging in a fast-paced process where parts contain both dielectrics and conductors. Ionization time is limited, and dies can have charges trapped on opposite surfaces facing trays and pickup nozzles. Ionizers can typically limit charging of large objects below ±10 V, but it is challenging to limit charging of small chips during fast pick and place processes.

There is limited information available about ESD current waveforms from small capacitance sources when the initial potential difference is below 100 V. Several papers discuss discharges between IC packages, and ESD events between dies should have mostly similar initial conditions [3]. Here, the discharge current waveform depends on the initial charge, capacitance, and discharge path. Similarly, the quasistatic ESD source capacitance of the die depends on the size, location, surroundings, and design of the die.

In this study, 3D electromagnetic solvers and circuit calculations are used to study D2D discharge events. Here, the main target is to identify significant discharge parameters affecting ESD current waveforms. The key parameters to study are the contact potential, resistance, rise time, peak current, and length of the pulse. This data is used to estimate reasonable protection targets for D2D interfaces and to give information on how to measure D2D discharge events [4].

## METHODS

### *Discharge Current Calculations*

ESD current waveform calculations are made in the time domain by using SPICE circuits presented in Figure 1 and Figure 2. Here, the two discrete components *R*_series and *L*_series are the parasitic series resistance and inductance of the discharge path. Figure 2 has the same circuit but now with additional discrete components presenting on-chip discharge path termination. This termination can contain on-chip protection structures and transistor input gate parameters, which are simplified here as 50 Ω termination and parasitic LC components. The component *F* with one or more ports is the calculated frequency response of the 3D discharge setup [5].

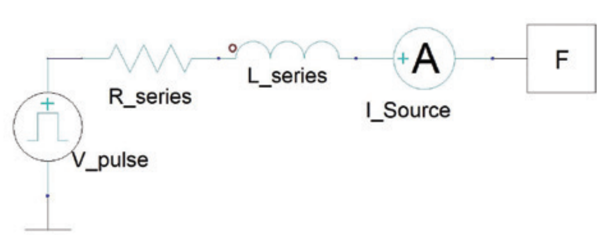


Figure 1: Simplified SPICE equivalent circuit for ESD discharge current calculations with one port setup

Figure 3 shows an example of a 3D setup for a µBGA die assembly with one signal port (enlarged for visualization) between the interposer and IC. This port is the discharge contact point between the die and interposer, and can be placed on any of the component joints depending on the discharge scenario under investigation. Both the IC and interposer are made of aluminum. A pick-up nozzle is located above the µBGA and contains grounded conductors, which define part of the source capacitance of the µBGA.

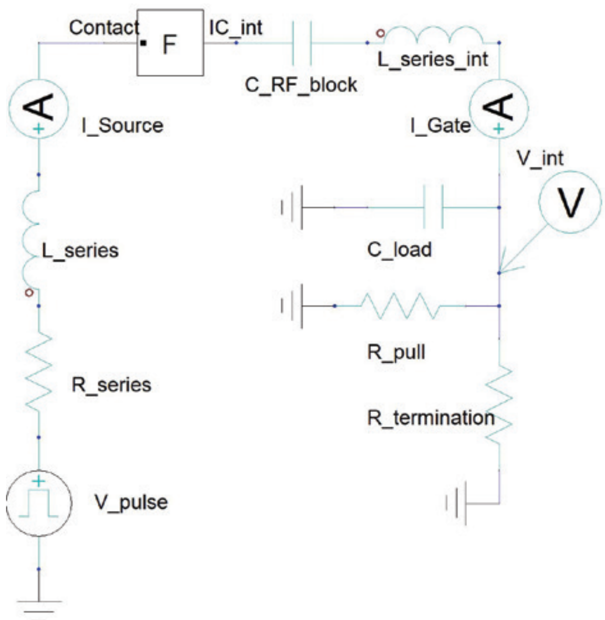


Figure 2: SPICE equivalent circuit for ESD discharge current calculations with two ports. The first port is the location of the discharge, and the second is used to model on-chip ESD protection circuits.

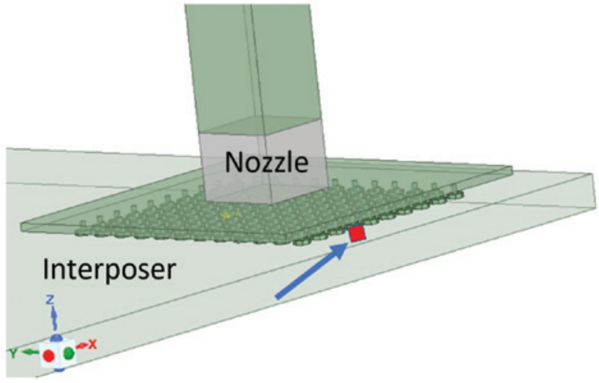


Figure 3: A simplified simulation setup where a pickup nozzle places a µBGA component on an interposer. µBGA has 120 micro bumps with 150 µm pitch. The red rectangle is the excitation port (discharge point) used to calculate the frequency response of the setup.

Figure 4 presents a more complex scenario, in which a µBGA is assembled on top of a 28 mm x 28 mm size IC using a nozzle. The discharge path is marked with red color, and an arrow indicates the discharge location. Ports are placed at the discharge point and at the bondwire contact point on the surface of the die. In this way, we can calculate discharge currents and voltages at both locations by using the circuit of Figure 2.

There can be multiple ports in one 3D setup so that different discharge point calculations can be made by using the same 3D model. The model can contain frequency-dependent dielectrics and conductivity based on the used materials.

## BANDWIDTH REQUIREMENTS

The SPICE circuits in Figure 1 and Figure 2 can calculate discharge current waveforms both by using 3D frequency response data of the 3D model or by replacing the model with a simplified RLC representation of the ESD source circuit. Here, the source ESD capacitance and parasitic inductance are the key parameters when considering the required bandwidth and rise time. These values can be calculated with basic analytical equations or with 3D electromagnetic simulation tools as presented in

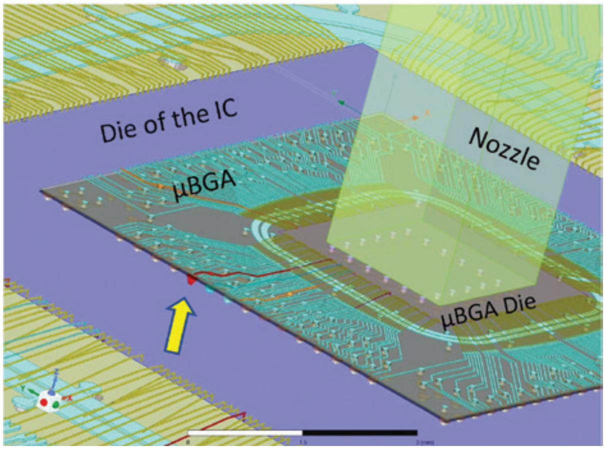


Figure 4: 3D assembly scenario where 7 mm x 7 mm size µBGA is assembled on top of a larger 28x28 mm size IC. Both components have a leadframe, bondwires, and joints under the package.

Figure 5 [3]–[6]. Here, the die is simplified as an aluminum block placed at varying distances from the reference surface. Unlike RLC circuits or analytic calculations, 3D frequency response models contain a full description of the source model frequency behavior, and these are used in this study. For example, one port 3D model produces S11 response calculated at the port location as shown in Figure 6.

The physical size of dies can vary from a few square millimeters up to >500 mm$^2$. ESD risks should decrease with a smaller die size due to a lower source ESD capacitance and stored energy. However, a smaller die can produce faster rise time pulses, and smaller dies can get higher quasi-static voltages with the same amount of charge. With large size dies, the source capacitance increases, thus also increasing the rise time, peak discharge current, and discharge energy, if compared to a small size die with the same initial voltage.

The required bandwidth for a measured or simulated D2D discharge event depends on the materials used, the discharge voltage, and the physical size of the

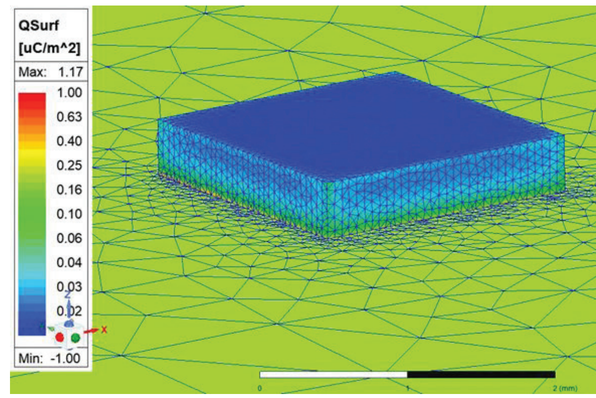


Figure 5: 2 mm x 2 mm x 0.4 mm size charged die 10 µm above the ground plane. An adaptive mesh matrix is visible on the model surface.

setup. With small dies (a few square millimeters in size) most of the discharge energy is at frequencies above 20 GHz, if external discharge path series parasitics are not included. In this study, the bandwidth is typically calculated for 10 MHz – 100 GHz.

Figure 6 presents an example S11 data for three different discharge scenarios for small-sized dies with 10 μm or 20 μm distance to the ground. This shows that the required calculation and measurement bandwidth should be >25 GHz to capture the rise time and peak discharge current at the contact point.

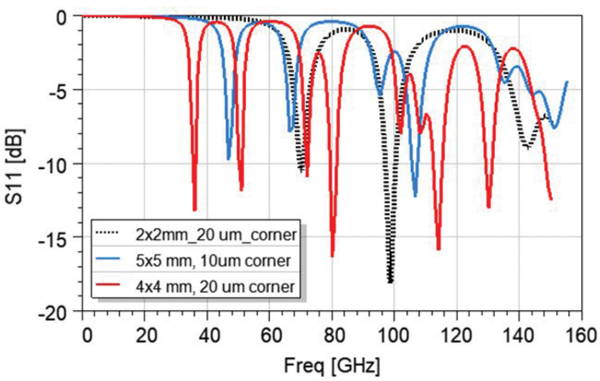


Figure 6: An example frequency response of D2D scenario when calculated at the discharge point. Here, the discharge point is the corner of the die with varying die area and distance to the ground reference.

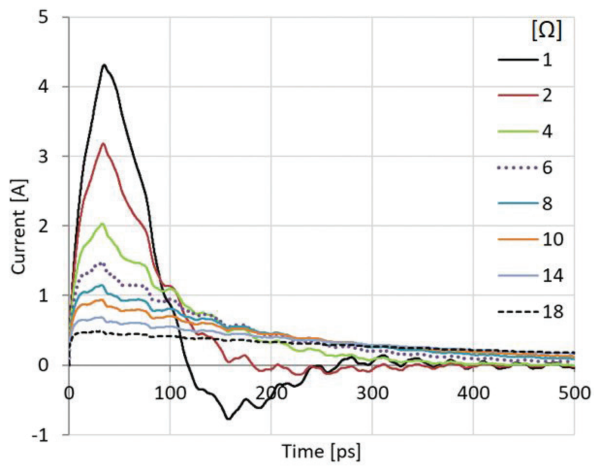


Figure 7: Discharge current waveforms from 5 mm x 5 mm size die. The series contact resistance varies between 1 Ω and 18 Ω. 10 V initial potential and the size of the gap is 10 μm.

### *Inductance and Resistance*

The resistance and inductance of the plasma channel change based on the length and width of the channel when discharge voltages are above Paschen limits. However, the die assembly is made in a controlled environment where charge buildup is limited. There is also mutual capacitive coupling between electrically floating charged objects, decreasing the discharge voltage before a physical contact [12]. Therefore, with voltage differences below tens of volts and a narrow <10 μm range gap between dies, Paschen's law does not apply [7][8].

The strength of the E-field can be high in small gaps even if the potential difference would be just a few Volts. For example, 1 V potential and 1 μm gap create

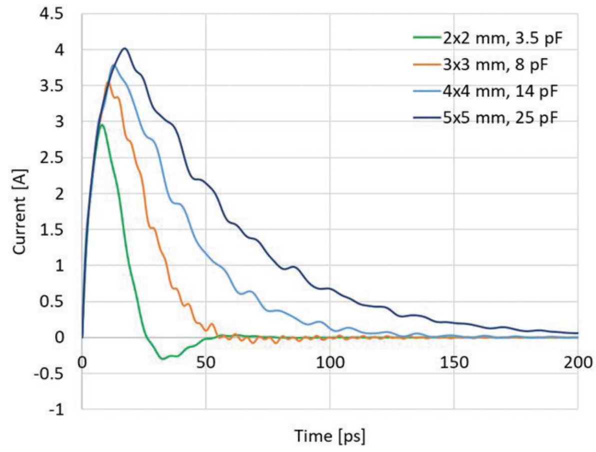


Figure 8: Discharge current waveforms with different-sized dies. R_series=2 Ω, L_series=5 pH, V_pulse=10 V, gap=10 μm

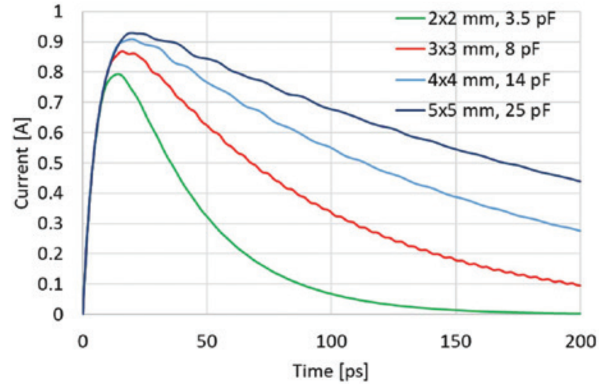


Figure 9: Discharge current waveforms with different-sized dies. R_series=10 Ω, L_series=50 pH, V_pulse=10 V, gap=10 μm

an E-field of 1 MV/m. An electric field emission in air would require significantly higher field strength to pull electrons free; thus, we can assume high resistance and limited current flow before a physical contact [9][10]. In this case, conductors of the die will most likely discharge only when contacting another surface, and thereby, there is no major additional series inductance at the discharge point due to the spark channel.

There can be significant contact resistance during a low voltage transient event between conductors. Therefore, when a die contacts another conductor, the contact resistance can vary from less than one ohm to some unknown higher value. Some additional variation to the contact resistance comes from possible atmospheric pressure differences, surface oxidation, contact area, roughness of surfaces, contact force, protective gases, moisture, power of the discharge current, and varying temperatures used inside the D2D assembly handling environment [10][11]. A contact resistance is treated as a variable and calculated or estimated from RLC circuit waveforms matching with measured discharge current waveforms [6]. The contact resistance can vary during the discharge, but in this study, the resistance is kept constant in calculations [4].

## RESULTS

### *Simplified Discharge Setup*

A simplified discharge scenario based on the circuit shown in Figure 1 and a solid aluminum block source as shown in Figure 5 produces ESD current waveforms presented in Figure 7 at the discharge point when the series resistance is between one ohm and 18 Ω. Here, the size of the “die” is 5 mm × 5 mm × 0.4 mm, a gap to the reference ground is 10 um, series inductance is 50 pH, and the discharge potential is 10 V. The current waveform is underdamped when the resistance is below four ohms and overdamped above this value. The peak current and rise time depend mostly on the series resistance and inductance, and the frequency response of the setup with 25 pF source capacitance. Below 10 Ω the peak current can be a few amps with the used 10 V initial voltage.

Figure 8 and Figure 9 have the same setup, but now the physical area of the die is between 4 mm$^2$ and 25 mm$^2$. The series resistance and inductance are 2 Ω and 5 pH in Figure 8, and 10 Ω and 50 pH in Figure 9.

These waveforms can be assumed to be worst-case discharge scenarios due to the relatively low series resistance and inductance. The discharge peak current is between 3 A and 4 A in Figure 8, and it drops below 1 A in Figure 9 due to the higher resistance.

Figure 10 and Figure 11 repeat the same simulations, but now the gap length is 20 µm, and the die size is larger, 56.3 mm$^2$ and 100 mm$^2$. The rise time increases with larger dies, and the peak current follows the source capacitance.

Based on these calculations, the series inductance and resistance are sensitive parameters from the discharge peak current and the rise time point of view. The source capacitance charges the length of the pulse, the rise time, and the total energy content. With overdamped current waveforms, the initial rise time of the current can be just tens of picoseconds due to a lower peak value, even if the total period of the pulse would be close to one nanosecond.

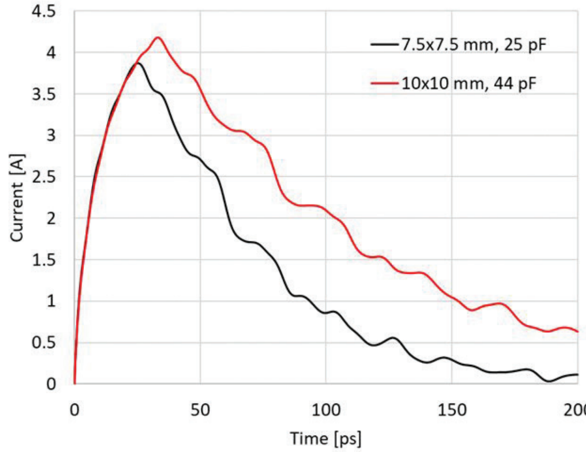


Figure 10: Discharge current waveforms with different-sized dies. R_series=2 Ω, L_series=5 pH, V_pulse=10 V, gap=20 µm. Die size is 56.3 mm$^2$ and 100 mm$^2$

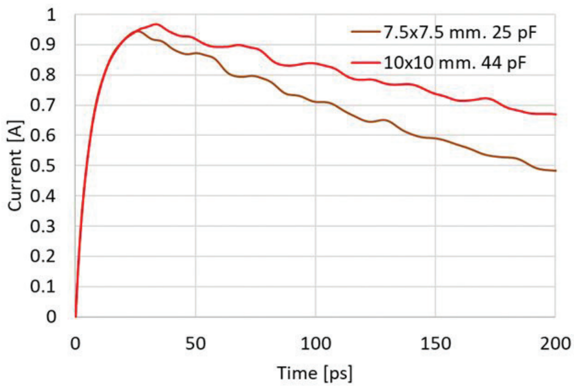


Figure 11: Discharge current waveforms with different-sized dies. R_series=10 Ω, L_series=50 pH, V_pulse=10 V, gap=20 µm. Die size is 56.3 mm$^2$ and 100 mm$^2$

### *Capacitive Coupling and Charge Distribution*

The voltage difference at the discharge moment depends on the charge distribution and mutual capacitive coupling between dies [12]. In addition, a die held by a nozzle may not be perfectly parallel to the reference surface. In this case, one edge or corner can contact the reference surface at first, as presented in Figure 12. This changes capacitive coupling, electrostatic charge distribution, and the discharge current waveform at the contact point.

Figures 13 – 15 show the potential of two dies and the potential difference between dies when they approach each other. Dies are modelled with ideal solid aluminum blocks. The smaller 4 mm × 4 mm size die has a constant 100 pC static charge, and the larger 14 mm × 14 mm size die is either grounded or electrically floating. In Figure 13, both dies are in parallel position, in Figure 14, the smaller die is tilted 0.5°, and in Figure 15, it is tilted 1°. Above the smaller die is a grounded nozzle with a 0.2 mm thick dielectric isolation layer touching the die surface, so that mixed charge distribution is part of the calculation.

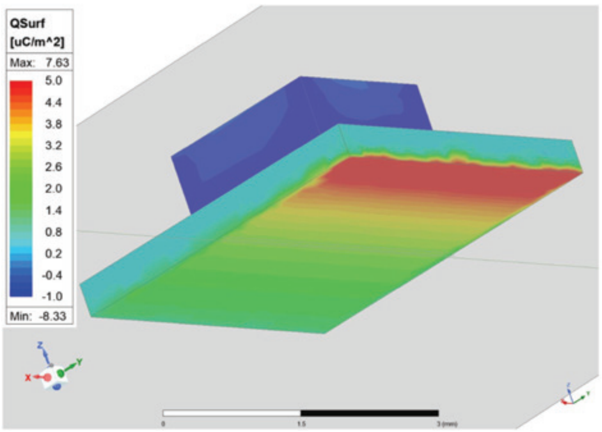


Figure 12: Surface charge density of 4 mm x 4 mm x 0.4 mm size die with 1-degree tilt and 10 µm minimum distance to the ground plane. There is more charge stored at the bottom of the die around the edge closest to the ground plane.

When both dies are parallel and the larger die is electrically floating (GND float), the final voltage difference between dies is 1.8 V at 5 μm distance. The voltage difference increases to 3.4 V if the larger die is grounded (GND 0 V). Similarly, with a tilted die, the voltage difference is smaller when both dies are electrically floating. However, a 0.5° tilt angle already increases the voltage difference to 6.9 V and 10.5 V with floating and grounded scenarios in Figure 14. 1° tilt angle increases the voltage difference to 10.4 V and 15.5 V, as shown in Figure 15.

Based on Figures 13 – 15, the expected typical discharge voltage during a D2D ESD event in a controlled environment could be less than about 10 V at 5 μm distance, even if the initial voltage of the die would be >100 V after pickup. However, the real potential values can vary in the die assembly as dies are not ideal solid metal blocks with an even surface at the bottom coupling to the reference surface.

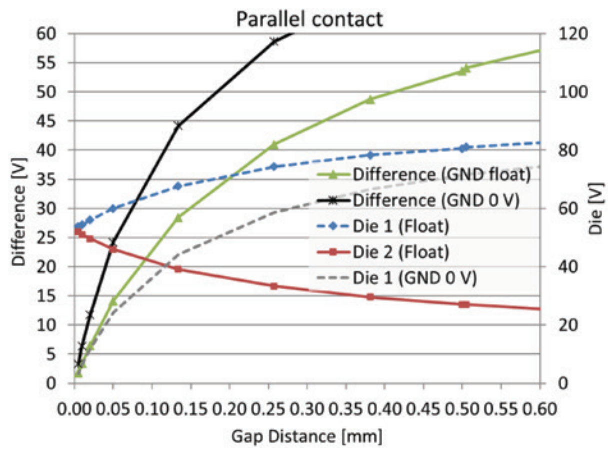


Figure 13: 4 mm × 4 mm size Die 1 with 100 pC static charge moves close to 14 mm × 14 mm size Die 2. Die 2 is grounded or electrically floating.

Figure 16 has a calculation where a nozzle with 16 mm² area is holding a 25 mm² size die with solder pumps under the package. This is a similar setup as that presented in Figure 3. In this case, the capacitive coupling effect is weaker due to the different charge distribution. The total static charge of the die is set to 1 nC when it is held by a conducting nozzle and 120 pC when the die is held by a non-conducting ceramic nozzle. The reference surface, an electrically floating interposer, has no charge. With these initial charge values, dies have 270 V initial potential when kept at 0.5 mm distance from the interposer. With the conducting nozzle, the voltage difference is about two times higher when the die touches the interposer. However, this phenomenon depends on the nozzle-die geometry as presented in Figure 17. Here, the size of the metallic nozzle is fixed to 16 mm², and the size of the die varies. If the size of the nozzle is large in comparison to the area of the die, the capacitive coupling phenomenon is weaker when the die approaches the interposer. Figure 17 also shows results without a nozzle for comparison.

As a summary, it would be better to use non-conductive low-capacitance nozzles when assembling dies. In addition, it would be better to let the second die or interposer electrically float to magnify capacitive coupling phenomena during assembly. Also, it would be good to keep the die parallel to the reference surface to magnify capacitive coupling phenomena.

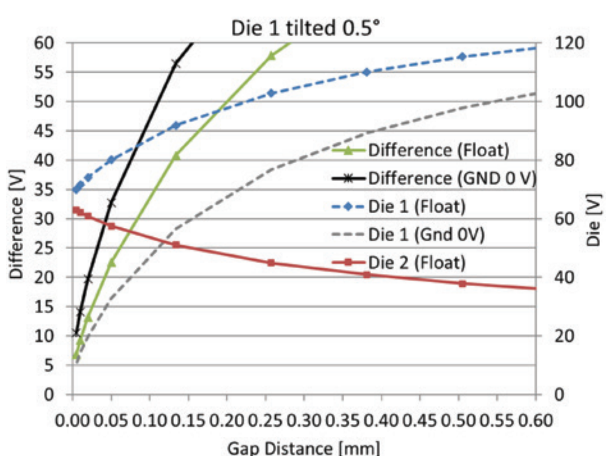


Figure 14: Die 1 with 100 pC static charge and 0.5° tilt moves close to Die 2. Die 2 is grounded or electrically floating.

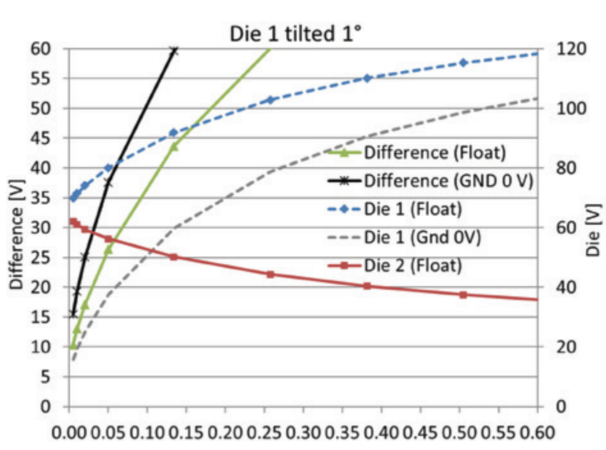


Figure 15: Die 1 with 100 pC static charge and 1° tilt moves close to Die 2. Die 2 is grounded or electrically floating.

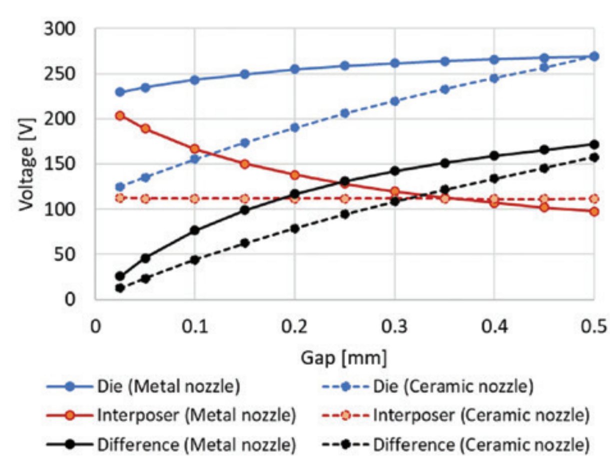


Figure 16: Capacitive coupling in a die assembly with a metallic and ceramic nozzle. The die has micro pumps under the package.

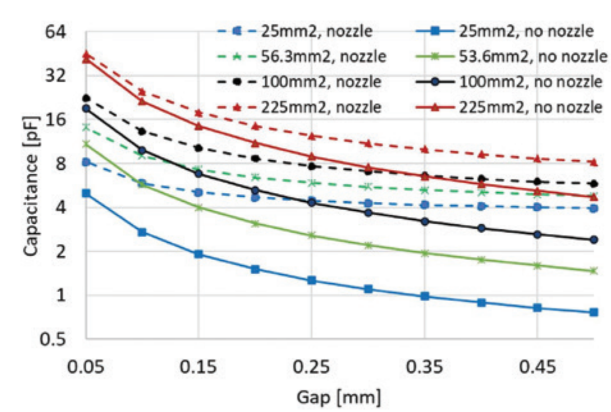


Figure 17: Capacitive coupling in a die assembly with a metallic nozzle and without a nozzle. Die has micro pumps under the package.

### *Discharge Current Analysis*

Figure 18 has discharge current waveforms between two dies representing the scenarios presented in Figures 13 – 15. In this calculation, the smaller die has a fixed 10 V potential and is tilted 0˚, 0.5˚, or 1˚ in comparison to the larger electrically floating die. The peak discharge current is the highest when dies are parallel, and the current decreases with increasing tilt angle due to the smaller source capacitance. However, capacitive coupling is weaker with tilted dies, and this would magnify the voltage difference and change the contact resistance in real-life discharge scenarios. The final discharge current waveform would be case-specific, depending on the die construction, contact resistance, and variations with the die alignment.

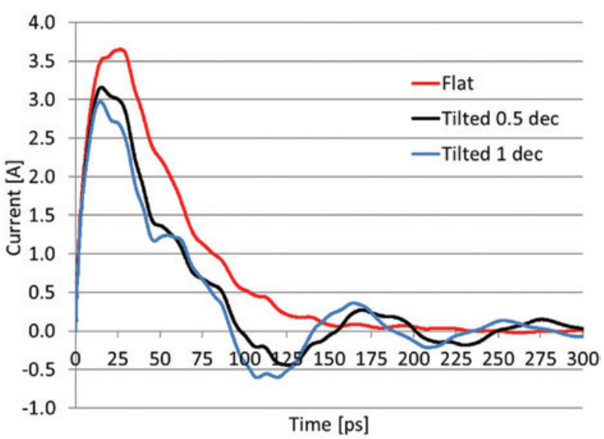


Figure 18: Discharge current waveform from a 4 mm x 4 mm size die to another electrically floating die. The die is parallel or tilted with a constant 10 μm minimum gap and a fixed 10 V potential between the two dies.

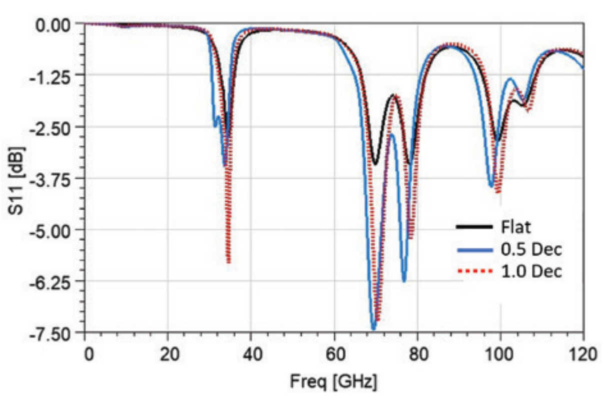


Figure 19: Frequency response of the D2D discharge setup

Figure 19 shows the frequency response of the source circuits for the three discharge waveforms presented in Figure 18. Alignment of the die changes the frequency response of the source. Most of the energy is above 10 GHz and the current rise time is about 12 ps, which corresponds to the frequency content around 70 GHz – 80 GHz.

Discharge current waveforms can vary depending on the location of the contact point. In Figure 20 on page 33, the discharge point is in the middle of the die, at the corner, and at the middle of the edge. Here, the size of the die is 4 mm × 4 mm × 0.4 mm, and the potential difference is 10 V. The highest peak current and fastest rise time occur in the middle of the die, and the corner of the die has the most attenuated discharge current waveform. Similar results have been reported by earlier studies on CDM discharge testing with larger IC packages [13].

The series contact resistance is significant from the peak discharge current point of view, as shown in Figure 21. However, it has less effect on the rise time. With overdamped current pulses, the rise time is around 20 ps; even so, the decay time is measured in the nanoseconds regime.

D2D discharge current waveforms can be different with more complex die and interposer constructions if compared, for example, to the waveforms presented in Figure 18 and Figure 20. Figure 22 has discharge current waveforms based on Figure 4 and Figure 2 setup, where both dies or interposers have a leadframe, bondwire structures, micro vias, and μBGA connections. In this case, there is more inductance and parasitic capacitance along the discharge path.

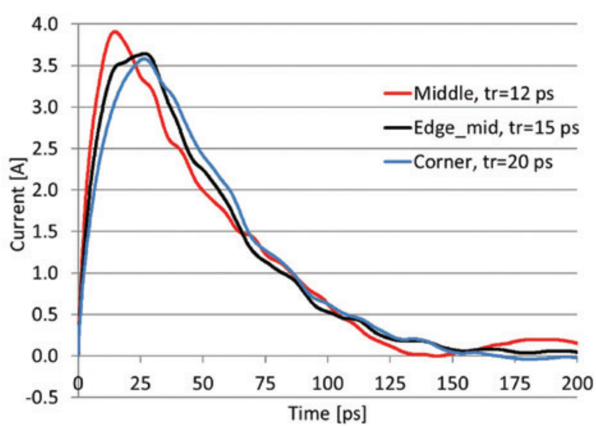


Figure 20: Comparison of D2D discharge current waveforms from the middle, corner, and middle of the edge of the die

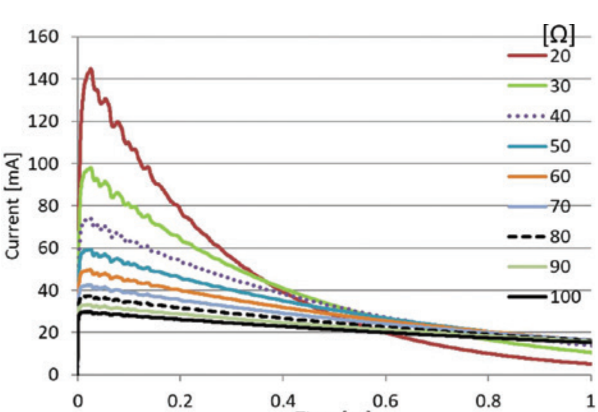


Figure 21: Discharge current waveform from 4 mm × 4 mm size die to the ground plane. With over 10 Ω resistance values, the discharge current waveform is overdamped.

Figure 22 presents the current at the transistor gate input area with four different contact resistance values. The waveform has two oscillating waveforms. At first, there is an initial fast pulse with about 150 mA peak current amplitude and multiple reflections originating from the leadframe structures close to the discharge point, as shown in Figure 23. This oscillation lasts about 150 ps. The main discharge current pulse with about 80 ps rise time follows from the rest of the structure and has the peak current amplitude of about 300 – 500 mA, depending on the value of the contact resistance.

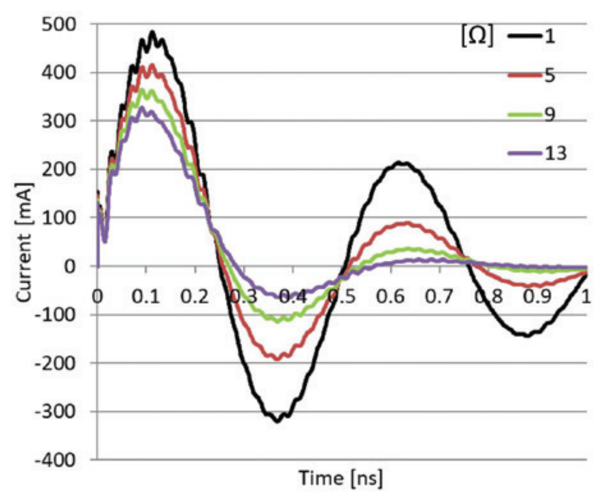


Figure 22: Discharge currents at the die gate input when a charged μBGAs discharges to a larger component. Contact series resistance as a variable.

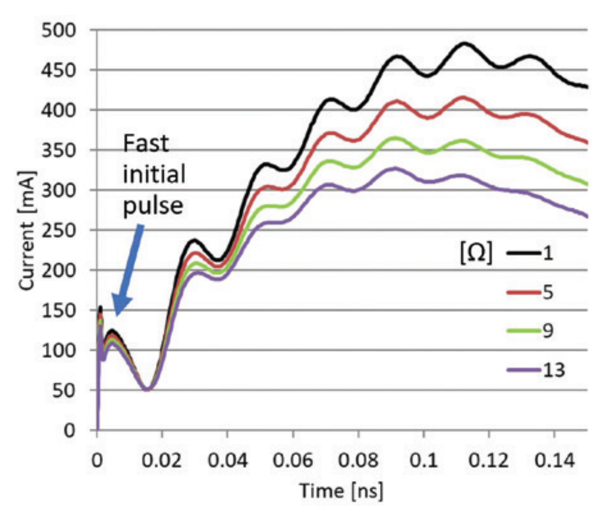


Figure 23: Initial 150 ps time period of the discharge current waveform shown in Figure 22

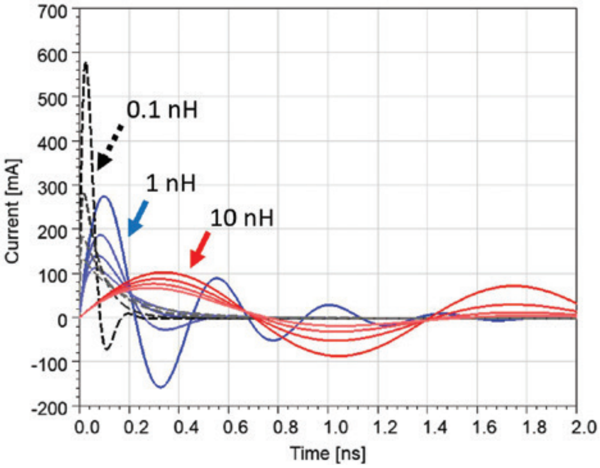


Figure 24: Calculated discharge current waveforms from 5 pF source with 0.1 nH, 1 nH, and 10 nH series inductance. Series resistance changes with each inductance value from 5 Ω to 35 Ω with 10 Ω steps.

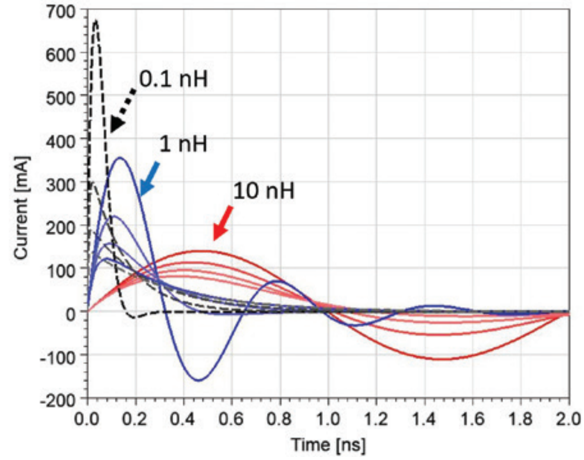


Figure 25: Calculated discharge current waveforms from 10 pF source with 0.1 nH, 1 nH, and 10 nH series inductance. Series resistance changes with each inductance from 5 Ω to 35 Ω with 10 Ω steps

As a summary:

- We can have both underdamped and overdamped discharge current pulses depending on the series contact resistance.
- Due to the low contact inductance, the rise time can be just tens of picoseconds.
- With overdamped pulses, the rise time can be around tens of picoseconds, even so the decay time of the current pulse is several nanoseconds.
- The rise time increases when the die or interposer has inductive structures, such as bondwires or a leadframe.
- Capacitive coupling and non-parallel surfaces affect both the rise time and peak current.
- The discharge current waveform can contain multiple waveforms with varying frequency content.

### *Discharge Current Analysis with Limited Measurement Setups*

D2D events do not necessarily resemble typical CDM discharges due to <20 V potential difference, faster current rise time, short pulse, and small total charge transfer. It is also challenging to measure discharge events with a low initial potential level, low source capacitance, and varying contact resistance. More challenges can arise from any additional parasitic series inductance, increasing the rise time. Based on calculations, the required measurement bandwidth can be > 20 GHz; thus, it can be difficult to measure current waveforms without changing the discharge scenario.

Figures 24 and 25 have calculations for discharge events where the series inductance, resistance, and capacitance are variables. Figure 24 has a fixed 5 pF source capacitance, and Figure 25 has a larger 10 pF source. Both figures have three discharge groups where the series inductance is set to 0.1 nH, 1 nH, and 10 nH. With each inductance value, the series resistance is 5 Ω, 15 Ω, 25 Ω, and 35 Ω. From both figures, we can see that the peak current depends more on the series resistance when the series inductance diminishes. Respectively, with larger inductance values, the series resistance has less effect on the peak current. In addition, both the series inductance and source capacitance affect the peak current, but the series resistance is the most sensitive discharge parameter from the peak current point of view, with low inductance D2D discharges.

Any additional parasitic inductance is critical if we try to measure D2D events with a measurement setup. There is typically additional inductance if we use a pogo pin to discharge a charged component. For example, a CDM tester has about 10 nH series inductance to fulfill the current waveform shape defined in calibration requirements [3]. To capture realistic discharge currents that represent D2D events, the measurement system should have less than 1 nH parasitic inductance. On the other hand, for verification measurement purposes, we could use a higher inductance value to compensate for possible variation with the contact resistance.

## DISCUSSION

With a higher expected D2D ESD stress, more silicon area would be required for die interface protection. This could become the limiting factor from the die or SoC design point of view due to the high number of protection circuits needed.

When considering the calculation results of this paper, it can be estimated that the potential difference during D2D assembly can be around 2 V – 10 V if dies have more than about 100 pC static charges after pickup. The resulting peak current can be over 1 A. For example, 10 V discharge potential would be at least one decade below a typical IC component CDM rating, but could still initiate a discharge event that can damage sensitive die interfaces with limited on-chip protection. This largely depends on how much static charge dies have, the physical construction of dies, and how the assembly setup has been realized. The effectiveness of ionization can also affect the final charge and voltage levels found in a real-life assembly environment.

One more open question is how to specify EPA control limits for D2D assembly processes. A voltage limit alone is not valid, as the measured electrostatic potential depends on the capacitance. Discharge current measurements are challenging, especially when done inside the process area. From our experience, it may require multiple attempts to capture the highest discharge current waveform from a charged die with less than 20 V initial potential in a laboratory environment. Here, the contact resistance plays a major role in changing the shape of the current waveform from pulse to pulse.

More challenges come from the die dimensions. Interconnections can have dense 25 µm – 400 µm pitch, making physical ESD testing difficult [2]. Discharge detection with antennas is also challenging due to weak discharge events from small-sized dies with a low initial potential difference. Die charge and potential measurement together would give good information for control purposes, but would require contacting the die with measurement probes inside the assembly equipment.

## CONCLUSION

D2D assembly is made with automated process tools where ESD risks are typically mitigated with ionization and by grounding conductors. However, D2D assembly can still have ESD events after a die charge during pickup and when it is placed on another die, interposer, or IC. Depending on the initial charge and contact resistance, these discharge events can have around 100 mA – 2 A peak current and current rise time from tens of picoseconds above 100 ps.

Based on this study, the contact resistance has a significant effect on the peak current of low-voltage discharges. Other affecting parameters are the initial source capacitance, charge of the die, capacitive coupling, location of the discharge, positioning, internal design of the die, and design of the reference die, IC, or interposer. D2D assembly setup can also alter the discharge current waveform. For example, changing the size or type of the pickup nozzle from conductor to dielectric changes the source capacitance, capacitive coupling, and discharge voltage during the assembly phase.

The required bandwidth to capture D2D discharges is typically more than about 20 GHz. This is due to the low series parasitic inductance in pH scale and source capacitances around ten picofarads. Simulation tools do not have strict bandwidth limitations, but practical D2D ESD current measurements can be challenging to carry out with a wide bandwidth. This also makes it challenging to directly compare measurement and simulation results.

There is no simple method to specify limits for D2D ESD control or for internal interfaces, as the die voltage or charge alone does not specify the discharge current waveform. Similarly, it is challenging to define one safe peak current or rise time limit for interconnection on-chip ESD designs. In addition, CDM tester current measurements may not correlate with real-life D2D discharge events due to different discharge scenarios. Finding a more suitable measurement method for D2D events requires more research.

## REFERENCES


1. L. Peters, "Enabling Test Strategies For 2.5D, 3D Stacked ICs," *Semiconductor Engineering*, September 8, 2022.
2. Z. Zhi Li, "Scaling Solder Micro-Bump Interconnect Down to 10 µm Pitch for Advanced 3D IC Packages," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), DOI: 10.1109/ECTC32696.2021.00082,
3. P. Tamminen, J. Smallwood, W. Stadler, "The Main Parameters Affecting Charged Device Discharge Waveforms in a CDM Qualification and Manufacturing," 2017 39th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), September 10-14, 2017.
4. D. Johnsson, P. Tamminen, H. Gossner, T. Viheriäkoski, "Peak Currents of Low CDM Die-to-Die Discharges," 2023 45th Annual EOS/ESD Symposium (EOS/ESD), October 2-4, 2023.
5. P. Tamminen, "Charge distribution and discharge current analysis with charged connector pins," *Electrostatics*, 2019.
6. T. Maloney, N. Jack, "CDM Tester Properties as Deduced from Waveforms," *IEEE Transactions on Device and Materials Reliability*, Volume 14, Issue 3, September 2014.
7. E. Hourdakis, B. J. Simonds, N. M. Zimmerman, "Submicron Gap Capacitor for Measurement of Breakdown Voltage in Air," Review of Scientific Instruments, Volume 77, Issue 034702, March 24, 2006.
8. A. Peschot, N. Bonifaci, O. Lesaint, "Deviations from the Paschen's Law at Short Gap Distances from 100 nm to 10 mm in Air and Nitrogen," *Applied Physics Letters*, 105, 123109, 2014.
9. R.H. Fowler, L. Nordheim, "Electron Emission in Intense Electric Fields," Proceedings of the Royal Society A, Volume 119, Issue 781, May 1, 1928.
10. I.A. Ivanov, I.G. Kiselev, S.V. Urushev, "The Transient Electric Resistance of Contacts Taking the Surface Roughness into Account," *Russian Electrical Engineering*, Volume 88, October 2017.
11. ASME B46.1-2019, *Surface Texture (Surface Roughness, Waviness, and Lay)*, American Society of Mechanical Engineers [ASME].
12. P. Tamminen, T. Viheriäkoski, "Characterization of ESD Risks in an Assembly Process by Using Component-Level CDM Withstand Voltage", 2007 29th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), September 16-21, 2007.
13. A. Jahanzeb, Y-Y. Lin, S. Marum, J. Schichl, C. Duvvury, "CDM Peak Current Variations and Impact Upon CDM Performance Thresholds," 2007 29th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), September 16-21, 2007.


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# RED'S CYBERSECURITY REQUIREMENTS UPDATE: EN 18031-X:2024

## Harmonized Standards and Related Thoughts

By Corey L. Sweeney, Jack Black, and Marilyn Sweeney

As a continuation of our article *Preparing for the EU's New RED Cybersecurity Requirements* from the June issue of *In Compliance* Magazine, this article will concentrate on the EN 18031-X series that was harmonized and published in the *Official Journal of the European Union* in January 2025, after our previous article was written.

Since our previous article covered the Radio Equipment Directive (Directive 2014/53/EU, known as the RED), plus other acts and directives referring to cybersecurity and why cybersecurity rules are necessary, we will not repeat them in this article.

### STANDARDS EN 18031-X:2024

*(Authors' Note: To make compliance easier for products that meet some or all of the requirements for ETSI EN 303 645, each of the three EN 18031-X standards shows a map of which of its requirements match specific ETSI EN 303 645 provisions (requirements).)*

The EN 18031-X series of standards was developed to provide manufacturers of radio equipment with a harmonized framework to meet the European Union's (EU's) cybersecurity requirements that became mandatory on August 1, 2025.

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Harmonized standards are a much easier way to go and are generally highly preferred. This series of standards combines the requirements for manufacturers and the requirements for testing laboratories into one standard, requiring less time to cross-reference documents when a better understanding of a requirement is needed.

The standard series is divided into three heavily overlapping standards, each of which has requirements consisting of an identifying code of three letters, a dash, and a number. For example, ACM-1 is the code for one of the requirements. EN 18031-1 has 31 requirements, EN 18031-2 has 40 requirements, and EN 18031-3 has 34 requirements.

Twenty-eight of the requirement codes are common to all three standards, making it appear that they are exactly the same. However, there are some differences in the text, and they do not necessarily all have the same section numbers, which can make the organization of the standards confusing. We will give examples of these differences later in this article.

To understand the organization of the standards better, it can help to know that they are divided into three parts to make it clear that they are covering 3(3)(d), 3(3)(e), and 3(3)(f) of the RED. More precisely:

- EN 18031–1 specifically addresses Article 3(3)(d), i.e., "radio equipment does not harm the network or its functioning nor misuse network resources, thereby causing an unacceptable degradation of service";
- EN 18031–2 specifically addresses Article 3(3)(e), i.e., "radio equipment incorporates safeguards to ensure that the personal data and privacy of the user and of the subscriber are protected";
- EN 18031–3 specifically addresses Article 3(3)(f), i.e., "radio equipment supports certain features ensuring protection from fraud".

So, the question is not "Which of these three standards applies to your product?" but rather "How many of the three standards apply to your product?"

## COMPLYING

### *Risk Assessment*

The answer to the above question will come from your product's risk assessment. As the EN 18031-X standards themselves state in Section A.2 Rationale:

> *"Whether one or multiple standards need to be applied to a specific radio equipment is a consideration that is made through a product-relevant risk assessment by the economic operator in order to identify threats and assess risks on the need to fulfil the essential requirements of the Radio Equipment Directive."*

Instead of thinking of the three standards as being organized to help with testing or organized to help with implementation of the standard during development, think of them as organized to help perform the mandatory risk assessment that manufacturers are responsible for performing.

Early in the required risk assessment, manufacturers need to determine which essential requirements of RED, as well as requirements in other Directives, apply to their product. A good reference to the application of the risk assessment can be found in the EU "Blue Guide" on the implementation of EU product rules (2022/C 247/01):

> *"Essential requirements must be applied as a function of the hazard inherent to a given product. Therefore, manufacturers have to carry out a risk analysis to first identify all possible risks that the product may pose and determine the essential requirements relevant for the product."*

So, to be clear, your company's risk assessment for each product should include a cybersecurity portion, as well as other portions, such as EMC and Safety.

While you may already be familiar with the safety portion of your risk assessment, you may be less familiar with the cybersecurity portion, which is a bit different. To read an explanation of cybersecurity risk assessment in the context of the RED (as well as the Cyber Security Act, and the Cyber Resilience Act), download the free Technical Report ETSI TR 103 935 at: https://www.etsi.org/deliver/etsi_tr/103900_103999/103935/01.01.01_60/tr_103935v010101p.pdf.

Since the EMC requirements have been active for much longer than the cybersecurity requirements, the guidance for the EMC portion of a risk assessment is more mature. Understanding risk assessment guidance in the context of something you already know can be potentially helpful. Guidance for the EMC portion of a risk assessment can be found in Technical Report ETSI TR 103 879. A free download can be obtained at: https://www.etsi.org/deliver/etsi_tr/103800_103899/103879/01.01.01_60/tr_103879v010101p.pdf.

After you begin your risk assessment by deciding which essential requirements of RED and other directives apply to your product, you will need to try to apply harmonized standards to your product. For RED 3(3)(d), 3(3)(e), and 3(3)(f), that will be the harmonized EN 18031-X standards.

Once it has been determined which EN 18031-X standard(s) apply to your product, each of the applicable standards provides details of its own part of the cybersecurity risk assessment for its associated RED essential requirement. Details can be found in each standard, starting with Section A.2.3, which is called "Threat modelling and security risk assessment."

EN 18031-X uses "STRIDE," which is a threat model to identify and enumerate specific types of possible threats to determine what important parts of your product need to be addressed. Additional details about STRIDE can be found at https://owasp.org/www-community/Threat_Modeling_Process#stride. Information on putting STRIDE into context can be found in Technical Report ETSI TR 103 935, section 8.4.2 (see previously provided link) in a section named "STRIDE."

### *EN 18031-1 "Part 1: Internet connected radio equipment"*

During the risk assessment, you will need to decide if EN 18031-1 applies to your product, which is simple for some products, but for other products, you'll need a definition of what counts as internet connected.

What follows is information that is currently available, in order of precedence:

- Directive 2014/53/EU 3(3)(d) basically states that the "goal" for EN 18031-1 is "radio equipment does not harm the network or its functioning nor misuse network resources, thereby causing an unacceptable degradation of service".
- Delegated regulation 2022/30 Article 1(1) says "The essential requirement set out in Article 3(3), point (d), of Directive 2014/53/EU shall apply to any radio equipment that can communicate itself over the internet, whether it communicates directly or via any other equipment."
- The EN 18031-X standards themselves introduce the phrasing "Internet connected radio equipment."

Although this partially clarifies the situation, it still leaves a lot of questions open. For example, "In the case of a Bluetooth device connected to a smartphone, to which devices does it apply and to which does it not apply?" The answer is not spelled out in the EN 18031-1 standard nor in the RED, probably because there is no simple answer. It can depend on factors, such as the intended use (including with what app it is intended to be used).

Not all cases lead to a consensus. This is understandable given the complexity and how new the requirement is. As the industry gains experience with these issues, it would be reasonable to expect a convergence toward consensus. This means in your product's risk analysis, you should probably add an "interpretation risk" for "internet connected" during the risk identification stage.

### *EN 18031-2 "Part 2: radio equipment processing data, namely Internet connected radio equipment, childcare radio equipment, toys radio equipment and wearable radio equipment"*

This is for "radio equipment processing personal data or traffic data or location data for either internet connected radio equipment, radio equipment designed or intended exclusively for childcare, toys, and wearable radio equipment."

To understand the intention of Part 2, several terms need to be defined:

- "Personal data" is defined as:

  *"any information relating to an identified or identifiable natural person ('data subject'); an identifiable natural person is one who can be identified, directly or indirectly, in particular by reference to an identifier such as a name, an identification number, location data, an online identifier or to one or more factors specific to the physical, physiological, genetic, mental, economic, cultural or social identity of that natural person;"* [1]

- "Traffic data" is defined as:

  *"any data processed for the purpose of the conveyance of a communication on an electronic communications network or for the billing thereof"* [2]

- "Location data" is defined as:

  *"any data processed in an electronic communications network, indicating the geographic position of the terminal equipment of a user of a publicly available electronic communications service;"* [3]

***EN 18031-3 "Part 3: Internet connected radio equipment processing virtual money or monetary value"***

This is for "internet connected radio equipment. That equipment enables the holder or user to transfer money, monetary value or virtual currency."

Virtual currency is defined as:

*"digital representation of value that is not issued or guaranteed by a central bank or a public authority, is not necessarily attached to a legally established currency and does not possess a legal status of a currency or money, but is accepted by natural or legal persons as a means of exchange, and which can be transferred, stored and traded electronically;"* [4]

## REQUIREMENTS – MECHANISMS

The EN 18031-X standards are made up of requirements that are grouped into categories called "mechanisms." Each mechanism has a 3-letter code, for example, "General Equipment Capabilities" is "GEC." The three-letter mechanism code becomes the first three letters of the five-character requirement code (e.g., GEC-1).

Table 1 shows which of the three standards has at least one requirement in each group (mechanism).

## REQUIREMENTS THAT ARE SIMILAR BUT NOT EXACTLY THE SAME IN ALL THREE STANDARDS

Although Parts 1, 2, and 3 of the EN 18031-X series each have their own specific requirements, 28 of the requirement codes show up in all three documents. The sections documenting the requirement code in

| Mechanisms | EN 18031-1 | EN 18031-2 | EN 18031-3 |
|---|---|---|---|
| ACM Access Control Mechanism | X | X | X |
| AUM Authentication Mechanism | X | X | X |
| SUM Secure Update Mechanism | X | X | X |
| SSM Secure Storage Mechanism | X | X | X |
| SCM Secure Communication Mechanism | X | X | X |
| RLM Resilience Mechanism | X | | |
| NMM Networking Monitoring Mechanism | X | | |
| TCM Traffic Control Mechanism | X | | |
| LGM Logging Mechanism | | X | X |
| DLM Deletion Mechanism | | X | |
| UNM User Notification Mechanism | | X | |
| CCK Confidential Cryptographic Keys | X | X | X |
| GEC General Equipment Capabilities | X | X | X |
| CRY Cryptography | X | X | X |

Table 1: Mechanisms (requirement groups) included in each standard

Although the ETSI EN 303 645 standard is available as a free download, there is no clear path at this time for freely using downloaded copies of the harmonized EN 18031-X:2024 standards Some progress has been made because of the "Malamud Case."

each standard have almost identical text with some minor changes that can potentially have large impacts.

To help you better understand these types of changes, some examples from requirement ACM-1 (Applicability of Access Control Mechanisms) are listed here:

- Wherever ACM-1 in EN 18031-1 mentions the word "network," EN 18031-2 mentions the word "privacy," and EN 18031-3 mentions the word "financial."
- ACM-1 in 18031-1:

  *"Do the physical or logical measures in the targeted operational environment limit to authorized entities?"*
- Whereas in ACM-1 in 18031-2 and 18031-3:

  *"Do the physical or logical measures in the targeted environment ensure that its accessibility is limited to authorized entities?"*
- ACM-1 in 18031-1 and 18031-3:

  *"The verdict FAIL for the assessment case is assigned if: **a** path through the decision tree documented in E.Info. DT.ACM-1 ends with 'FAIL' ..."*
- Whereas in ACM-1 in 18031-2:

  *"The verdict FAIL for the assessment case is assigned if: **all** path through the decision tree documented in E.Info. DT.ACM-1 ends with 'FAIL' ..."*
- ACM-1 in 18031-2 and 18032-3, but not in 18031-1:

  *"If the equipment relies on the access control given by the intended operational environment, it is to be ensured that this access control is appropriate as described in ACM-2."*
- ACM-1 18031-2 but not in 18031-1 or 18032-3:

  *"In general, full public accessibility to privacy assets cannot be considered as a reasonable intended equipment functionality, especially concerning children's privacy and childcare. However, specific scenarios involving public accessibility to privacy assets may be considered as intended equipment functionality if part of clearly advertised functionality or is communicated (to non-child users) via UNM."*

So be sure to check the requirements in each of the three standards, even though they may appear to be the same.

## RESTRICTIONS

When EN 18031-X was harmonized, restrictions were added, a full list of which can be found in OJ L, 2025/138 - 30/01/2025.[5] Here's an example of the importance of being aware of all restrictions that apply to these standards. In the Authentication category, AUM-5-1 *Requirement for factory default passwords* referenced in all three standards includes the line: "NOTE: The user can choose to not use any password."

However, in the Restrictions, it says:

*"Clauses 6.2.5.1 and 6.2.5.2 of harmonized standards EN 18031-1:2024, EN 18031-2:2024 and EN 18031-3:2024 deal with default passwords. Those clauses offer manufacturers the possibility to allow a user not to set or use any password. It is considered that, if this option is implemented, the relevant authentication risks will not be properly addressed and therefore conformity with the essential requirements set out in Article 3(3), first subparagraph points (d), (e) and (f), of Directive 2014/53/EU would not be ensured."*

## OBTAINING THE EN 18031-X:2024 STANDARDS

Although the ETSI EN 303 645 standard is available as a free download, there is no clear path at this time for freely using downloaded copies of the harmonized EN 18031-X:2024 standards. Some progress has been made because of the "Malamud Case," so EN citizens may want to search for the "Malamud Case" to see if their country's standards organization has made progress on making some form of free access available.

Be aware that IEC/ISO 18031 is not the same as EN 18031-1, -2, and -3. While IEC/ISO 18031 is the same number and is also on the topic of cybersecurity, it is not the same type of standard, as it is specifically focused on random number generators.

Otherwise, the EN 18031-X standards can be purchased. And yes, we realize the irony in how many people will end up lowering the security of their computers by installing "FileOpen" just to be able to download and read a security standard. ("FileOpen" appears to be a DRM binary without a reproducible build process or auditable source and requires other binaries without reproducible build process or auditable source preinstalled, and prevents you from reading them from a secure system with access to the internet blocked.)

We are not providing a link to EN 18031-X:2024 as there is no single source for the standards since they are distributed through the standards organizations of the various EU countries.

## A WORD OF CAUTION

Be aware that IEC/ISO 18031 is not the same as EN 18031-1, -2, and -3. While IEC/ISO 18031 is the same number and is also on the topic of cybersecurity, it is not the same type of standard, as it is specifically focused on random number generators. IEC/ISO 18031 is actually mentioned in the EN 18031-X series when discussing random number generation.

## CONCLUSION

The world of cybersecurity is relatively new and rapidly changing. Meeting its regulations can feel complex and overwhelming, so you may want to contact your test lab for assistance. Cybersecurity updates can be found at http://www.dlsemc.com/cybersecurity-red.

## REFERENCES

1. https://eur-lex.europa.eu/eli/reg/2016/679/oj/eng, Article 4(1)
2. https://eur-lex.europa.eu/eli/dir/2002/58/oj/eng, Article 2(b)
3. https://eur-lex.europa.eu/eli/dir/2002/58/oj/eng, Article 2(c)
4. https://eur-lex.europa.eu/eli/dir/2019/713/oj/eng, Article 2 (d)
5. https://ec.europa.eu/docsroom/documents/64474/attachments/1/translations/en/renditions/native

# SHIELDING TO PREVENT RADIATION

## Part 4A: Far-Field Shielding Effectiveness of Solid Conducting Shield – Approximate Solutions

By Bogdan Adamczyk

This is the first part of the fourth installment in a series devoted to the topic of shielding to prevent electromagnetic wave radiation. The first article [1] discussed reflection and transmission of uniform plane waves at a normal boundary. The second article, [2], addressed normal incidence of a uniform plane wave on a solid conducting shield with no apertures. The third article, [3], presented the exact solution for shielding effectiveness of a solid conducting shield. In this article, two approximate, yet accurate, solutions are obtained from the exact solution.

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### SHIELDING EFFECTIVENESS – APPROXIMATE SOLUTION – VERSION 1

The approximate solution for the shielding effectiveness is obtained from the exact solution of the previous article, [3]:

$$\left|\frac{\hat{E}_i}{\hat{E}_t}\right| = \left|\frac{\left(\eta_0+\hat{\eta}\right)^2}{4\eta_0\hat{\eta}}(\Delta)e^{-\frac{t}{\delta}}e^{-j\beta t}e^{-j\beta_0 t}\right| \tag{1a}$$

where

$$\Delta = e^{\frac{t}{\delta}}e^{j\beta t}e^{-j\beta_0 t} - \left(\frac{\eta_0-\hat{\eta}}{\eta_0+\hat{\eta}}\right)^2 \tag{1b}$$

Let's investigate the consequence of the assumption that the shield is made of a good conductor. Intrinsic impedance of a good conductor, at the frequencies of interest, is much smaller than the intrinsic impedance of free space. That is $|\hat{\eta}| \ll \eta_0$. (For instance, the magnitude of the intrinsic impedance of copper at 1 MHz is $3.69 \times 10^{-4} \ll 377\ \Omega$).

It follows,

$$\hat{\eta} \ll \eta_0 \quad \Rightarrow \quad \frac{\eta_0-\hat{\eta}}{\eta_0+\hat{\eta}} \cong 1 \tag{2}$$

If the shield is thick, $t \ll \delta$, then we have

$$t \gg \delta \quad \Rightarrow \quad e^{-\frac{t}{\delta}} \ll 1 \tag{3}$$

and the right-hand side of Eq. (1) can be approximated by

$$\left|\frac{\hat{E}_i}{\hat{E}_t}\right| \cong \left|\frac{\left(\eta_0+\hat{\eta}\right)^2}{4\eta_0\hat{\eta}}\left[e^{\frac{t}{\delta}}e^{j\beta t}e^{-j\beta_0 t}\right]\right| \tag{4}$$

or

$$\left|\frac{\hat{E}_i}{\hat{E}_t}\right| \cong \left|\frac{\left(\eta_0+\hat{\eta}\right)^2}{4\eta_0\hat{\eta}}\right| e^{\frac{t}{\delta}} \tag{5}$$

Furthermore, for a good conductor, we have

$$\hat{\eta} \ll \eta_0 \quad \Rightarrow \quad \left|\left(\eta_0 + \hat{\eta}\right)^2\right| \cong |\eta_0^2| \tag{6}$$

and Eq. (5) simplifies to

$$\left|\frac{\hat{E}_i}{\hat{E}_t}\right| \cong \left|\frac{\eta_0}{4\hat{\eta}}\right| e^{\frac{t}{\delta}} \tag{7}$$

This is the approximate solution for a *good and thick conductor in far field*. In dB, this solution becomes

$$SE_{dB} = 20\log_{10}\left|\frac{\hat{E}_i}{\hat{E}_t}\right| \cong \underbrace{20\log_{10}\left|\frac{\eta_0}{4\hat{\eta}}\right|}_{R_{dB}} + \underbrace{20\log_{10} e^{\frac{t}{\delta}}}_{A_{dB}} \tag{8}$$

or

$$SE_{dB} = R_{dB} + A_{dB} \tag{9}$$

where

$$R_{dB} = 20\log_{10}\left|\frac{\eta_0}{4\hat{\eta}}\right| \tag{10}$$

$$A_{dB} = 20\log_{10} e^{\frac{t}{\delta}} \tag{11}$$

Note that the approximate reflection loss is different from the exact reflection loss, (Eq. (49) in [3]) while the absorption loss is the same as in the exact solution. Also note that the multiple-reflection loss is not present in Eq. (8), which means that for a good and thick conductor in far field, it can be ignored.

## SHIELDING EFFECTIVENESS – APPROXIMATE SOLUTION

The approximate solution for the reflection loss given by Eq. (12) and the exact solution for the absorption loss given by Eq. (11) can be expressed in more practical forms. To derive these alternative forms, we need some parameter relationships. Recall the expressions defining the propagation constant and the intrinsic impedance (Equations (6) and (7) in [2]).

$$\hat{\gamma} = \sqrt{j\omega\mu(\sigma + j\omega\epsilon)} \tag{12}$$

$$\hat{\eta} = \sqrt{\frac{j\omega\mu}{\sigma + j\omega\epsilon}} \tag{13}$$

Thus,

$$\hat{\gamma}\hat{\eta} = \sqrt{j\omega\mu(\sigma + j\omega\epsilon)}\sqrt{\frac{j\omega\mu}{\sigma + j\omega\epsilon}} = j\omega\mu \tag{14}$$

or

$$\hat{\eta} = \frac{j\omega\mu}{\hat{\gamma}} \tag{15}$$

We will return to this equation shortly.

The propagation constant in Eq. (12) can be expressed as

$$\hat{\gamma} = \sqrt{j\omega\mu\sigma\left(1 + j\frac{\omega\epsilon}{\sigma}\right)} \qquad (16)$$

For good conductors, [4],

$$\frac{\sigma}{\omega\epsilon} \gg 1 \quad \Rightarrow \quad \frac{\omega\epsilon}{\sigma} \ll 1 \qquad (17)$$

Thus, the propagation constant in Eq. (16) can be approximated by

$$\hat{\gamma} = \sqrt{j\omega\mu\sigma} = \sqrt{\omega\mu\sigma}\angle 45° \qquad (18)$$

Using this result in Eq. (15), we get

$$\hat{\eta} = \frac{\omega\mu\angle 90°}{\sqrt{\omega\mu\sigma}\angle 45°} \qquad (19)$$

or

$$\hat{\eta} = \sqrt{\frac{\omega\mu}{\sigma}}\angle 45° \qquad (20)$$

and thus

$$|\hat{\eta}| = \sqrt{\frac{\omega\mu}{\sigma}} = \sqrt{\frac{2\pi f\mu}{\sigma}} \qquad (21)$$

Absolute permeability can be expressed in terms of relative permeability (with respect to free space) as

$$\mu = \mu_r\mu_0 = \mu_r \times 4\pi \times 10^{-7} \qquad (22)$$

Absolute conductivity can be expressed in terms of relative conductivity (with respect to copper) as

$$\sigma = \sigma_r\sigma_{Cu} = \sigma_r \times 5.8 \times 10^{7} \qquad (23)$$

Using Equations (22) and (23) in Eq. (21) we have

$$\left|\hat{\eta}\right| = \sqrt{\frac{2\pi f\mu_r(4\pi\times 10^{-7})}{\sigma_r(5.8\times 10^{7})}} = \sqrt{\frac{8\pi^2 f\mu_r}{\sigma_r(5.8\times 10^{14})}} \qquad (24)$$

In the second part of this installment, we will utilize the above parameter relationships and present a more practical solution for the far field shielding effectiveness of a solid conducting shield.

## REFERENCES

1. Bogdan Adamczyk, "Shielding to Prevent Radiation – Part 1: Uniform Plane Wave Reflection and Transmission at a Normal Boundary," *In Compliance Magazine*, June 2025.
2. Bogdan Adamczyk, "Shielding to Prevent Radiation – Part 2: Uniform Plane Wave Normal Incidence on a Conducting Shield," *In Compliance Magazine*, July 2025.
3. Bogdan Adamczyk, "Shielding to Prevent Radiation – Part 3: Far-Field Shielding Effectiveness of a Solid Conducting Shield – Exact Solution," *In Compliance Magazine*, August 2025.
4. Bogdan Adamczyk, *Principles of Electromagnetic Compatibility – Laboratory Exercises and Lectures*, Wiley, 2023.

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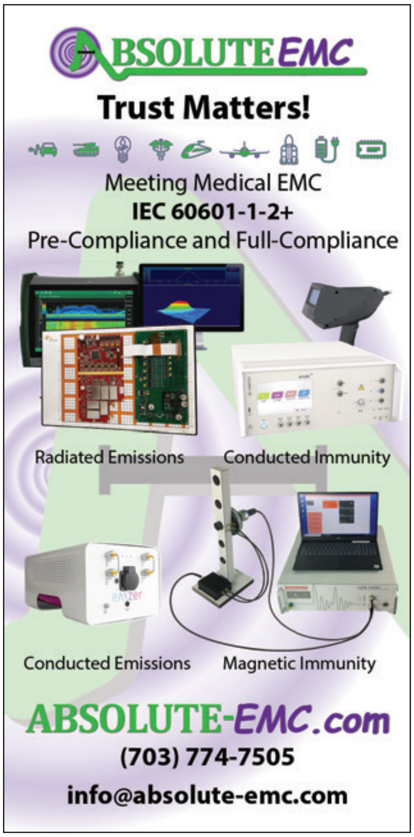






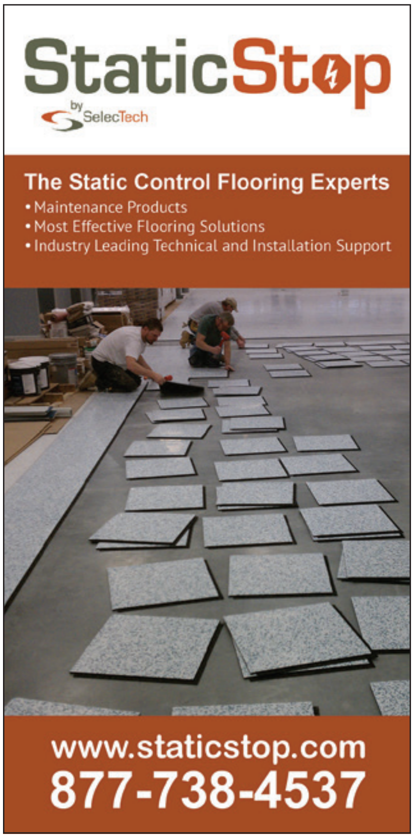

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