SEPTEMBER 2024

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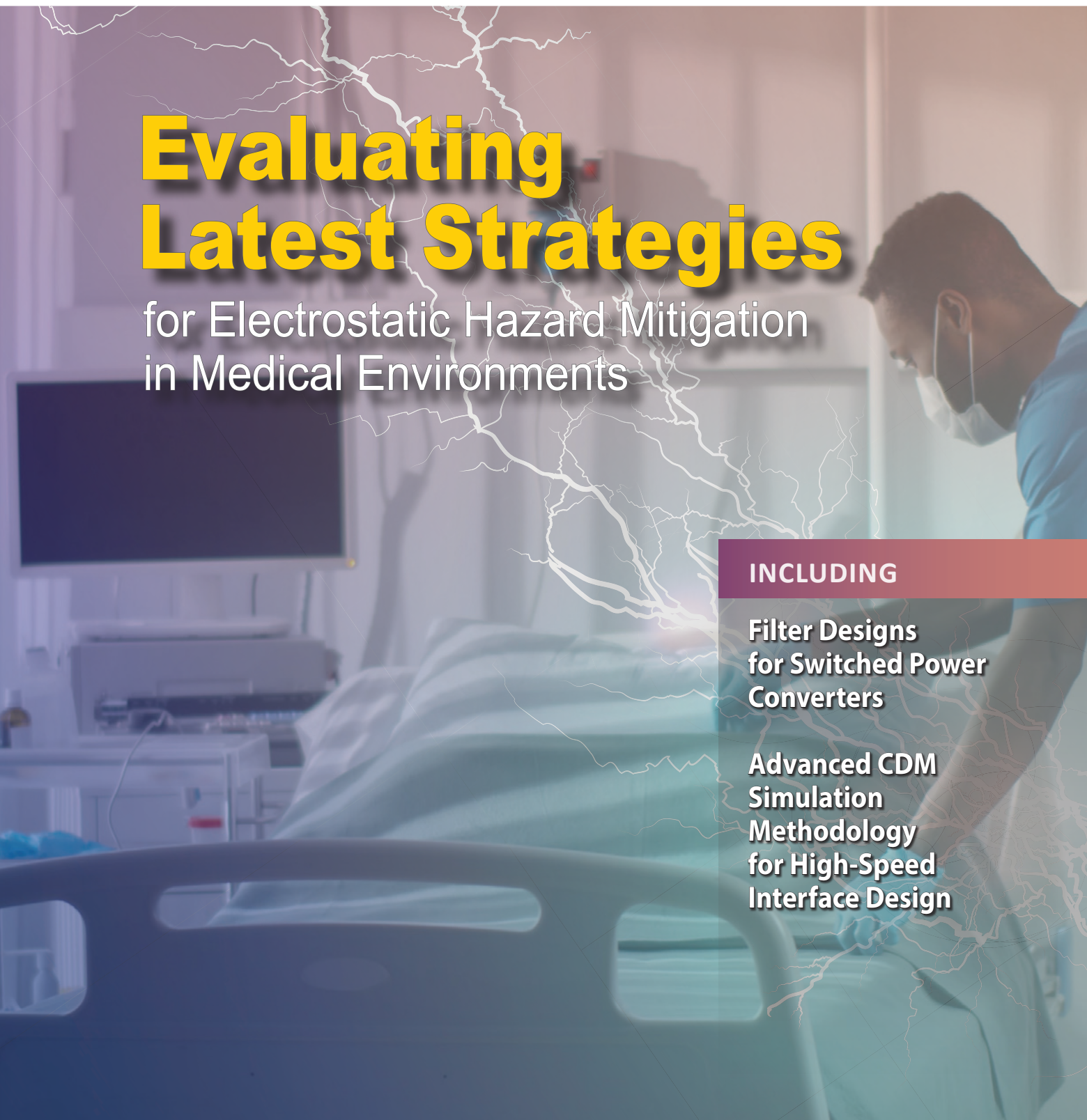

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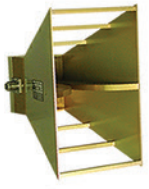

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FEATURE ARTICLES

SPECIAL COVERAGE

COLUMNS

DEPARTMENTS

Milestones

Manuel Sierra Castañer Awarded AMTA Honor

The Antenna Measurement Techniques Association (AMTA) has given its Distinguished Achievement Award to Professor Manuel Sierra Castañer. A professor at the Universidad Politécnica de Madrid, Castañer directs the school's Antenna Measurement Laboratory, one of the few university laboratories with ISO 17025 certification, and has been actively involved in the characterization of antennas and systems for satellite applications and space missions organized by the European Space Agency.

Peter Collins Receives AMTA Life Membership Award

The Antenna Measurement Techniques Association (AMTA) has recognized its long-time contributor and supporter, Dr. Peter Collins, with the organization's Joe Pape Honorary Life Membership Award. The Joe Pape Award is given to individuals who are widely recognized for their contributions to the electromagnetic community and who have had a direct impact on the work of AMTA.

Andrew Drozd Reappointed to FCC Advisory Council

Dr. Andrew Drozd, President and CEO of ANDRO Computational Solutions, has been reappointed to the Communications Security, Reliability, and Interoperability Council IX (CSRIC IX) of the U.S. Federal Communications Commission (FCC). The Council advises the Commission on communications considerations related to public safety and homeland security networks. Drozd, who leads efforts at ANDRO to explore the use artificial intelligence technologies to secure wireless communications, will serve on the Council for a two-year term, ending in May 2026.

Absolute EMC and Lightning EMC Merge

Absolute EMC and Lightning EMC have announced the merger of their two companies. Absolute EMC specializes in EMC testing knowledge and equipment. The company will continue operations under the name Absolute EMC.

StaticWorx Makes Inc. 5000 for Fifth Time

StaticWorx has been named to Inc. Magazine's 2024 Inc. 5000 list of the 5000 fastest-growing private companies in the U.S. As a fifth-time honoree, StaticWorx has now been placed on the Inc. 5000 honor roll and has taken its place among the 4% of honorees who have made the list five times.

UL Solutions NA Opens Advance Battery Laboratory

UL Solutions North America has opened its new advanced battery laboratory. It is located in the Oakland Technology Park complex in Auburn Hills, MI, near Detroit, MI, one of the largest automotive technology development and production centers in the world.

Insights

Researchers Develop Framework for the Design of Quantum Sensors

Researchers at North Carolina State University and the Massachusetts Institute of Technology have reportedly developed a protocol for the design of quantum sensors that would allow sensor designers to maximize their power and performance. The researchers designed an algorithmic framework that couples quantum bits (the counterpart to computing bits) with a bosonic oscillator, allowing designers to manipulate the coupling between the components to more precisely tune the sensor for its intended use. The researchers' findings were published in the journal *Quantum*.

China Court Halts Sale of Patent-Infringing Products

China-based company Itech Electronics has been found in violation of China's patent infringement laws in connection with its manufacturing and sale of resistor devices. The company reportedly manufactured and sold devices that infringed on an invention patent issued by the Peoples Republic of China and held by U.S.-based ChromaATE for "Resistor Device and Manufacturing Method Thereof." The court ruling orders Itech to immediately cease manufacturing, selling, or offering for sale specific products that infringe on ChromaATE's invention patent rights, and to destroy any infringing products in their inventory.

Products

EMITE's over-the-air chambers now integrate with Rohde & Schwarz's R&S CMX500 tester. This combination supports testing for LTE, 5G NR (FR1 up to 8 GHz, FR2 up to 50 GHz), 5G RedCap, and Wi-Fi 7. The partnership aims to provide comprehensive testing for current and future wireless technologies, with plans to include NB-IoT NTN and NR NTN capabilities.

Integra Optics has launched a new 10G SFP+ transceiver with a 120 km reach. This innovative product supports 10 Gbps data rates over single-mode fiber for Metro Ethernet transport and access networks without requiring amplification. The transceiver complies with industry-standard SFP+ MSA for broad compatibility and operates efficiently in commercial temperature ranges.

ITG Electronics has introduced the PFC433835B Series, a new line of power factor correction chokes designed for high switching frequencies up to 200KHz. These compact, cubic-designed chokes handle up to 3,300 Watts and offer inductance ranges from 90-285uH. Featuring flat wire and square core construction, they are up to 50% smaller than traditional toroidal PFC chokes and can reduce DC resistance by 40%. Suitable for AC to DC conversion in various applications, these chokes can handle up to 50 Amp with 50% roll off, addressing industry needs for higher power density in compact designs.

Pasternack has launched a new series of high-power RF terminations. These products offer power ratings of 5, 10, and 50 watts, suitable for various high-frequency applications in telecommunications, broadcasting, and satellite communications. The terminations are designed for reliable signal termination in demanding environments.

Rohde & Schwarz has introduced gASIC-based zone triggering in their new MXO series oscilloscopes. This industry-first feature allows for precise event isolation that traditional triggers struggle with. Zone triggering enables users to define trigger conditions by drawing areas on the display, proving effective for complex scenarios where conventional triggers fall short. This approach works on analog channel signals, math, and spectrum, making it a versatile solution for various challenging measurement tasks.

Saelig introduced Siglent SPD4000X Series 4-channel Programmable DC Power Supplies. Available in 240W, 285W, and 400W models, they offer 1mV/1mA resolution. Two channels can be combined for higher output. Features include 4-wire remote sensing, 5-digit voltage/current display, and a 4.3" color screen.

SCHURTER has expanded its 400 VDC connector family, now offering a complete IEC TS 62735-compliant solution from network to device. Building on the 2019 launch of GP21 and GS21 connectors, SCHURTER introduces new device-side models: GC21, GH21, and GI21. The GI21 is for DC operation, while GH21 is a hybrid AC/DC version. A new cord retention system enhances safety. All new products are made from bio-based plastic, emphasizing SCHURTER's commitment to sustainability in this innovative DC connector line.

TDK launched a new ACT1210E Series common mode filter for 10BASE-T1S automotive Ethernet. The ACT1210E-131-2P-TL00 offers 30% lower line-to-line capacitance, achieving OPEN Alliance EMC test Class IV status. It features 130 µH common mode inductance at 100 kHz and 70 mA rated current.

Würth Elektronik introduced the WE-MXGI power inductor, featuring extremely low core losses and the lowest winding resistance in its class. This compact, magnetically shielded SMT inductor is designed for high-frequency DC/DC converters using GaN and SiC technologies, enabling more efficient and compact designs with higher power capabilities.

Upcoming Events

September 2-5
EMC Europe Symposium

September 11-13
Fundamentals of Product Safety

September 12
Space Applications, EMC, ENV

September 15-19
★46th Annual EOS/ESD Symposium and Exhibits

September 19
★2024 Minnesota EMC Event

September 22-27
European Microwave Week 2024

September 24-27
Applying Practical EMI Design and Troubleshooting Techniques

October 2-4
Battery Japan

October 7-9
EMC COMPO 2024

October 7-10
★The Battery Show

October 10
Cyber-Security Webinar

October 15
★2024 San Diego Test Equipment Symposium

October 22-25
Applying Practical EMI Design and Troubleshooting Techniques

October 27-November 1
★46th Annual Meeting and Symposium of the Antenna Measurement Techniques Association

October 28-October 31
Military Standard 810 (MIL-STD-810) Test Training

★ Visit In Compliance's booth at these events!

New Mobile Speed Test Application from the FCC

The U.S. Federal Communications Commission (FCC) has released a new version of its smart device application that enables users to evaluate the speed of their mobile broadband connection.

The FCC's updated Mobile Speed Test application includes new features, including a "repeat test" functionality that allows users to conduct repeated tests without having to reenter and certify their information before each individual test, and an in-app map that displays the location where an individual test was performed.

The revised Mobile Speed Test app also allows users to log in to the National Broadband Map to review their speed test results in context. The Mobile Speed Test app is part of the FCC's Broadband Data Collection program to continually evaluate the characteristics of our national broadband service capability, as well as actual broadband performance in residential consumer markets.

FCC Issues Proposed Rules for AI-Generated Political Advertising

The U.S. Federal Communications Commission (FCC) has proposed requirements intended to increase transparency in the use of artificial intelligence (AI) technologies in the creation of political advertising on television and radio.

According to Notice of Proposed Rulemaking (NPRM), the FCC would require those who must file information with the agency about television and radio political advertising to specify whether AI technologies were used in the generation of such content and, if so, to disclose the use of AI in the advertisements.

The FCC says that it's proposed rulemaking follows growing concerns among the American electorate that misleading AI-generated content will have an undue influence on the outcome of the 2024 U.S. presidential election, and cited specific recent examples of the use of AI-generated voices and images in misleading political advertising.

IEEE's FDA-Recognized Cybersecurity Standards See First Certifications

The IEEE's new certification program for medical device cybersecurity is off and running!

The IEEE Standards Association announced that several testing facilities operated by atsec Information Security have been officially recognized to conduct testing in accordance with the requirements of the IEEE's Medical Device Cybersecurity Certification Program. The atsec facilities that have received IEEE recognition under the Program are located in Sweden, Germany, and the United States.

In addition, the IEEE says that the first medical devices have now been reviewed and certified in accordance with the requirements of the IEEE 2621 series of standards, which have been recognized by the U.S. Food and Drug Administration (FDA) and which serve as the basis for the IEEE's cybersecurity certification.

Auto Industry Awaits New Safety Spectrum Rules

The U.S. Federal Communications Commission (FCC) is set to vote on final rules to integrate advanced communications technologies into intelligent transportation systems (ITS).

According to a press release issued by the Commission, the new rules would allow in-vehicle and roadside units to operate cellular-vehicle-to-everything (C-V2X) technology in the 5.9 GHz spectrum. C-V2X technology supports "direct communications between vehicles, roadside infrastructure, and other road users…to facilitate… non-line-of-sight awareness, notice of changing driving conditions, and automated driving."

The new rules would also codify C-V2X technical parameters, including power and emission limits, and prioritize safety-of-life communications. Finally, the rules would set a two-year timeline for phasing out the use of dedicated short-range communications (DSRC-based technologies.

Making Plastic Waste Into Polymers for Electronic Devices? Who Knew

Sometimes, it takes time and patience to develop solutions to hard problems. But thankfully, dedicated scientists and researchers are never deterred when facing challenges. Instead, challenges energize them, frequently producing some amazing outcomes.

The latest example of this comes courtesy of a group of researchers at the University of Delaware and the Argonne National Laboratory, who have discovered a chemical process that can convert Styrofoam and other types of plastic waste into a valuable conducting polymer material that can then be used in electronic devices.

According to a paper published in the Journal of the American Chemical Society (ACS), the joint research team started with evaluating whether PEDOT:PSS, a polymer that has electronic and ionic conductivity could be synthesized from plastic waste. Specifically, they explored the sulfonation of plastic waste made from polystyrene, which is used in many types of containers and packaging materials.

A group of researchers has discovered a chemical process that can convert Styrofoam and other types of plastic waste into a valuable conducting polymer material.

After extensive experimentation and testing over several months, the researchers ultimately determined the specific solvents, the molar ratios of sulfonating agents, and the temperatures needed to achieve the highest possible polymer sulfonation of polystyrene samples. They then compared the resulting waste-derived material compared with conventional PEDOT:PSS and found comparable performance.

In addition, the researchers also found that their process minimized the amount of waste generated during the conversion process, resulting in a win-win outcome!

EMC BENCH NOTES

Some Starting Tools

By Kenneth Wyatt

As a product designer, one of the biggest issues you'll face is radiated emissions. This month, we'll describe the minimal set of tools to characterize and help mitigate radiated emissions right on your workbench.

NEAR FIELD PROBES

Most designers may be familiar with near field probes but may not understand how to go from using them to identify "hot spots" of high harmonic energy within your board or system to actually mitigating the issues.

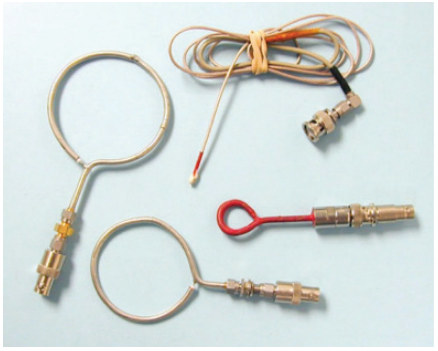

Figure 1: Some DIY H-field probes. The smaller one may require a broadband preamplifier to observe usable harmonics.

Figure 2: A variety of commercial H-field probes. Rohde & Schwarz, Com-Power, Tekbox and Beehive Electronics (top to bottom).

These can either be constructed as DIY projects or commercial probe kits may be purchased. Flexible or semi-rigid coaxial cables may be used. H-field (loop) probes may be constructed by soldering the center conductor to the shield, as in Figure 1. An E-field probe may be constructed by cutting away a short (5mm) portion of the shield, exposing the center conductor. Both types of DIY probes should be dipped in rubberized "tool dip" or otherwise insulated to avoid shorting out circuitry. See the example in red.

More details for commercial product choices can be found in Reference 1 at all price points. Each month, we'll be using this basic equipment for some hands-on experiments we can do together.

Let's start off with the most basic probe; E-field (voltage measurement) and H-field probes (current measurement). These are designed to be most sensitive to either E-fields or H-fields, respectively.

H-field probes are most sensitive to currents in wires or cables. While these DIY versions have an unbalanced geometry, which creates common mode currents flowing up the "handle" portion, they are still useful for general troubleshooting.

E-field probes are more sensitive to components that create large E-fields, such as heat sinks and any circuit switching large voltages. A good example of large changing voltages would be off-line switching power converters.

The advantage to commercial near field probes is that they are insulated and, being longer and thinner, can penetrate into narrow spaces (Figure 2). Commercial probes come as sets, usually three H-field probes in different sizes and an E-field probe. Beehive Electronics and Tekbox probe sets are about $350. Make sure to order the cable (sold separately) for the Beehive probes.

Com-Power probe sets include a capacitive-couple probe that can directly measure harmonic voltages on circuit traces and can also be used to inject signals useful for troubleshooting immunity issues. The Rohde & Schwarz probe set is unique in that, in addition to the usual H- and E-field probes, they also include some very tiny probes that may be more useful in today's small wearable products.

Near field probes are most useful for identifying major energy sources on PC boards and internal cables. I use H-field probes for detecting high currents (as in ICs and circuit traces) and E-field probes for detecting high voltage swings (as in buck converters). A record of the harmonic spectrum for each major energy source should be recorded.

RF CURRENT PROBES

The reason most products fail radiated emissions is that their attached cables carry high-frequency harmonic currents, which tend to make them radiate as transmitting antennas. Note that it takes only 6 to 8 µA of high-frequency harmonic currents to exceed the FCC or EU limit for Class B (household) products!

By measuring and monitoring these RF currents, we can often perform troubleshooting right on our workbenches and mitigate emissions prior to taking the product to the compliance test lab. Reducing these RF currents will also reduce the cable emissions.

While I personally own several commercial current probes, those pictured in Figure 3 are the ones I started out with for a couple of years before I could afford a good set. Many of my clients are helped remotely, and I've had them make these DIY probes so I can guide their troubleshooting efforts.

Choose a ferrite that has some impedance in the frequency range of most common mode currents: 30 to 200 MHz. A Fair-Rite choke made from type 31 material, or equivalent, should work well. The number of turns is not critical, and I usually use 5 to 7 turns. Terminate with the desired coaxial connector epoxied in place. Be aware the hinge on these DIY current probes won't last forever, so be prepared to replace them occasionally.

The fact these DIY probes are uncalibrated is unimportant when used for troubleshooting purposes since we're only looking for relative changes. For example, if we know we're failing by 5 dB, then at the workbench, we'll want to apply mitigations to reduce the harmonic amplitude by 10 to 15 dB for safety.

Eventually, you'll want to purchase a calibrated RF current probe. Figure 4 shows an affordable commercial probe from Com-Power. Similar affordable probes are available from Tekbox. Be sure to order one that can clamp around the wire or cable to be tested.

As for the near field probes, you'll want to record the harmonic frequency spectrum for each cable attached to your product. By examining the cable currents, you should find some correlation to the energy source or sources on the board or interior cables. Part of the mitigation process will be to identify and reduce the coupling between the dominant energy sources and radiating cables.

NEARBY ANTENNA

Once your product is characterized using the near field and current probes, I usually switch to a nearby antenna placed about 1m from the product under test. The resonant frequency doesn't matter much so long as you can observe the harmonics from the EUT. Monitoring the actual emissions while troubleshooting and applying mitigations in real-time is a very efficient way to resolve design problems.

The antenna I like to use is made by Kent Electronics and costs just $38. I show how to make the PVC fixture that attaches to a table-top tripod in Reference 2.

SPECTRUM ANALYZERS

In recent years, the cost of spectrum analyzers has dropped to very affordable levels. I started my career with a Rigol DSA815TG, which was about $1,500 at the time. Since then, this price has dropped to about $1,000. I'm currently using the Siglent SSA 3032X, with its larger screen. If you're in the market for one of these, be sure to order the tracking generator and EMI options, as we'll be using these for more advanced EMC characterizations.

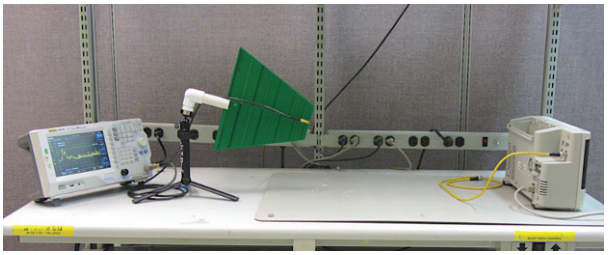

Figure 5: Monitoring the emissions from the product under test with a spectrum analyzer and simple antenna is a very efficient method for fixing problem harmonics.

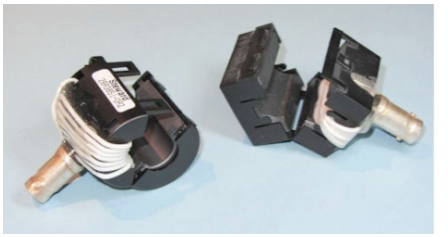

Figure 3: A couple of DIY RF current probes made from standard clamp-on ferrite chokes.

Figure 4: An example of a commercial RF current probe that is calibrated from 10 kHz to 400 MHz. Photo, courtesy Com-Power.

There are several other good choices in analyzers, and Rigol and Siglent have captured much of the affordables market. Many other alternatives are described in Reference 1. The U.S. distributor for these models is Saelig Electronics.

SUMMARY

This summarizes the most basic equipment needed for identifying the major harmonic noise sources and for characterizing radiated emissions. Next month, we'll use these tools to help characterize some actual embedded processors and suggest some mitigations that would improve the designs.

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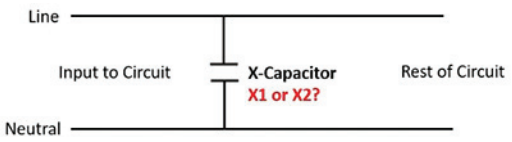
2. Wyatt, "PC Board Log Periodic Antennas," *EDN*.

PRACTICAL ENGINEERING

X1 vs X2 Capacitor Types: How to Select the Correct Type

By Don MacArthur

X-type capacitors suppress differential mode conducted emissions in applications such as switch-mode power supplies, DC-DC converters, variable-speed motor drives, and other similar devices. The X designation means they are applied line-to-neutral, as shown in the simple diagram below.



THE ISSUE

Manufacturers of X capacitors have their capacitors tested and certified by a Nationally Recognized Testing Laboratory (NRTL), and a certificate is provided. X-type capacitors are considered a safety critical component of the end-product, and as a compliance engineering professional, it is crucial that you know which subclass to use. Not selecting the correct sub-class for the end-products' application will result in a non-compliance that will cause re-design and delay of production release of the product. Switching is not a simple process if you select an X2-rated capacitor and need an X1 instead. First, you must find a suitable X1-rated part and try to make it fit into the existing design. X1-rated capacitors are physically bigger than X2-rated parts.

X-TYPE CAPACITOR SUBCLASSES

The standard most often used to certify X (and Y) capacitor types is IEC 60384-14. This standard specifies three different subclasses of X-type capacitors depending on their peak impulse voltage rating.

X3 Subclass

The subclass X3 has a peak impulse voltage rating of less than or equal to 1.2 kV. This is not too high of an impulse rating, so only use X3-rated capacitors in benign environments (those protected from overvoltage transients). Since it is not to be used for robust design, the X3 subclass is not discussed further in this post.

X2 Subclass

The subclass X2 has a higher peak impulse voltage rating than the X3 type. The X2 subclass has a peak impulse rating of less than or equal to 2.5 kV.

X1 Subclass

Finally, the subclass X1 is even more robust than the X2 capacitor type. It has a peak impulse rating of greater than 2.5 kV and less than or equal to 4.0 kV.

WHICH SUBCLASS TYPE DO I USE? X1 OR X2?

To determine which subclass type to use (X1 or X2), you must know the end-product's overvoltage category of the intended environment. This is something that is usually determined early in the product development cycle.

IEC 60664-1 (latest edition is dated 2020) describes the overvoltage categories. There are four overvoltage categories, designated as I, II, III, and IV. Devices installed in category IV locations are subjected to the most severe transients (surges), whereas category I locations are the least severe, protected environments. This post focuses on categories II and III. Examples of category II locations are household appliances plugged into the standard home wall outlet. Category III locations are closer to the voltage supply and subjected to harsher transient conditions. Examples are switches in the fixed installation and equipment for industrial use with permanent connection to the fixed installation.

Annex B (informative) of IEC 60664-1 describes nominal voltages of mains supply for different modes of overvoltage control. See Table B.1 – Inherent control or equivalent protective control. This table is something you need to look at.

For example, select 300V as the voltage line-to-neutral derived from nominal voltages AC or DC. The rated impulse withstand voltage for the equipment is provided for each overvoltage category. For category II, it is 2.5 kV; for category III, it is 4.0 kV.

Given this information, if your end-product is installed in an overvoltage category II location, then an X2-rated capacitor is acceptable. However, if it is installed in an overvoltage category III location (a location that requires a rated impulse withstand voltage of 4.0 kV), then an X1-rated capacitor is required.

WHAT IF I SELECT AN X2 BUT REQUIRE AN X1?

All is not lost if you inadvertently select an X2-rated capacitor but require an X1. You can install a clamping device (such as a metal oxide varistor) across the line that limits the transient overvoltage seen by the rest of the circuit to less than or equal to 2.5 kV and work with your NRTL to accept it. This workaround has some risks as it depends on the NRTL's policy for dealing with this situation, which could change anytime.

MILITARY AND AEROSPACE EMC

DO-160

By Patrick André

Last month, I talked about the RTCA and who they are. This month, let us look at the history and development of DO-160.

The RTCA document titled "Environmental Conditions and Test Procedures for Airborne Equipment" is better known as DO-160 and as EUROCAE ED-14 in Europe and elsewhere. It is based on a history of documents and test procedures to establish equipment performance standards for avionics in a wide range of environmental conditions.

The roots of this document go back to April 13, 1954, and a publication called DO-60 (Note 60, not 160), titled "Environmental Test Procedures Airborne Radio Equipment" – based on earlier works such as DO-44. The document includes just 15 pages for temperature, altitude, humidity, vibration and shock tests, and two tests one would consider EMI Tests. These two tests were a "Susceptibility Test," which injected a 1000 µV signal through a capacitor onto various lines, and a "Low Voltage Test."

By June 1968, DO-138 "Environmental Conditions and Test Procedures for Airborne Electronic/Electrical Equipment and Instruments," was created. It appears to be based on DO-108, but that document is unavailable to verify that basis. DO-138 has much in common with early editions of DO-160, including setup drawings and test equipment. However, for EMI testing, the emissions section is included as Appendix A, not part of the body of the test procedure.

For the release of DO-160 in February of 1975 and DO-160A (July 1980), all current sections from 1-21 are in place. The use of document revisions (DO-160A, DO-160B, etc.) and of Change Notices (ex., DO-160A has Notice 1 replacing Section 9 Explosion Test) locked DO-160 into the Environmental Test Procedure it is now known as.

With DO-160C, December 1989, and its three Change Notices, the EMI section of the document took a radical turn. Before this, conducted and radiated susceptibility test levels were typically benign, often performed using a signal generator and no amplifier – the highest level was Category Z in DO-160B at 2 V/m from 118-135 MHz. However, Section 20 was updated to include test amplitudes of no less than 5 V/m (Category T) and as high as 200 V/m (Category Y), with testing performed up to 18 GHz. Previously, no testing was performed above 1.215 GHz. In addition, Section 22 Indirect Lightning was introduced, and Section 23 for Direct Lightning.

In DO-160D, Section 18 through Section 21 mandated sweep rates for testing, and for emissions, the bandwidths to be used were fixed, with broadband testing removed. Section 25, ESD, was included. In Notice 2, Sections 16 and 18 were updated, and in Notice 3, Indirect Lightning was reworked to include Multiple Burst and Multiple Stroke effects.

Currently, the special committee, SC-135, along with EUROCAE working group WG-14, is laboring to complete DO-160H along with EUROCAE's ED-14H, with plans to have it available in December 2025. A great deal of work is being done to clean up the document, correct misunderstandings and misinterpretations, and hopefully arrange the information in a more logical manner. When completed, the committee hopes to start work on the update to DO-357, the user guide and supplement for DO-160. It is hoped that providing more information in DO-357 will help the user understand the intent and goal of the test, perform proper measurements, and obtain quality data for the compliance of the avionic system.

In the EMC world of aeronautics, the RTCA has other documents which may be of interest. These include:

- DO-199 – Potential Interference to Aircraft Electronic Equipment from Devices Carried Aboard (Volumes 1 and 2)
- DO-233 – Portable Electronic Devices Carried on Board Aircraft
- DO-294C – Guidance on Allowing Transmitting Portable Electronic Devices (PED) Tolerance
- DO-307B – Aircraft Design and Certification for Portable Electronic Device (PED) Tolerance
- DO-363 – Guidance for the Development of Portable Electronic Devices (PED) Tolerance for Civil Aircraft
- DO-380 – Environmental Conditions and Test Procedures for Ground Based Equipment

It should be noted that DO-199 is a 1988 document and report based on an earlier DO-119 document from 1963. Portable electronics in the 1960s were limited to portable radios and the like. It was not found to be a significant concern until 1983 when some aircraft carriers would not allow the use of personal computers by passengers on the aircraft. In the next blog, we will look at the use of portable electronics on aircraft and the documents above, which address them.

EVALUATING THE LATEST STRATEGIES FOR ELECTROSTATIC HAZARD MITIGATION IN MEDICAL ENVIRONMENTS

A Review of ESDA's TR29 "Guidance for Control of Electrostatic Hazards in Healthcare Facilities"

Tom Ricciardelli founded SelecTech in 1993 to create products from recycled materials, and invented an adhesive-free, interlocking static-control flooring system. He joined the ESD Association in 2013, and currently chairs multiple working groups. Ricciardelli can be reached at tricca@selectech.com.

By Tom Ricciardelli

Electrostatic discharge (ESD) poses significant hazards in healthcare settings, affecting both patient safety and the functionality of medical equipment. Understanding these hazards is crucial for implementing effective prevention measures.

The earliest concerns with ESD in the healthcare environment were related to preventing ignitions of anesthesia caused by ESD. In 1953, the Bureau of Mines published "Static Electricity in Hospital Operating Suites: Direct and Related Hazards and Pertinent Remedies"[1]. This document provided technical background on the nature of these hazards and prescribed the use of static control flooring and equipment grounding to mitigate this risk. Since that time, the National Fire Protection Agency (NFPA) created NFPA 99 "Healthcare Facilities Code"[2] to help prevent fires and explosions in healthcare facilities and included guidance on preventing ESD-related events.

However, in more recent years, the use of flammable anesthesia has decreased, and the NFPA dropped its guidance on controlling ESD from NFPA 99. Simultaneously, the use of sensitive electronic devices and electronic data has dramatically increased, creating new ESD-related risks. Moreover, the use of synthetic materials, such as bedding and gowns, increased the electrostatic charges being created in these environments. With NFPA dropping its guidance and these new risks emerging, facility managers were left with problems and nowhere to turn for help.

In response to this need, the International Electrotechnical Commission (IEC) published in 2018 IEC 61340-6, "Electrostatics - Part 6-1: Electrostatic control for healthcare - General requirements for facilities"[3], which provides technical requirements and recommendations for controlling electrostatic phenomena in healthcare facilities, including requirements for equipment, materials, and products used to manage static electricity.

With support from members of the IEC committee, the ESDA decided to create a guidance document that delved deeper into this topic, provided more technical background on the nature of the risks involved, additional guidance on the mitigation measures that can be used, and descriptions of programs that can be implemented to ensure proper implementation of these recommendations. This new technical report, TR29 "Guidance for Control of Electrostatic Hazards in Healthcare Facilities"[4], was released this year and provides a comprehensive review of the nature of the risks and the scientific support to justify the implementation of the recommended mitigation measures.

CAUSES OF ESD IN HEALTHCARE FACILITIES

TR 29 provides a comprehensive description of how static charges are generated to provide the reader with a better understanding of how to minimize and control static charge generation. Some common sources of static charge generation in a healthcare facility are shown in Figure 1.

Figure 1: Common sources of static charge generation in a healthcare facility

Means of Generation	10-25% RH
Walking across vinyl tile	12,000 volts
Moving in a chair with urethane foam	18,000 volts
Opening a plastic package of medical devices	20,000 volts
Walking across carpet	35,000 volts
Stripping bedding	60,000 volts

Table 1: Examples of static generation voltage levels

Risk	Voltage Level of Concern
Damage and loss of function to equipment	8,000 volts
Electronic record corruption	5,000 volts
Involuntary reaction to shocks	10,000 volts
Contamination caused by ESA	2,000 volts

Table 2: Voltage levels of concern in a healthcare environment

Table 1 provides some examples of the voltage that can be generated in some typical activities that occur in a healthcare facility. Table 2 provides the levels of concern for the various risks of concern in a healthcare setting. As you can see, common activities in a healthcare setting can easily generate electrostatic charges that are far in excess of levels of concern.

RISKS ADDRESSED IN ESDA TR29

TR29 addresses the most common risks associated with ESD in the healthcare environment. As previously mentioned, there are now risks associated with the use of electronic equipment and data. The risks addressed, depicted in Figure 2, include:

- *Disruption/loss of function of medical devices:* Medical instruments, such as MRI machines, ventilators, and infusion pumps, are highly sensitive to ESD. A discharge can cause these devices to malfunction or fail, potentially leading to incorrect diagnoses or treatment interruptions. For instance, an ESD event could disrupt the operation of a heart monitor, leading to false readings that might cause unnecessary alarm or, conversely, a lack of response to a genuine emergency.
- *Disruption/loss of data:* ESD can corrupt electronic data, impacting patient records and diagnostic results. This can lead to delays in treatment and errors in patient care. For example, if an ESD event occurs while updating a patient's electronic health record (EHR), it could result in the loss of critical information, such as medication allergies or recent test results, which are essential for making informed medical decisions.
- *Shocks to personnel:* Patients and healthcare personnel can experience painful electrostatic shocks. These shocks can cause involuntary movements, which may lead to accidents or injuries, especially in critical care environments. For example, a patient receiving an intravenous injection might jerk their arm due to an ESD shock, potentially causing the needle to dislodge and leading to further complications.
- *Contamination caused by electrostatic attraction (ESA):* ESD can increase the deposition of microorganisms onto charged surfaces, contributing to hospital-acquired infections. This is particularly concerning in sterile environments like operating rooms and intensive care units. For instance, if ESD causes dust particles carrying bacteria to settle on surgical instruments, it could increase the risk of postoperative infections.
- *Ignition of flammable materials:* Although the use of flammable substances in healthcare has decreased, the risk of fires and explosions due to ESD remains, especially in laboratories and areas where oxygen is used. For example, in a laboratory setting, an ESD event could ignite volatile chemicals, leading to a fire that endangers both staff and patients.

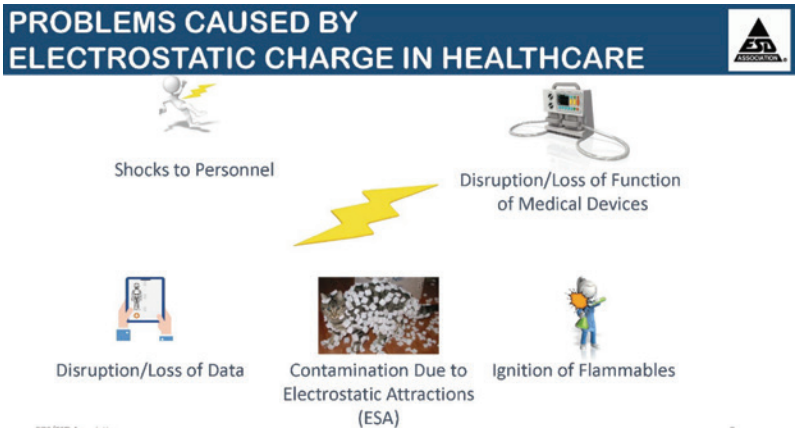


Figure 2: Problems caused by electrostatic charge in healthcare

PREVENTION OF ESD IN HEALTHCARE SETTINGS

Preventing ESD in healthcare settings requires a multifaceted approach. The mitigation measures recommended in TR29 include:

- *Static control flooring/footwear/mobile equipment:* Installing proper static control flooring in critical areas can help dissipate static charges from personnel and mobile equipment, such as hospital beds and IV carts. This is particularly important in operating rooms and laboratories. Also, static control tiles or carpets can be used in areas where sensitive electronic equipment is frequently used, such as radiology departments. Static control flooring can also be used in areas where data is entered, transferred, or stored.
- *Equipment grounding:* All electrical/electronic medical equipment should be properly grounded to prevent ESD. As mentioned above, this can also include grounding mobile equipment through the use of a drag chain or conductive wheel in combination with a static control floor.
- *Low-charging and dissipative materials:* Low-charging relates to how much charge is generated upon contact and separation of the material from itself or other materials. Many patient care items are available with additives or treatments that make them low-charging. Conversely, untreated versions of these items are typically made of synthetic textile materials that are electrically insulating and can potentially acquire significant electrostatic charge. Also, applying antistatic sprays to surfaces can help reduce the generation of charges. For instance, antistatic sprays can be applied to synthetic garments to reduce charge generation and minimize the risk of ESD.
- *Ionization:* Ionizers can be used to neutralize static charges in the air and on insulative items, such as plastic packaging. Ionizers emit ions that attach to charged particles, neutralizing them and preventing ESD. Ionizers are generally useful for spot applications. For example, ionizers can be used to neutralize the static charge that is generated when surgical device packages are opened or at entrances to surgical suites to help remove ESA-attracted particles from personnel garments.

The ESD risks in a healthcare facility will vary depending on the area of the facility. TR29 provides a section that defines the inherent risks by type of area within the facility and the recommended mitigation measures to take for those areas.

- *Humidity control:* Maintaining a relative humidity level of 40-60% can help reduce static electricity. Dry environments are more prone to ESD, so humidifiers can be used to maintain optimal humidity levels. For example, in a hospital ward, humidifiers can be strategically placed to ensure that the air remains sufficiently moist, reducing the likelihood of ESD events. There is also strong evidence that controlling humidity in this range has health benefits for occupants and can help reduce infections from airborne contaminants.
- *Static control seating:* The routine movement of a person seated in a chair or moving the chair across the floor can generate significant static charges. Using static control chairs in combination with a static control floor can be an effective means of removing those charges, which would be helpful in areas such as computer workstations.

DEFINED RISKS AND SUGGESTED MITIGATION BY AREAS

The ESD risks in a healthcare facility will vary depending on the area of the facility. TR29 provides a section that defines the inherent risks by type of area within the facility and the recommended mitigation measures to take for those areas. The guidance is defined for:

- Public spaces/waiting areas
- Administrative and office areas
- Server rooms and data closets
- Clinical examination rooms
- Patient wards
- Acute care wards
- Diagnostic areas
- Surgical and operating suites
- Laboratories
- Pharmacies

ESD CONTROL PROGRAMS

TR29 provides a sample of a control program that a healthcare facility can implement to reduce the risk of ESD hazards. Modeled after ANSI/ESD S20.20, this guidance includes suggestions for:

- *Electrostatics coordinator:* Having a designated person to oversee the program. This person should have basic knowledge of electrostatics.
- *Staff training:* Healthcare personnel should be trained on the importance of ESD control and the proper use of ESD prevention tools. This training could be as simple as having an understanding of TR29 since it provides a comprehensive background on the science of ESD, the nature of the risks, and details on mitigation measures. Also, regular

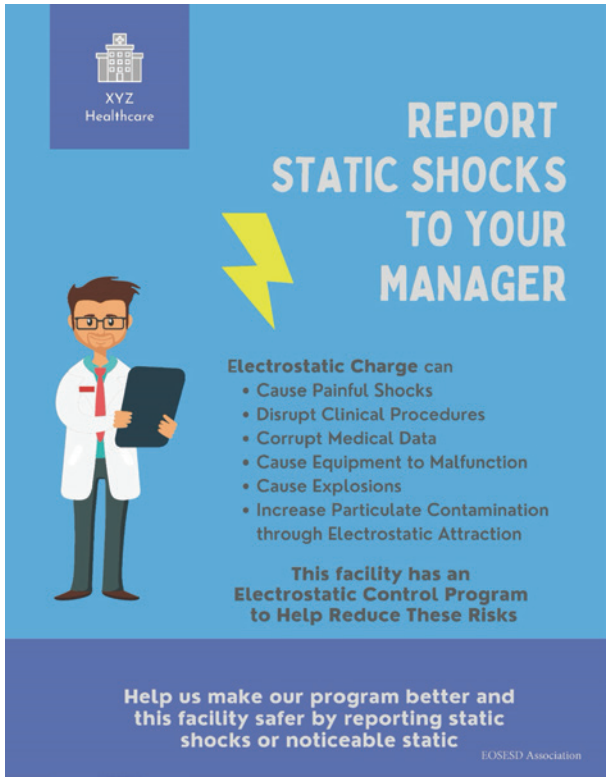


Figure 3: Poster displaying best practices for ESD prevention

awareness campaigns can help reinforce the importance of ESD control and encourage compliance with ESD prevention protocols. For instance, posters, such as the one shown in Figure 3, and informational brochures can be distributed throughout the healthcare facility to remind staff of best practices for ESD prevention.

- *Defined controls by facility area:* The sample program includes a matrix that can be used to define the mitigation measures to be used in the various areas of the facility
- *Compliance verification:* The sample program also provides measures to use to ensure mitigation measures are functioning properly.
- *Recordkeeping:* It is also recommended that the facility keep records of the mitigation measures employed, any records of their compliance verification, and reports of incidences of ESD events.
- *Consultation:* Healthcare facilities can benefit from consulting with ESD experts to develop and implement effective ESD control programs. These experts can provide guidance on best practices and help identify potential ESD hazards. For example, an ESD consultant can conduct a thorough assessment of a hospital's ESD control measures and recommend improvements. ESD experts can also provide specialized training programs for healthcare personnel. These programs can cover advanced ESD prevention techniques and the proper use of ESD control tools.

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4. ESD TR29.0-01-24, *ESD Association Technical Report for the Protection of Electrostatic Discharge Susceptible Items – Guidance for Control of Electrostatic Hazards in Healthcare Facilities.*

FILTER DESIGNS FOR SWITCHED POWER CONVERTERS – PART 1: OVERVIEW

Understanding the Power Converter and Its System Requirements for Good EMC Practice

Dr. Min Zhang is a Senior Contributor to *In Compliance Magazine*, and the founder and principal EMC consultant of Mach One Design Ltd., a UK-based engineering firm that specializes in EMC consulting, troubleshooting, and training. His in-depth knowledge of power electronics, digital electronics, electric machines, and product design has benefitted companies worldwide. Zhang can be reached at info@mach1design.co.uk.

By Dr. Min Zhang

I have always wanted to write articles on filter design. Needless to say, the subject alone can easily spawn a book. This is because, in the world of electronics, we have power filters, transformers, low-frequency filters, digital circuit filters, and analog circuit filters. Each design requires its unique and dedicated filter design principles. Additionally, we have different requirements, and it is fair to say that most commercially available filters are designed to meet certain EMC specifications. Hence, they are most likely designed to work efficiently with the test setup, particularly the line impedance stabilization network (LISN) for conducted emission tests.

Given the numerous points to consider, capturing everything in one article is nearly impossible. My favorite books and articles on this subject are listed in the reference section [1]-[3], and I encourage readers to explore them.

This series of articles focuses primarily on power filters for switched-mode power converters and similar applications. By defining this boundary, I am concentrating on conducted emissions (from 9 kHz to 110 MHz) and radiated emissions (from 30 MHz to 1 GHz). Although most power supplies also need to meet transient protection requirements, we will not cover transient protectors in this series. Topics related to harmonics, as well as digital and analog circuit filter design, are beyond the scope of this series. When referring to switched power converters and similar applications, I mean power converters such as AC-DC, DC-DC, DC-AC, and motor drive applications.

We want to discuss filter design in this specific field because we now live in an era where we aim to electrify everything for the good purpose of making a more sustainable future. In this article, which is Part 1 of the series, I will provide an overview of the filter design principles for switched conversion applications.

UNDERSTANDING THE EMC & EMI REQUIREMENTS

First, let us distinguish between the concepts of EMC and EMI requirements. When we refer to EMC (electromagnetic compatibility), we mean meeting the electromagnetic compatibility requirements. This entails demonstrating control over electromagnetic interference (EMI) by adhering to the emission limits defined by the specific standard relevant to your product application. For instance, if you are designing a power supply for an aircraft, the conducted emission limit defined in RTCA DO-160 is very different from the limits for a commercial application (CISPR/FCC Class B limit). The LISNs used in these two applications differ as well [4], which means you need to understand your source-load impedance to effectively design the filter.

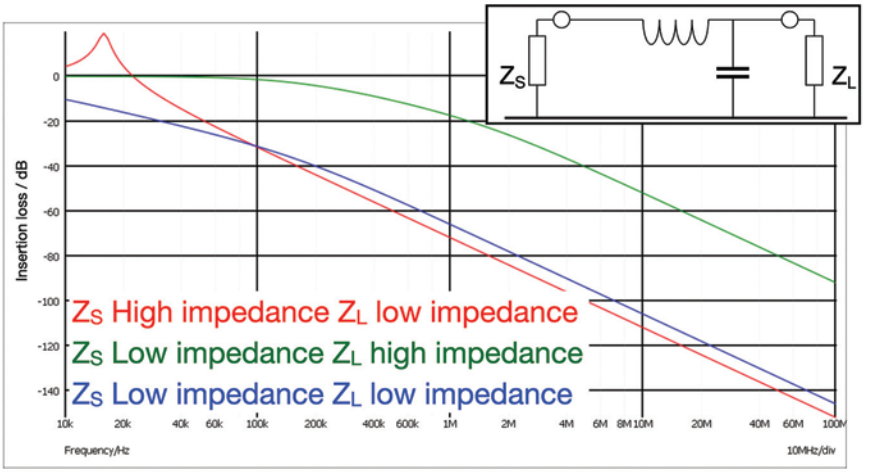

Figure 1: The effectiveness of the filter configuration (such as this simple L-C low pass filter) depends on the impedances seen at either end of the filter network.

Most of my work involves helping clients meet these EMC requirements, whether they are the stringent military specifications or the relatively easier industrial emission standards. However, engineers sometimes face unique challenges. For example, a client in the semiconductor manufacturing industry required an extremely EM-quiet environment for their machines to operate accurately. This meant they needed to control the electromagnetic interference (EMI) based on their own system requirements. In this scenario, there is no LISN per se, as the power supply design depends solely on their specific system. Consequently, the system's impedance is unlikely to match a 5 or 50 µH LISN [5].

Although the requirements differ, they all aim to achieve one end goal: operating the product with controlled EM noise to avoid interfering with other equipment and preventing nuisance issues within the product/system itself.

UNDERSTANDING THE SWITCHED POWER CONVERTER OPERATION

This area is crucial. An EMC engineer with little or no knowledge of switching converters cannot effectively solve the challenging EMI issues caused by these converters. Similarly, design engineers with advanced knowledge of complex switching schemes but lacking an understanding of EM theory (particularly the concept of energy in space) will struggle to control emissions.

I highlight this because I experienced it first-hand. During my PhD research on sophisticated switching schemes, I lacked EM knowledge. It was only years later, after understanding EM theory, that I could view the problem from a different perspective. Many EMC engineers likely have similar stories.

It's unrealistic to expect EMC engineers to possess the same level of knowledge of power converters as power electronics design engineers. EMC engineers have their own disciplines, including testing skills and simulations. However, a basic understanding of power converter fundamentals is always useful.

In my view, the two essential circuits that engineers need to understand are the buck converter and the flyback converter. Why? The buck converter represents the most basic DC-DC step-down converter, widely used in power conversions. Understanding the buck converter helps in understanding other applications, such as boost converters, which are essentially the mirror image of buck converters (as shown in Figure 2 (a) vs (b)).

As shown in Figure 2, most motor drive applications, whether DC brushed motors or brushless DC motors (single-phase or three-phase), are essentially made of buck converters. For instance, three-phase brushless DC motors use hardware that is essentially three synchronous buck converters, regardless of the control method (sinusoidal pulse width modulation (PWM), space vector modulation (SVM), field orientated control (FOC), etc.). Similarly, the concepts of hot loop and switch nodes in the buck converter apply to motor drive applications. The hot loop areas and the switch

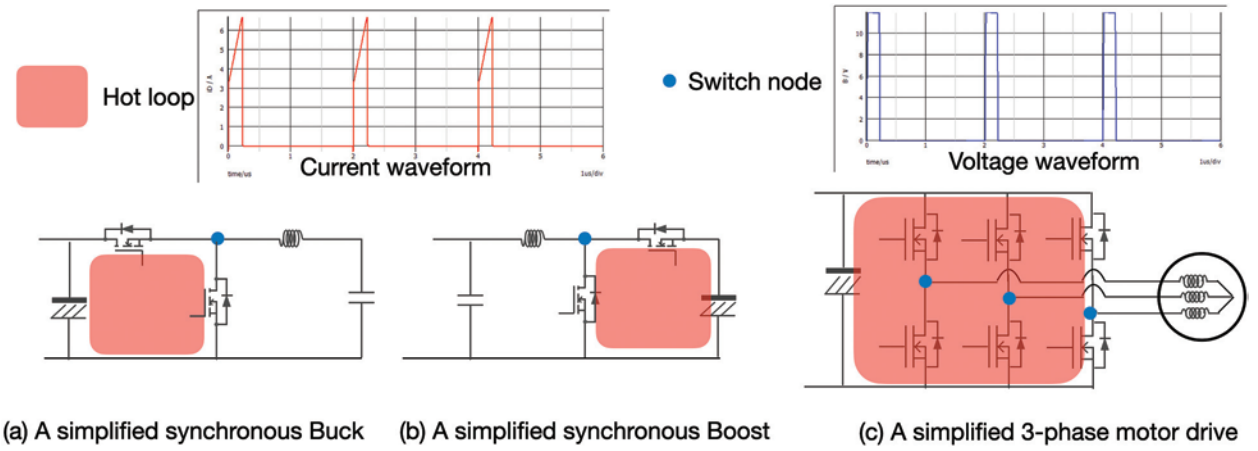

Figure 2: (a) Simplified diagram of a synchronous buck converter, (b) simplified diagram of a boost converter, and (c) a three-phase motor drive consisting of three synchronous buck converters.

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Model Number	Frequency Range	Rated Power Watts	Gain dB
10KHz-250MHz, Low Frequency Amplifiers			
AMP2080B	10kHz-250MHz	100	50
AMP2080C-1	10kHz-250MHz	150	52
AMP2080C	10kHz-250MHz	300	55
AMP2080D	10kHz-250MHz	600	58
80-1000MHz, VHF, UHF Range Amplifiers			
AMP2032	80-1000MHz	300	55
AMP2071-2	80-1000MHz	500	57
AMP2071A-LC	80-1000MHz	750	60
AMP2115-LC	80-1000MHz	1300	61
AMP2121-LC	80-1000MHz	2000	63
700MHz-6.0GHz, Broadband Amplifiers			
AMP2070C	0.7-6.0GHz	100	50
AMP2070A	1.0-6.0GHz	150	52
AMP2030-LC	1.0-6.0GHz	300	55
AMP2030-600-LC	1.0-6.0GHz	600	58
AMP2030D-LC	1.0-6.0GHz	750	59
AMP2030LC-1KW	1.0-6.0GHz	1000	60
2.0-8.0GHz, SC Band Amplifiers			
AMP2085-1	2.0-8.0GHz	120	51
AMP2085C	2.0-8.0GHz	200	53
AMP2085E-1LC	2.0-8.0GHz	250	54
AMP2085E	2.0-8.0GHz	400	56
6.0-18.0GHz, High Frequency Amplifiers			
AMP2118	6.0-18.0GHz	40	46
AMP2111	6.0-18.0GHz	50	47
AMP2033-LC	6.0-18.0GHz	100	50
AMP2065A-LC	6.0-18.0GHz	200	53
AMP2065B-LC	6.0-18.0GHz	300	55
AMP2065E-LC	6.0-18.0GHz	500	57
18-26.5GHz, K-Band, Millimeter Amplifiers			
AMP4032	18.0-26.5GHz	10	40
AMP4065LC-1	18.0-26.5GHz	20	43
AMP4065-LC	18.0-26.5GHz	40	46
AMP4065A-LC	18.0-26.5GHz	100	50
AMP4065B-LC	18.0-26.5GHz	200	53
26.5-40.0GHz, Ka-Band, Millimeter Amplifiers			
AMP4072	26.5-40.0GHz	10	40
AMP4066LC-1	26.5-40.0GHz	20	43
AMP4066-LC	26.5-40.0GHz	40	46
AMP4066A-LC	26.5-40.0GHz	100	50
AMP4066B-LC	26.5-40.0GHz	200	53
18.0-40.0GHz, Millimeter Amplifiers			
AMP2145A-LC	18.0-40.0GHz	10	40
AMP2145B-LC	18.0-40.0GHz	25	44
AMP2145C-LC	18.0-40.0GHz	50	47
40.0-50.0GHz, Q-Band, Millimeter Amplifiers			
AMP4076-1	40.0-50.0GHz	5	37
AMP4076A	40.0-50.0GHz	20	43
AMP4076B	40.0-50.0GHz	40	46
AMP4076C	40.0-50.0GHz	80	49

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nodes are highlighted in Figure 2. The hot loop area is defined as the loop area where the worst di/dt current circulates, indicating a high level of magnetic field (near field). This highlights the importance of reducing this area. The switch node is defined as the worst dv/dt voltage node in the circuit, indicating a high level of changing electric field. This underscores the importance of minimizing capacitance coupling nearby.

We will discuss the details of how buck converters work and their EMI characteristics in later articles. So why flyback converters? The biggest disadvantage of a buck converter is that it is not isolated, meaning it does not provide safety isolation. For many applications, system safety requirements necessitate an isolation transformer. Typically, for power levels under 150W, a flyback converter is preferred due to its good balance of efficiency, size, and cost (owing to the small number of components). Such converters are popular in designs like mobile phone and laptop chargers. Therefore, understanding the operation of flyback converters is essential.

Understanding flyback converters helps in understanding other circuits like forward converters. Flyback converters are popular in the power range under 150W. When power requirements increase, we often see topologies such as phase-shift full bridge (PSFB), dual-active-bridge (DAB), LLC, etc. However, the principles of these higher power converters are not far from those of a flyback converter.

Isolated flyback converters are more complex due to their requirement for a transformer. It is worth noting

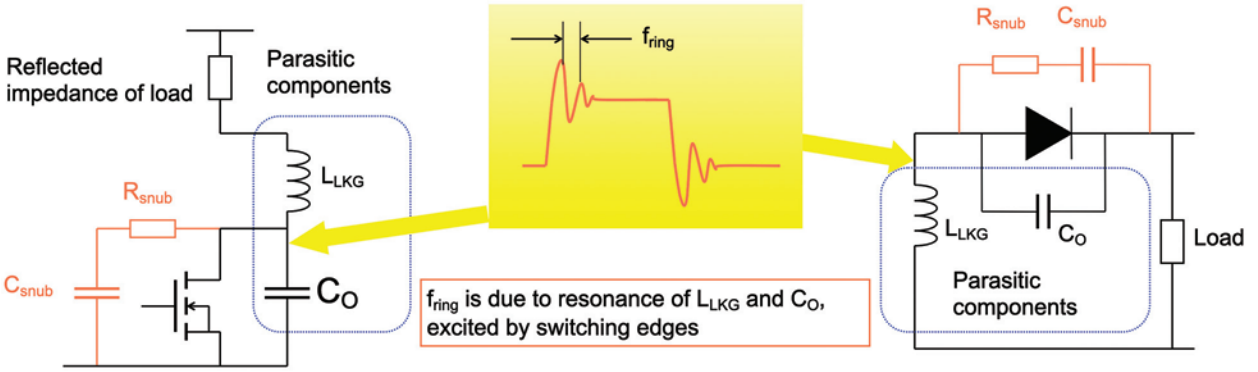
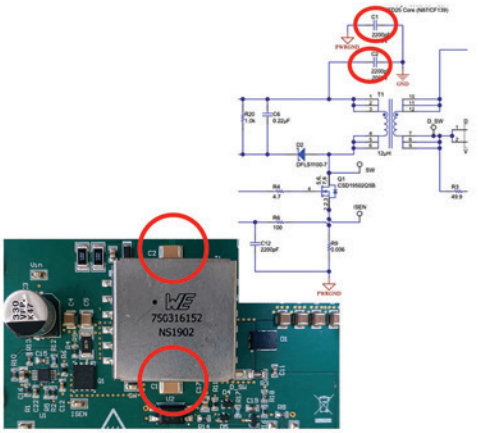
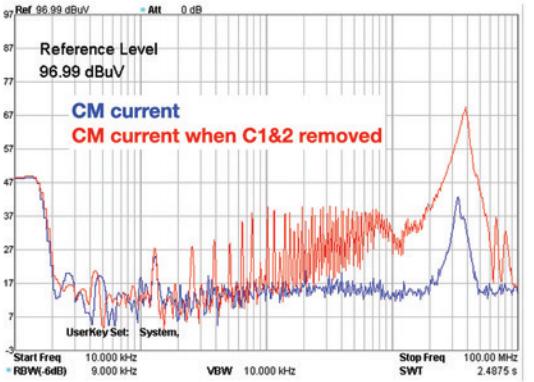


Figure 3: Snubber circuit for flyback converters



Capacitors across the two sides of the transformer



Conducted Emission Current Probe Measurement Results

Figure 4: Putting capacitors across the transformer can reduce the common mode noise, but one needs to be cautious of the leakage current requirement.

that, unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer but rather functions as an inductor with two windings; a more descriptive name should be "two winding inductor" [6]. In most applications, since the flyback transformer stores energy, an air gap is needed. During power conversion, energy moves from the input bulk capacitor to the transformer's air gap and then to the output capacitor.

The presence of the transformer introduces additional considerations. From an EMC perspective, the first is leakage inductance. The leakage inductance of the transformer forms an L-C resonance circuit with the parasitic capacitance of the switching device, causing overshoot and ringing. This is why a snubber circuit is often needed for the converter. This is illustrated in Figure 3.

Another consideration is the parasitic capacitance of the transformer, which includes the primary side, the secondary side, and, most importantly, the capacitance between the primary and secondary sides. This determines the common mode current path of the converter, making it standard practice to place capacitors between the primary and secondary sides of the transformer. I haven't seen many articles discussing how to characterize and test the parasitics of a flyback converter transformer, so we will discuss this in greater detail in subsequent articles.

Both buck and flyback converters generate broadband noise, which is often a significant noise culprit in electronic systems. The concept and consequence of broadband noise is well explained in [7]. In terms of noise profiles, the two circuits discussed above are very similar.

UNDERSTANDING THE BASICS OF FILTER PRINCIPLES

Now that you understand the converter circuits and are familiar with the system EMC/EMI requirements, you are ready to design a filter. Filters (except for active filters, which require a microcontroller) are made of passive components, which are relatively simple, such as inductors (L), capacitors (C), and resistors (R). You also have

Engineers sometimes buy an off-the-shelf part and hope it will magically eliminate all noise. In other cases, they simply add some inductors and capacitors without proper calculation.

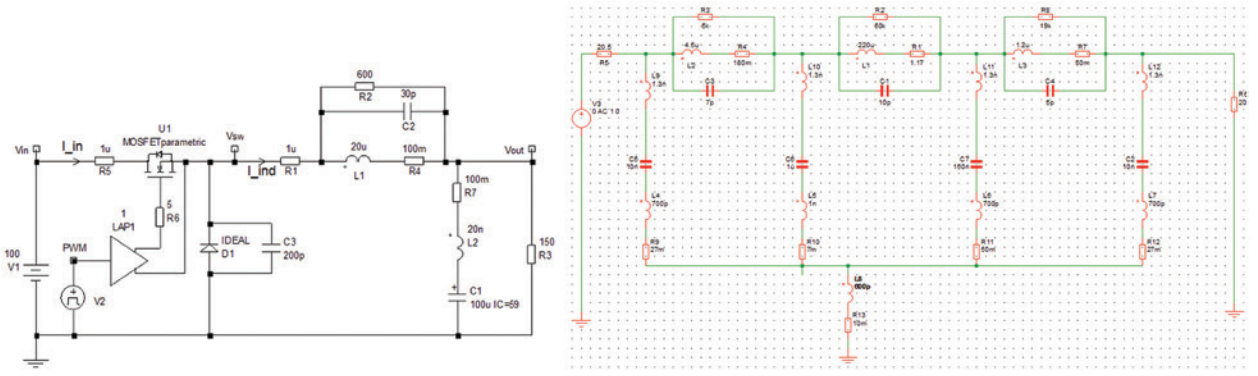
transient protection devices, such as MOVs, TVS diodes, etc. Therefore, filter design might seem easy at first glance. The basic filter design flow is as follows:

1. *Understand your circuit's noise profile:* This can be achieved through benchtop tests and/or SPICE simulations.
2. *Determine the required dB reduction (attenuation):* Based on the results, identify how much attenuation is needed across the frequency range.
3. *Select the L, C, and R components:* Choose components to meet the required reduction, often determined by the filter's cut-off frequency.
4. *Perform a simulation:* Verify that the noise is reduced (e.g., by 60 dB) through simulation.
5. *Implement the filter:* Build the filter based on your design.
6. *Measure the performance:* Test the filter and observe the results. Often, the actual performance may not match your expectations.

This is a common scenario I observe in my fieldwork. Engineers sometimes buy an off-the-shelf part and hope it will magically eliminate all noise. In other cases, they simply add some inductors and capacitors without proper calculation. But let's say you followed Steps 1-5—why might the results still be unsatisfactory?

We will discuss this in greater detail later, but at a top level, here are common areas that engineers often overlook:

1. *Simulation model detail:* Does the model capture all parasitics, such as leakage inductance of transformers and parasitic capacitance of switching devices (Figure 5(a))?
2. *Inclusion of a LISN circuit:* Does the simulation include a LISN circuit? Often, design engineers who are not EMC specialists may overlook this.
3. *Parasitic capacitance to test ground:* Does the simulation model include parasitic capacitance between the circuit and the test ground plane? This is crucial for determining the common mode current path.
4. *Differential and common mode noise separation:* Has the engineer clearly separated the noise types into differential and common modes?
5. *Realistic component models:* When building L-C-R filter circuits, have the parasitics of the L, C, and



(a) A more realistic buck converter model

(b) A more realistic filter model

Figure 5: (a) a more realistic simulation circuit of a buck converter, including key parasitics, (b) a more realistic filter circuit (differential mode only).

R components been considered? Engineers should use a more realistic passive component model based on the impedance curves provided by manufacturers (as shown in Figure 5 (b))

6. *Filter damping:* Is the filter dampened? High-Q (resonant) filters can worsen the situation.
7. *Filter connection to the board:* Has the connection of the filter, for example, capacitors to RF reference, been well considered? The "ground" connection is equally important. (I always try to avoid using "ground," so we will discuss this in future articles).
8. *Filter layout:* Is the layout of the filter well-considered? Could the magnetics in the filter couple noise to nearby circuitry?
9. *Saturation and DC offset:* What is the current RMS value going through the magnetics? What is the DC voltage offset on the capacitors?
10. *And more:* The list can go on.

Given these considerations, review your approach—are there any missing elements? Additionally, as mentioned earlier, engineers need to understand their source and load impedance (as shown in Figure 1). The performance of a filter heavily depends on these parameters. When a LISN defines the impedance, it's straightforward. Most commercial off-the-shelf manufacturers design filters based on a defined LISN impedance.

KEEPING UP WITH TECHNOLOGY PACE

When I started as a power electronics engineer 20 years ago, IGBTs were the go-to devices for medium voltage power conversion and motor drive applications. MOSFETs dominated lower voltage applications. By the early 2010s, advancements in technology had reduced the R_{DS}(on) (on-resistance) of MOSFETs to a few milliohms, enabling higher efficiency and smaller form factor products. Of course, in terms of EMC/EMI challenges, we had to deal with tail currents related to IGBTs, reverse recovery charge issues with MOSFETs, and fine-tuning dead time for applications using both devices. Nonetheless, we managed. The switching speeds of MOSFETs increased, but never to a level that was hard to manage.

However, things have changed with the development of wide bandgap devices such as GaN and SiC semiconductors. I write extensively on this subject, which readers can find in [8]. These advancements have had a significant impact on switching speeds, specifically the rise and fall times, creating substantial EMI challenges.

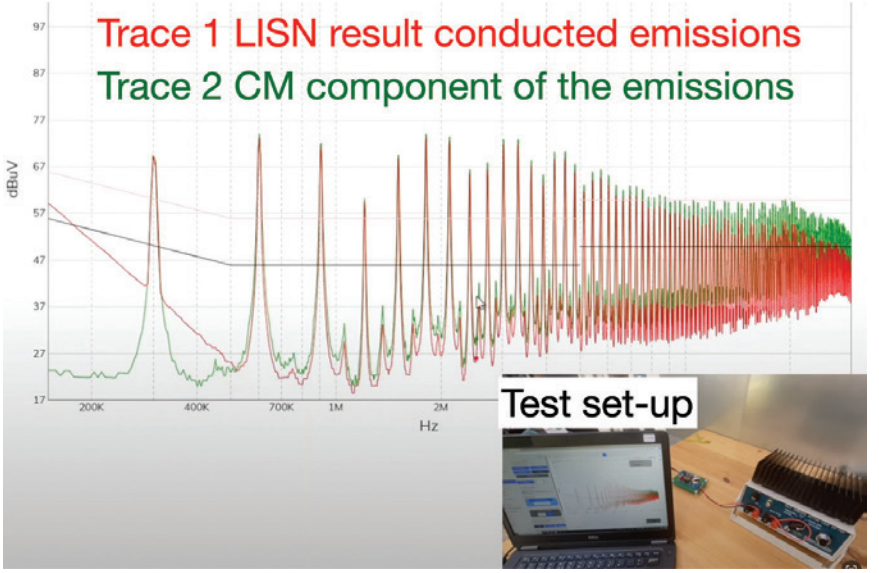


Figure 6: Conducted emissions of an active-clamp flyback converter, the common mode components dominate the noise spectrum
(See a video demonstration at https://youtu.be/70xhHsDk_M4?si=pf3p_q_63UCQEuAC)

One trend I have observed is that, in the past, conducted emissions associated with switched converters were mainly differential mode below a few MHz, while common mode noise dominated the spectrum above a few MHz. This pattern no longer holds with wide bandgap devices. Due to their extremely fast switching, common mode noise now dominates even in the low-frequency range. This is not limited to high voltage, high power systems, as demonstrated in [9]. For example, in much smaller power applications like a GaN-based charger (active clamp flyback converter), common mode noise dominates the low-frequency range, as shown in Figure 6.

This is the trend of technology. As more advanced devices emerge in the future, our knowledge in suppressing the associated noise must also evolve.

OTHER CHALLENGES

As I was writing this article, I realized I was gradually stepping into power converter design territory. I don't want to step on power electronics engineers' toes, but there are many considerations when designing a power converter. Designing a filter with a specific cut-off frequency is not always straightforward; a power converter filter must work with the converter control loop.

To simplify for EMC engineers who don't design power converters: a control loop, often consisting of a feedback loop (typically a voltage loop) and/or a feedforward loop (often a current loop), is designed to stabilize the circuit so the power converter can supply well-regulated power under various load conditions. These loops ensure stable operation even with step changes in load. Power electronics engineers design the loop based on the power converter circuit's transfer function together with the filter transfer function.

A simple controller may have a proportional-integral design (what we call a PI controller). The proportional and integral gains (Kp and Ki) need to consider the filter transfer function to achieve the desired gain margin and phase margin. This means the cut-off frequency of the filter needs to be adjusted. Therefore, the filter's transfer function affects the loop design. It doesn't necessarily deteriorate the loop design, but it does make the design more challenging, requiring compromises, as with all engineering tasks.

As usual, a filter design must also meet size, weight, and, perhaps most importantly, cost requirements.

SWITCHING SCHEMES AND SPREAD SPECTRUM CONTROL

There are switching schemes that can reduce the switching events for power converters, such as discontinuous space vector modulation schemes

(typically employed in three-phase power applications and motor drives). Other schemes aim to reduce the common mode voltage by cleverly selecting the switching vectors (again, a subset of space vector modulations). Such switching schemes can also be employed in multi-level converters. One can simply search the keywords, and there are abundant resources in the IEEE database.

Having spent four years developing such switching schemes myself, I have mixed feelings about them. On an academic level, the idea is certainly sound. However, I have rarely seen such schemes used in industrial applications for various reasons. Perhaps the benefit of using a complicated switching scheme is compromised when it comes to real-life engineering. The complexity of implementing such schemes (not so much in computing power, but in ease of implementation for engineers) is also a reason why they are not popular.

Spread spectrum can be implemented even in the simplest converter topology (such as a buck converter). The idea of not using a fixed switching frequency spreads the energy out, resulting in reduced signal measured in any one bandwidth. It should be noted that such techniques can either result in low-frequency noise improvement or high-frequency noise suppression, sometimes both, depending on the software schemes that engineers employ.

Figure 7 on page 30 demonstrates the conducted emission improvement a spread spectrum technique can achieve on a dual active bridge-based DC-DC converter. Reference [10] demonstrates the high-frequency (radiated emission) improvement by utilizing the spread spectrum scheme. However, as it was rightly pointed out in [7], such techniques are fine for passing the EMC test, but when it comes to protecting a real-life victim, such as a broadcast television, the spread spectrum technique can still potentially cause TVI. I also agree with the

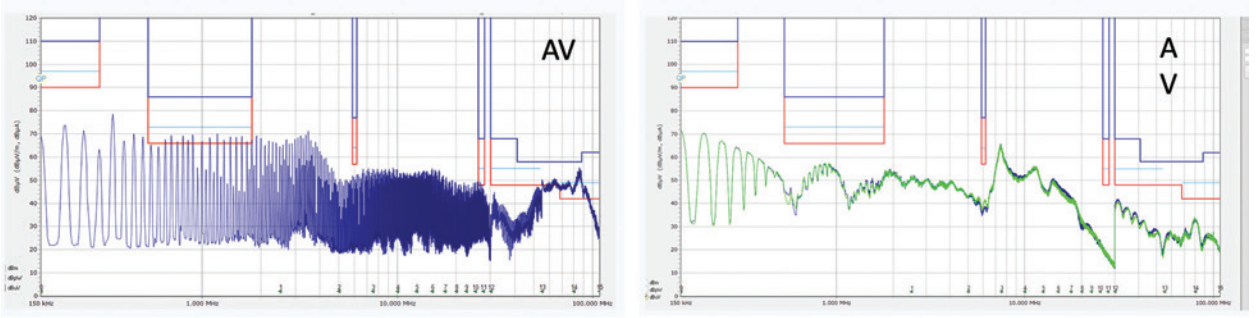


Figure 7: The effect of spread spectrum switching scheme on a dual active bridge converter (Source: Lyra Electronics, the author worked with Lyra on this project.)

argument stated in [7], where the author suggests that with FFT or time-domain type receivers, we should perhaps revisit the emission tests (which always measure the noise with a fixed bandwidth).

IS ACTIVE FILTER TECHNOLOGY GOING TO TAKE OFF?

I am a practical engineer who works almost entirely with industrial partners, so my approach to solving EMI noise is very practical. However, I have also spent my fair share of years in academia, keeping my ears open for potential technological breakthroughs. I have always had a great interest in active filters.

In the past, active filters were primarily used to counter low-frequency magnetic fields [11]. One could also say that the power factor correction technique, widely used in AC-DC applications, is also a form of active filter. Attempts were made to address higher frequency spectra (both conducted and radiated regions), but they never gained traction. In the year 2023, Texas Instruments introduced active filter solutions for both single and three-phase industrial applications [12], detailed in [13]. We are still waiting for more case studies on this chip, and I personally plan to work with it to assess its potential.

Other techniques are also available, forming part of my ongoing research, which I hope to share with the audience in the near future. In conclusion, I believe active filters will eventually find their market, given the advancements in technology.

SUMMARY

In this first part of our series on filter designs for switched power converters, we've laid the groundwork by exploring the essential aspects of EMC and EMI requirements, the operation of switched power converters, and the fundamental principles of filter design. Understanding these core concepts is crucial for effectively managing emissions and ensuring compliance with regulatory standards. By delving into both the buck and flyback converter circuits, we highlighted their significance in power conversion and the common challenges faced in their design.

As technology continues to evolve with advancements like wide bandgap semiconductors, staying abreast of these changes is vital. Future articles will build on this foundation, offering deeper insights into specific design strategies and practical solutions for overcoming EMI challenges in switched power converter applications.

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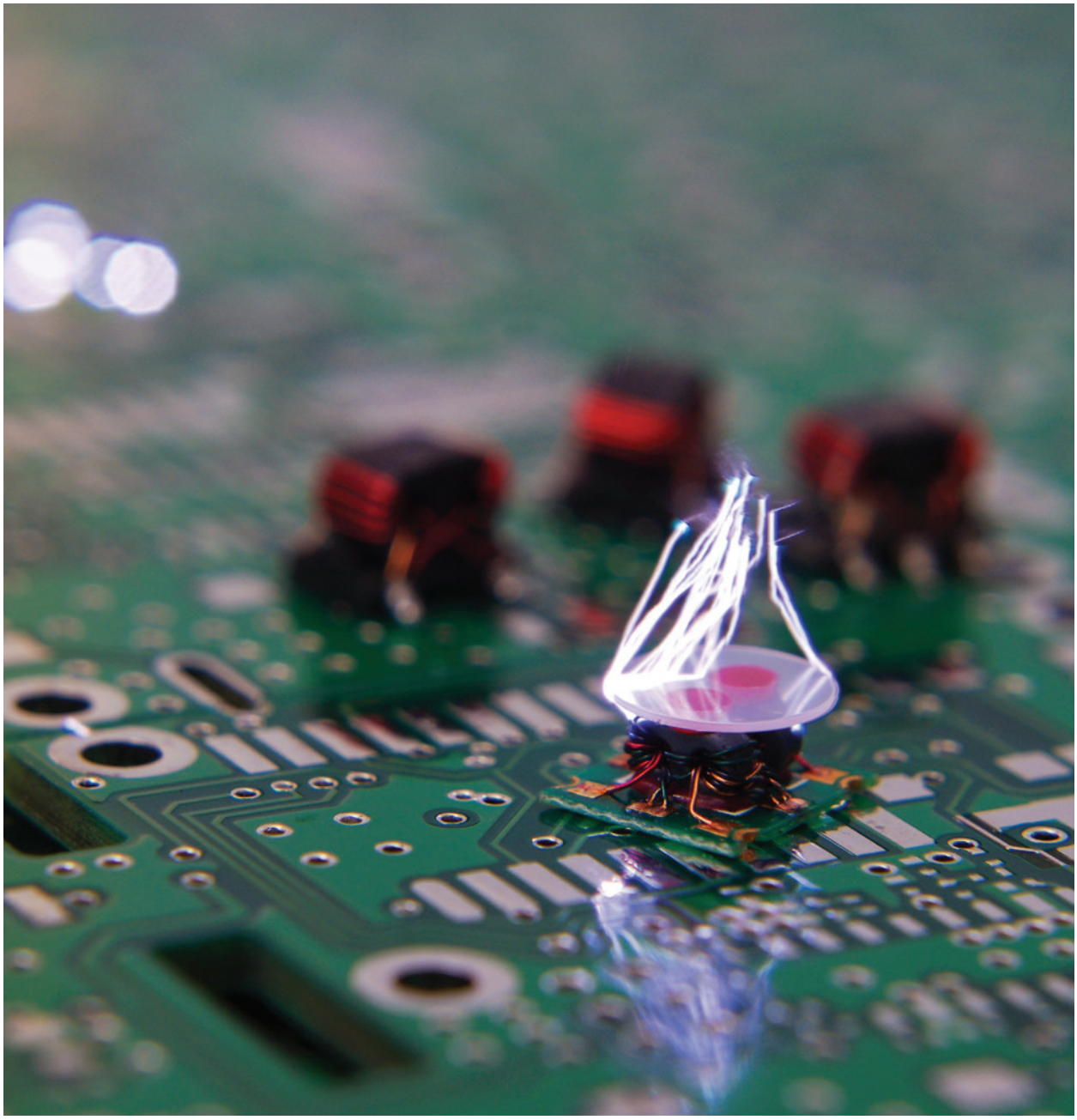
ADVANCED CDM SIMULATION METHODOLOGY FOR HIGH-SPEED INTERFACE DESIGN

Outstanding Paper at the 45th Annual EOS/ESD Symposium



By Umair Ishfaq, Krzysztof Domanski, Susanne Heber, and Harald Gossner

Editor's Note: *The paper on which this article is based was originally presented at the 44th Annual EOS/ESD Symposium in September 2022. It was subsequently awarded the 2022 Symposium Outstanding Paper at the 45th Annual EOS/ESD Symposium in October 2023. It is reprinted here with the gracious permission of the EOS/ESD Association, Inc.*

INTRODUCTION

For high-speed interfaces and RF analog receiver circuits the total capacitive budget is very limited, to optimize performance the capacitance added by Electrostatic Discharge (ESD) protection must be minimized. For ESD protection design this means operating close to the victim breakdown. As the victims in these kinds of circuits are thin-gate oxides directly connected to the pad and the ESD robustness of the devices shrink with every technology node, the ESD protection becomes more challenging. The Charged Device Model (CDM) pulse with its fast and high currents is the most critical ESD event and to achieve "first-time-right" CDM robust designs, a predictive CDM simulation method for pre-silicon design is needed [1][6].

Existing methods of CDM simulation do not reliably predict the failure level of circuits with thin GOX gate at the pad. It was shown in [2] that for the GOX directly at pad the failure is caused by the initial fast current step of 20ps or less of the CDM event. It was also shown that the inductance of the critical path is very important for CDM performance. In another study [7], Charged Coupled (CC)-TLP, with pulse risetime of 20ps, has been demonstrated to predict CDM robustness reliably.

In this work, CDM simulation approach with stimulus current having initial risetime component of 20ps is investigated. The analysis is supported by CDM measurements of packaged Low Noise Amplifier (LNA) circuits, Very Fast (VF)-TLP measurements with 100ps risetime and ultrafast TLP (UF-TLP) measurements with 20ps risetime. To achieve a fast and simple simulation method the simulation is restricted to the receiver circuit itself and the complex RC network of charge distribution across the chip usual for CDM simulations are neglected and a simple charge distribution between VSS and VDD rail is assumed [3]. This is a valid assumption for designs using a common VSS rail for the IP block under investigation. Interconnect and device parasitics are considered by introducing parasitic resistance and inductance values to the schematic for CDM SPICE simulation. Resistance values are extracted. The initial range of inductance values are gained from layout assessment, which is refined based on the voltage measurements at the pads of reference structures. Capacitive coupling between metal lines is accessed to in range of femto-farad, the effects are considered negligible. The simulation is valuable both for an early design study with preliminary target values for resistance and inductance and for the final design using extracted values from layout. An excellent agreement of simulated and measured CDM failure thresholds for CDM currents could be proven for a large set of LNA test structures.

CDM SIMULATION METHODOLOGY

The following study is based on the set of test structures prepared for the purpose of optimizing a LNA receiver circuit. Since the CDM discharge nature is same for all the processes, these structures were used to prove CDM simulation methodology.

Investigated Devices

The devices investigated in this study consist of an input stage with thin-GOX MOS transistors tied directly or via cap to the pad, due to RF performance

requirements. Dual diode protection, with small 6-finger diodes having fast turn-on time, is chosen as ESD protection. The supply filter and a large, dedicated power-clamp are placed close to the pad and routed well to avoid any inductive paths and to reduce bus resistance. The receiving gates are either directly connected to the pad or via a cap that is bypassed with a 200kΩ resistor to enable DC leakage testing to detect GOX damage. The discrete caps are placed at the critical path to the gate to capture the capacitive coupling effects. In total eleven different ESD protection topologies are investigated, out of which four circuit schematics (not showing supply-filter and power-clamp) are shown in Figure 1.

Each topology is a variant of "Basic." "NoCap," without capacitor and resistor in the RF line, connects GOX directly to pad. "2xAreaDiodes" has larger diodes (Y-size of active-diffusion increased to twice of Basic). "2xSecondStage" has second stage with twice the number of fingers as Basic. "NmosLkgOnly" has no resistor bypassing the cap in front of PMOS which allows detection of gate-oxide damage at NMOS. Table 1 summarizes the differences between the 11 ESD protection topologies.

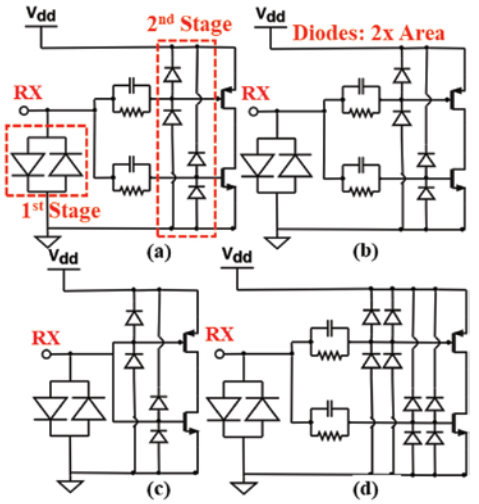


Figure 1: Investigated devices: (a) "Basic," (b) "2xAreaDiodes," (c) "NoCap," and (d) "2xSecondStage"

Name	Circuit Description
Basic	LNA circuit as shown in Fig. 1(a)
NoCap	Cap and resistor removed from RF line to GOX
2xAreaDiodes	Y-size of diode active-diffusion increased by 2x
2xSecondStage	2nd stage with 2x fingers as in *Basic*
SmallerPrimary	Primary diodes are reduced in width by one third
NMOSLkgOnly	Bypass resistor in front of PMOS removed
PMOSLkgOnly	Bypass resistor in front of NMOS removed
QuarterCap	Cap in RF line reduced to ¼ of value in *Basic*
NoSupplyCap	Supply filter cap removed
SupplyShort	VDD and VSS nets shorted
TcoilInductor	Inductor in the RF line in the 1st stage.

Table 1: Variants of the "Basic" circuit

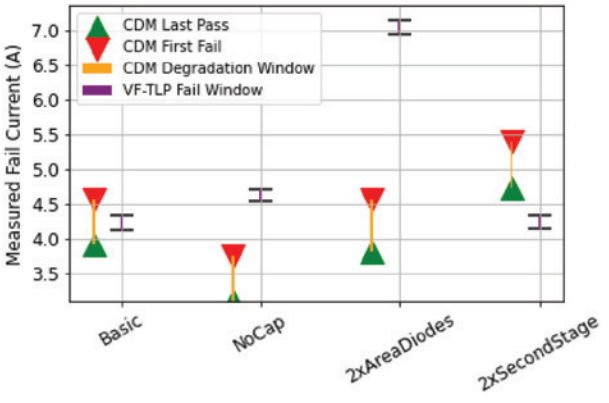


Figure 2: Comparison of CDM and VF-TLP results

Correlation of CDM with UF-TLP

For silicon verification of the simulation results, test circuits were placed on a wafer-level chip scale package (WL-CSP) to perform CDM test, on an Orion 2 CDM tester with a JS-002 compliant test head. The damage was detected by a DC sweep between pad and VSS. Wafer-level packages resulted in negligible variation in peak currents during CDM [5]. The UF- TLP measurements were obtained by stressing the same receiver circuits on wafer-level. For analysis, both TLP positive stress and CDM negative stress produce positive current (positive charge flowing into the device). During CDM test procedure, 10 zaps were performed on a single device where the maximum of 10 measured peak currents, was used for analysis after DC readout. In CDM, lowest fail current and highest pass current out of 10 stressed samples were selected as First-Fail and Last-Pass, respectively, for the CDM degradation window of each test structure.

During a CDM event the sensitive gate oxide connected to the pad in an LNA circuit is damaged by the fast rise time component of 20ps or less as shown in [2]. VF-TLP with 1ns pulse width and 100ps rise time shows no correlation with CDM test (shown in Figure 2) and thus, cannot

be used for predicting CDM robustness. Contrary to the expectation raised from the overestimation of the single LNA in [2], the CDM robustness can also be underestimated or show a "lucky" fit with the VF-TLP results, depending on the circuit.

Ultrafast (UF-)TLP with a rise time of 20ps and pulse duration of 0.6ns is performed. The difference between VF- and UF-TLP is best visible in the comparison of current waveform and voltage response (shown in Figure 3 and Figure 4) where methods caused breakdown of the receiver gate. The fast risetime of the current pulse during UF-TLP stress leads to a significantly higher voltage overshoot measured at the pad because of the turn-on time (forward recovery time) of the diode protection. Comparing both current waveforms,

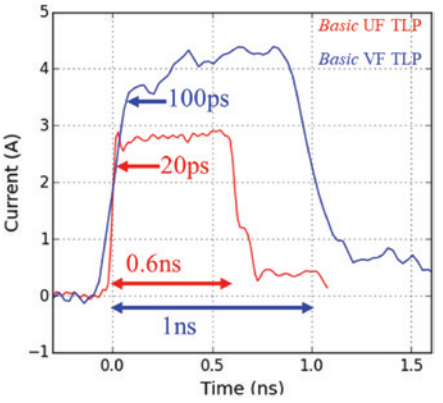


Figure 3: Comparison of VF-TLP and UF-TLP current waveforms

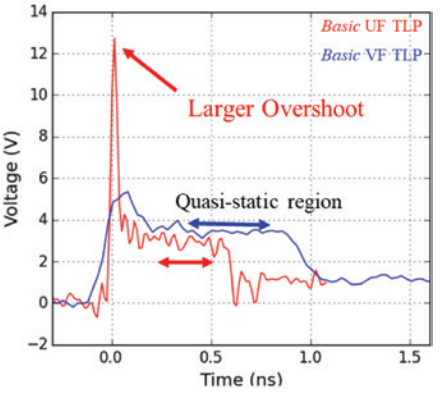


Figure 4: Comparison of VF-TLP and UF-TLP voltage response

the injected current with smaller magnitude and shorter pulse (UF-TLP) has damaged the victim GOX due to larger peak voltage.

Investigation of the same ESD protection circuits with UF-TLP shows better correlation, even though the UF-TLP underestimates the CDM robustness consistently by 0.5-1 A fail current, see Figure 5. This indicates that the rise time of the CDM pulse is slightly slower. In terms of the design robustness the worst-case assessment by UF-TLP is appropriate. With UF-TLP, the test structures have a range of fail currents because of the statistical nature of GOX breakdown.

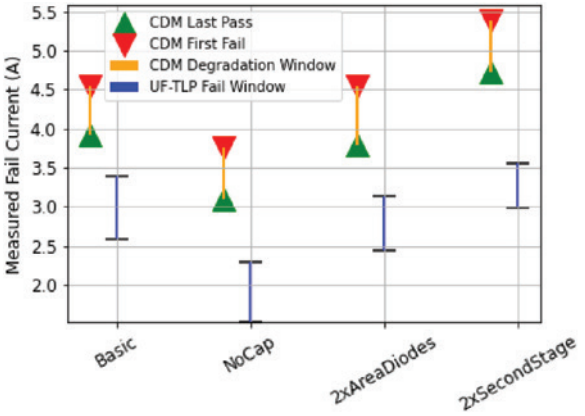


Figure 5: Comparison of CDM and UF-TLP measurement results

Calibration of Schematic with TLP

To accurately model the circuits under a CDM event, we incorporated the parasitics of interconnect. Resistance of the primary ESD paths including branch-point resistance and resistance to the victim, were extracted using a PathFinder-based extraction tool [5]. The inductance of metallization was estimated using 0.3pH/μm rule on measured length of highest metallization from primary diodes to supply/ground bump [8]. Interconnect parasitics are shown as blue instances in Figure 6. Diode models were also improved for fast and large currents during CDM discharge by involving intrinsic resistance and forward recovery inductance of the diode. These were extracted from diode's UF-TLP measurements and are shown as red instances in Figure 6. Intrinsic resistance is extracted from the ratio of quasi-static voltage to quasi-static current after diode turns-on during UF- TLP. Forward recovery inductance is extracted from the ratio of initial voltage overshoot to the rate of change of current (di/dt) during UF-TLP. These guidelines were used for modifying schematics, as shown in Figure 6, for all eleven ESD protection circuits.

Transient simulation was performed to check validity of interconnect parasitics and enhanced diode modelling. Rectangular current pulse, with 20ps risetime, was used as stimulus between RX pad and ground of the circuit "NoCap." Shown in Figure 7, UF- TLP simulation and measurement results of "NoCap" are compared on a TLP IV plot which produced some surprising results. In this quasi-static

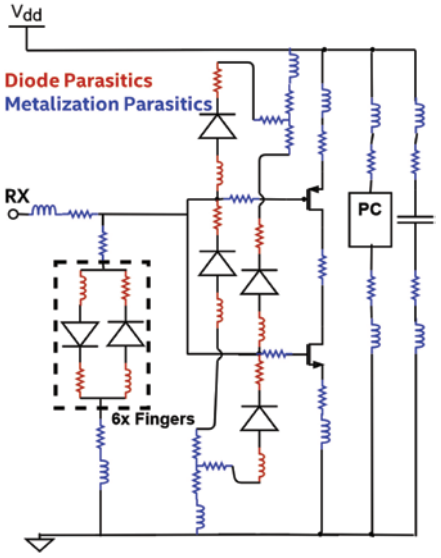


Figure 6: Modified NoCap schematic

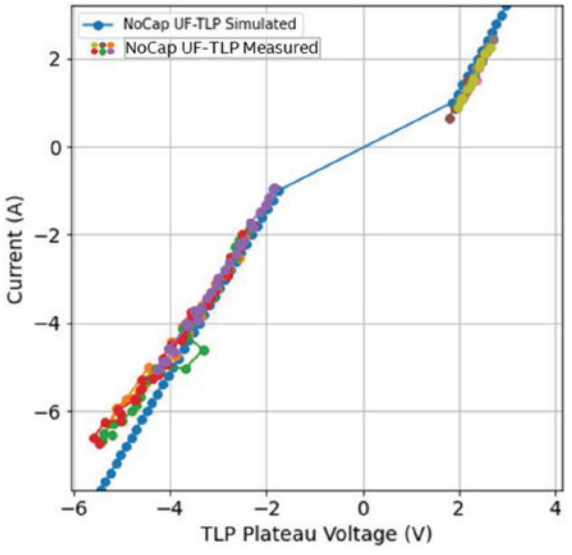


Figure 7: Simulated plateau voltage at bump/pad

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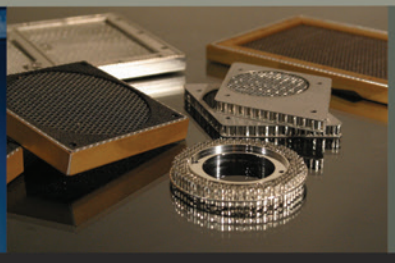

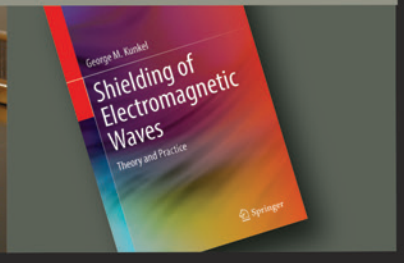

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region, the simulated voltage response fits well to the measured voltage response for different input currents. This validates resistive modelling and shows that the resistance extraction tool produced accurate path resistance values.

In Figure 8, a good match is shown between the simulated RX peak voltage and the measured pad peak voltage noted from voltage pulse corresponding to the UF-TLP current pulse at failure of the circuit. The vertical spread of blue inverted triangles corresponds to slight variation in failure currents due to statistical nature of GOX breakdown between samples. Simulation was performed with the measured failure currents and peak voltage plotted as red circle. The match between simulation and measurements provides confidence in the quality for the retrofit of the inductance values. Please note that due to topology of the presented circuits, significant amount of CDM current flows through the primary ESD stage so the peak voltage is dominated by its parasitics. This also indicates negligible contribution of the power clamp ESD path to the peak voltage at the pad.

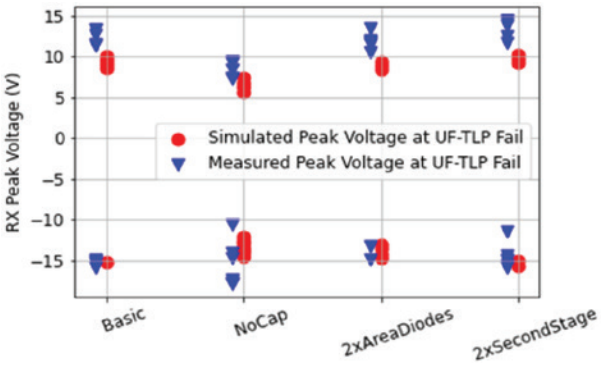

Figure 8: Peak voltages at UF-TLP failure currents

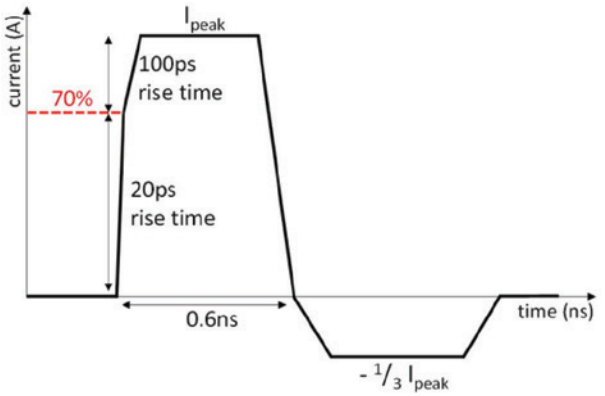

Figure 9: Current pulse for predictive CDM simulation

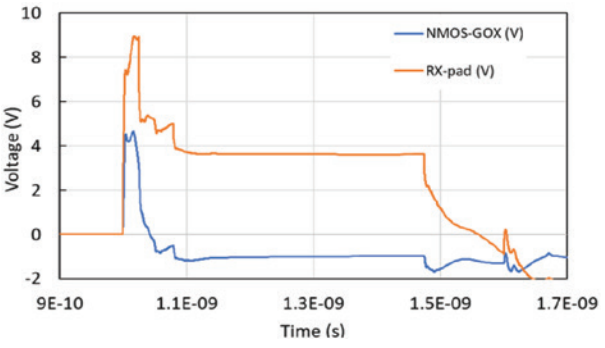

Figure 10: Voltage pulses during CDM simulation

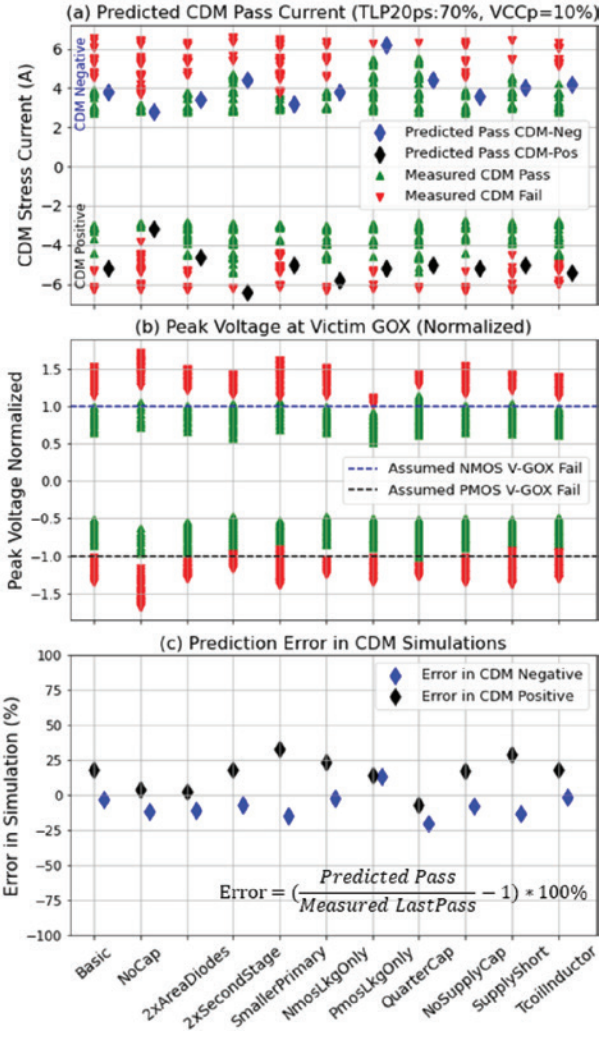

Figure 11: Comparison of CDM simulation and measurement results (a) simulated peak voltage across GOX (b) and prediction error in CDM simulation (c)

A novel CDM simulation approach involving current-force transient simulation with 20ps rise time component in the CDM current pulse has been shown to predict CDM failure.

CDM SIMULATION SETUP

The fast rise time component in the CDM pulse originates from the initial spark discharge of the pogo pin stray capacitance and only contributes a part of the full peak current of the CDM pulse in the initial phase of the waveform, this has been proved by measurement and simulation in [2]. Distribution of the first 70% of the full CDM peak with 20ps rise time and the last 30% peak with a rise time of 100ps is chosen for the CDM simulation in this study as according to the CC-TLP study in [2], it predicts the failure of LNA circuit correctly.

The VSS network is relatively large, in terms of area, compared to the VDD network in our test structures. Considering the ratio, we assumed distribution of CDM relevant change of 10% on the VDD network and 90% of the charge on the VSS network. The CDM charge sources are simulated as current sources where the current source between pad and VSS rail contributes 90% of the current and the second current source between pad and supply rail adds 10% to the CDM current at the pad. The current waveform, shown in Figure 9, is used as current force into RX during transient analysis of circuit, as shown in Figure 6, in SPICE simulation. The maximum voltage across GOX of the victim from the voltage pulse in Figure 10, is compared it to the oxide breakdown voltage as the failure criteria.

CDM SIMULATION RESULTS

For CDM simulation, different Ipeak current pulses, having same characteristics as shown in Figure 9, were generated and distributed between the VSS and the VDD net. Experimentally assessed P/NMOS GOX breakdown voltages, were used as a fitting-parameter (GOX breakdown uncertainty) to predict the breakdown current of the different LNA variants. The stronger victims with higher breakdown voltages, PMOS in CDM-negative and NMOS in CDM-positive, were disregarded during evaluation. The voltage failure criterion is indicated by the dashed line in Figure 11b and corresponds to NMOS (inversion) in CDM-negative and PMOS (accumulation) in CDM-positive. For measured CDM currents, the legend is common between Figure 11a and Figure 11b. CDM simulation was performed with the recorded CDM-Pass and CDM-Fail peak currents which are shown in Figure 11a. For each case, the peak voltage across GOX is plotted in Figure 11b. These values have been normalized by the corresponding MOS GOX breakdown voltage. Figure 11b clearly shows that the method evaluates and differentiates between CDM-Pass and CDM-Fail based on GOX breakdown. The criterion is chosen to minimize the error in predicted pass-current of all investigated structures, shown in Figure 11a. Shown in Figure 11c, is the CDM prediction inaccuracy for each test-structure which has been calculated using the data from Figure 11a. The term *Measured LastPass* refers to the highest measured peak discharge current during CDM stress where the structure survived or did not show any degradation in the post-stress DC evaluation. CDM prediction average inaccuracy is ~10% for the negative and ~15% for the positive.

SUMMARY

A novel CDM simulation approach involving current-force transient simulation with 20ps rise time component in the CDM current pulse has been shown to predict CDM failure. Initial 20ps rise time provides a much better prediction of the CDM failure level due to GOX breakdown of MOSFET device in the receiving circuit than the classical approach with assumption of a 100ps risetime pulse. The importance of interconnect parasitics and diode modelling during CDM simulations has also been highlighted. The methodology has been proven for a set of 11 ESD protection circuits, different topologies with gate-at-pad designs, in a state-of-art technology.

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PRODUCT Showcase

SMITH CHART AND VOLTAGE STANDING WAVE RATIO

By Bogdan Adamczyk

This article explains how to use a Smith Chart to determine the voltage standing wave ratio (VSWR). The concept of the standing waves and VSWR was described in detail in [1], while the Smith Chart construction and its use for determining the input impedance to the transmission line was discussed in [2,3,4].

Let's briefly review these concepts to provide the background needed for determining the VSWR graphically using a Smith Chart. Consider the transmission line circuit shown in Figure 1. A sinusoidal voltage source $\hat{V}_S$ with its source impedance $\hat{Z}_S$ drives a lossless transmission line with characteristic impedance Z_C, terminated in an arbitrary load $\hat{Z}_L$.

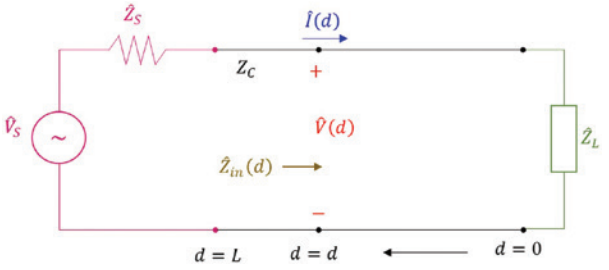

Figure 1: Transmission line circuit

In this model, the load is located at $d = 0$, and the source is located at $d = L$. The magnitudes of the voltage and current at a distance d away from the load are [1]

$$\left|\hat{V}(d)\right| = \left|\hat{V}^+\right|\left|\left[1 + \hat{\Gamma}_L e^{-j2\beta d}\right]\right| \tag{1a}$$

$$\left|\hat{I}(d)\right| = \left|\frac{\hat{V}^+}{Z_C}\right|\left|\left[1 - \hat{\Gamma}_L e^{-j2\beta d}\right]\right| \tag{1b}$$

where $|\hat{V}^+|$ denotes the amplitude of the forward propagating voltage wave, β is the phase constant, related to the wavelength, λ, by

$$\beta = \frac{2\pi}{\lambda} \tag{2}$$

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and $\hat{\Gamma}_L$ the load reflection coefficient given by

$$\hat{\Gamma}_L = \frac{\hat{Z}_L - Z_C}{\hat{Z}_L + Z_C} \tag{3}$$

A sample plot of the voltage and current magnitudes is shown in Figure 2.

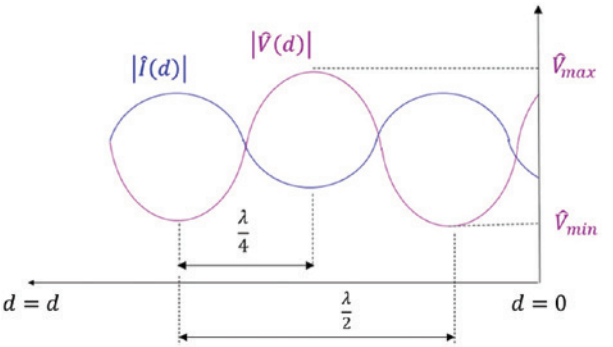

Figure 2: Magnitudes of the voltage and current for an arbitrary load

Except for the case of a matched load, the magnitudes of the voltage and current vary along the line. This variation is quantitatively described by the voltage standing wave ratio (VSWR) defined as

$$VSWR = S = \frac{\left|\hat{V}_{max}\right|}{\left|\hat{V}_{min}\right|} \tag{4}$$

When the load is short-circuited or open-circuited, $|\hat{V}_{min}| = 0$, and

$$S = \begin{cases} \infty & \hat{Z}_L = 0 \\ \infty & \hat{Z}_L = \infty \end{cases} \quad (5)$$

When the load is matched, we have

$$S = 1,\ \hat{Z}_L = Z_C \quad (6)$$

In general,

$$1 \le S \le \infty \quad (7)$$

VSWR can also be expressed in terms of the magnitude of the load reflection coefficient as

$$S = \frac{1+|\hat{\Gamma}_L|}{1-|\hat{\Gamma}_L|} \quad (8)$$

Let's return to the load reflection coefficient. Being a complex quantity, it can be expressed either in polar or rectangular form as

$$\hat{\Gamma} = \Gamma e^{j\theta} = \Gamma_r + j\Gamma_i \quad (9)$$

If we create a complex plane with a horizontal axis Γ_r and a vertical axis Γ_i, then the load reflection coefficient will correspond to a unique point on that plane, as shown in Figure 3.

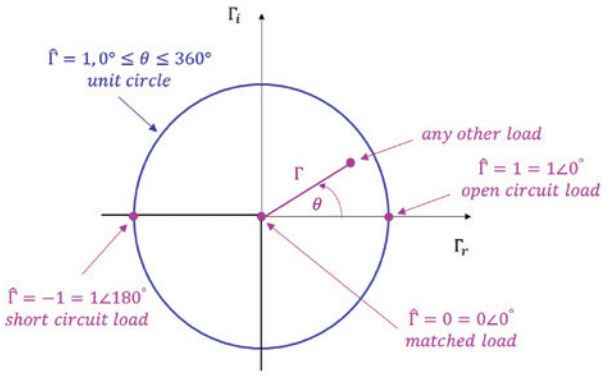

Figure 3: Load reflection coefficient and the complex Γ plane

The magnitude of the load reflection coefficient is plotted as a directed line segment from the center of the plane. The angle is measured counterclockwise from the right-hand side of the horizontal Γ_r axis.

For passive loads, the magnitude of the load reflection coefficient is always

$$0 \le \Gamma \le 1 \quad (10)$$

Figure 4 shows a Smith Chart with the circle (not a unit circle) centered at the origin of the complex plane.

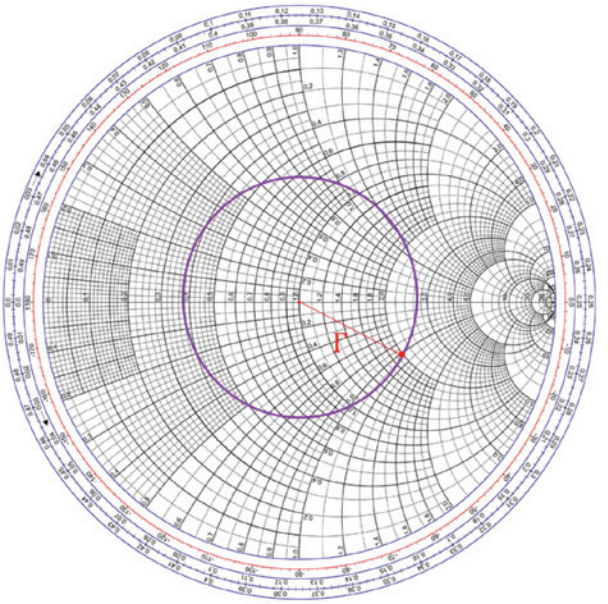

Figure 4: Smith Chart and the magnitude of the load reflection coefficient

All points on this circle have the same value of $|\hat{\Gamma}_L| = \Gamma$. Thus, this is a constant Γ circle. Now, recall Eq. (8), repeated here

$$S = \frac{1+\Gamma}{1-\Gamma} \quad (11)$$

or, equivalently,

$$\Gamma = \frac{S-1}{S+1} \quad (12)$$

Since Γ is constant, all points on this circle will have the same value of S. Thus, this is also a constant VSWR circle. To determine the value of S, we proceed as follows [5].

Consider a load with the normalized load impedance [2]

$$\hat{z}_L = 2 + j1 \tag{13}$$

represented by point *A* in Figure 5.

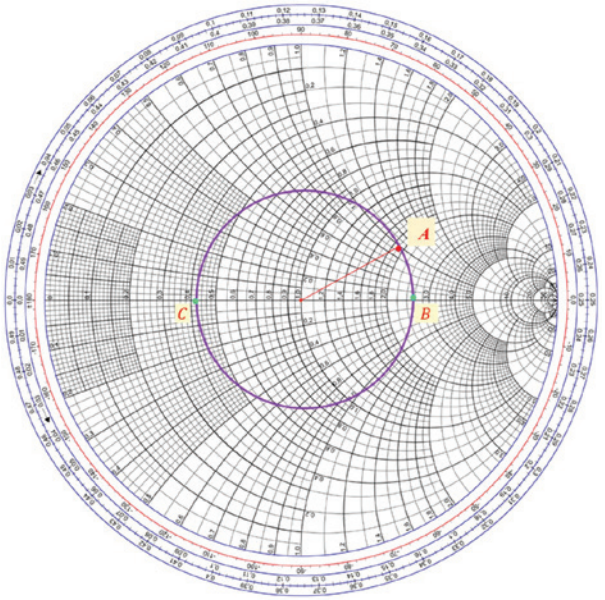

Figure 5: Smith Chart and the constant S circle

Let's draw a constant *S* circle passing through point *A*. This circle intersects the real Γ_r axis at two points, *B* and *C*. At both points, we have

$$\Gamma_i = 0,\ \Gamma = \Gamma_r \tag{14}$$

Since both points, *B* and *C*, lie on the real axis, the imaginary part of the normalized load impedance at those points is zero.

$$\hat{z}_L = r_L + jx_L = r_L \tag{15}$$

Now, the load reflection coefficient in Eq. (3) can be expressed in terms of the normalized load impedance as [2]

$$\hat{\Gamma}_L = \frac{\hat{z}_L - 1}{\hat{z}_L + 1} \tag{16}$$

Utilizing Eq. (12) in Eq (13) we have

$$\hat{\Gamma}_L = \Gamma = \frac{r_L - 1}{r_L + 1} \tag{17}$$

Points *C* corresponds to $r_L < 1$ and point *B* corresponds to $r_L > 1$. Let's compare Eq. (17) with Eq. (11), repeated as Eq. (18).

$$\Gamma = \frac{S-1}{S+1} \tag{18}$$

This comparison reveals that at point *B*, r_L must be equal to the VSWR, as shown in Figure 6.

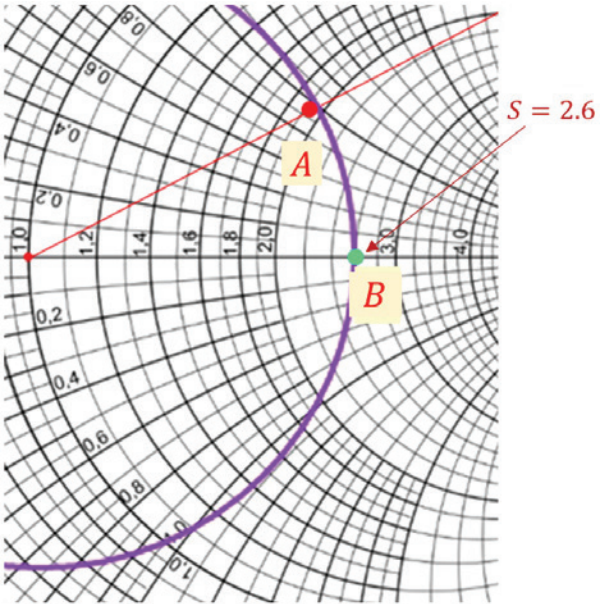

Figure 6: Smith Chart and the VSWR

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WHAT'S NEW IN ESD CONTROL STANDARDS?

By Wolfgang Stadler on behalf of EOS/ESD Association, Inc.

Standards continuously evolve, and EOS/ESD Association, Inc. standards are no different. Besides the routine five-year and ten-year review of standards (S), standard test methods (STM), and standard practices (SP), documents on new topics in the field of electrostatic control, electrostatic discharge (ESD) testing and characterization, electrical overstress (EOS), and ESD design and modeling are developed and published by more than thirty working groups (WGs). From 2021 to the beginning of 2024, approximately 30 documents have been reaffirmed, revised, or newly released. Slightly more than half of these documents address ESD control topics, some of which are covered in this short overview article. A second article will cover the new developments in ESD and EOS test and characterization and ESD design and modeling documents.

Wolfgang Stadler is an ESD expert at Intel Germany Services GmbH. He focuses on ESD protection, assessment, and control programs for Intel's Product Business Groups. Stadler holds multiple patents, has authored over 120 papers, and co-authored a book on ESD simulation. He's active in industry associations, teaches ESD courses, and received the EOS/ESD Association's Outstanding Contribution Award in 2019. He's also president of the German ESD FORUM e.V.

The central document on ESD control is *ANSI/ESD S20.20 – ESD Association Standard for the Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment.* This standard defines the limits of ESD control items and ESD control measures. ANSI/ESD S20.20 refers to several standards and STMs defining the test methods for ESD control items, such as ESD-control flooring, seating, packaging, etc., and ESD control measures, such as personnel grounding (see Figure 1). Furthermore, it references the technical report (TR) *ESD TR53 – ESD Association Technical Report for the Protection of Electrostatic Discharge Susceptible Items – Compliance Verification of ESD Control Items* for all requirements on compliance verification. The new version of ANSI/ESD S20.20 was released at the end of 2021, and, consequently, ESD TR53 as a "companion document" was updated slightly later in May 2022 to align with the new version of ANSI/ESD S20.20. The second companion document of ANSI/ESD S20.20, *ESD TR20.20 – ESD Association Handbook for the Development of an Electrostatic Discharge Control Program for the Protection of Electronic Parts, Assemblies, and Equipment,* is currently being updated to address the comments received during the review processes of ANSI/ESD S20.20.

The major technical changes in ANSI/ESD S20.20 include requirements on product qualification, the assessment of the risk by process-essential insulators, which now adds the measurement of the

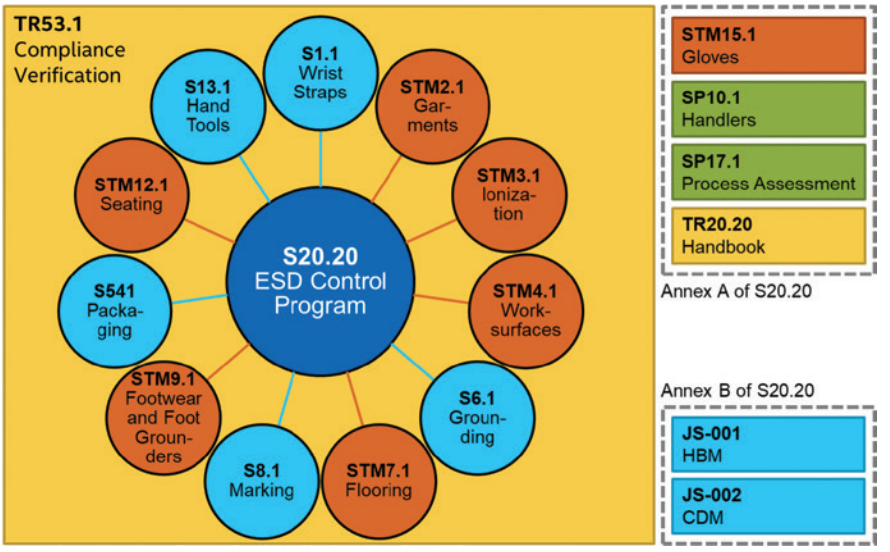

Figure 1: ESD Association Documents Referenced in ANSI/ESD S20.20

electrostatic field at the location where the ESD-sensitive (ESDS) item is handled as an alternative test method. Additionally, a new section was added to the United States Department of Defense (DoD) packaging requirements per a request from the DoD to support the withdrawal of Mil-STD 1686. *ANSI/ESD STM4.2 – ESD Association Standard Test Method for the Protection of Electrostatic Discharge Susceptible Items – ESD Protective Worksurfaces – Charge Dissipation Characteristics* was removed as a qualification method for worksurfaces as this test method was withdrawn due to a lack of commercially available test equipment. A separate article will discuss all relevant changes in ANSI/ESD S20.20 and the compliance verification document ESD TR53.

In Annex A, ANSI/ESD S20.20 provides guidance and outlines documents available to help the users evaluate additional control products and equipment, such as *ANSI/ESD SP17.1 – ESD Association Standard Practice for the Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques*. This newly developed standard practice describes a set of methodologies, techniques, and tools that can be used to characterize a process where ESDS items are handled. This document aims to identify whether potentially damaging ESD events are occurring or if significant electrostatic charges are generated on personnel, equipment, materials, or devices – even though there is a static control process in place (for example, ANSI/ESD S20.20). It can be used to assess whether devices of a given ESD robustness can be handled safely in the process, improve ESD capabilities if required or desired, or save money by reducing ESD control measures. ANSI/ESD SP17.1 addresses some challenges of current ESD control programs, such as the assessment of automated handling equipment (AHE), the use of ESD-sensitive items with an ESD robustness lower than defined in ANSI/ESD S20.20, that is 100 V against Human Body Model (HBM), 200 V against Charged Device Model (CDM), and 35 V against isolated conductors. Obviously, increasing I/O bandwidth and new packaging techniques such as die-to-die or wafer-to-wafer can lead to significantly reduced ESD robustness; process assessment is a crucial tool to ensure safe handling of ESD-sensitive items.

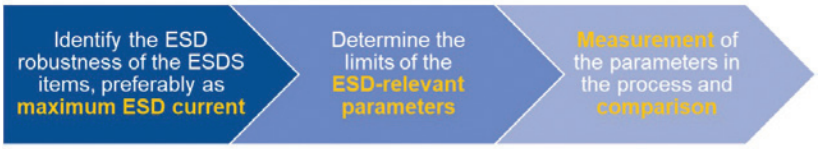

Figure 2: Basic Approach to Perform ESD Risk assessment According to ANSI/ESD SP17.1

The flows and measurement methodologies of ANSI/ESD SP17.1 can also be used for "troubleshooting."

The document suggests ESD risk assessment flows in processes for ESD risks due to charged personnel, conductors, charged ESDS items, and insulators. Additionally, a simple assessment flow is described using ESD event detection methods. The document's annex describes ESD measurement techniques typically used for ESD risk assessment. The overall approach for an ESD risk assessment with the framework of ANSI/ESD SP17.1 is shown in Figure 2. A *sine qua non* condition for a successful ESD risk assessment is a detailed understanding of the process and the potential ESD risks. Questions to be answered in preparation for the ESD risk assessment are, for example, whether there is a "critical" contact to the ESD-sensitive item in the process, that is, a metal-to-metal contact to the ESD-sensitive item. If potentially critical contacts are identified, the first step is to clarify the ESD robustness of the ESDS item in the process. The relevant parameter for the ESD robustness is the ESD withstand *current*; guidance is given in the document on how to come to the ESD withstand current even if "only" ESD qualification data with a withstand voltage are known. As the withstand current can rarely be measured in the process, limits for other ESD-relevant parameters such as the charging (voltage) in the process, the contact resistance of the object enabling the ESD-sensitive item to discharge or electrostatic fields have to be derived from the ESD withstand current. Finally, those parameters must be measured in the process and compared with the limits.

Without question, ANSI/ESD SP17.1 is already a very important document today, and its importance will continue to grow in the future with lower ESD robustness. However, the procedures in this document are not simple and are for use by personnel possessing advanced knowledge and experience with electrostatic measurements. Also, interpreting the results from the

measurements described in this document requires significant experience and knowledge of the physics of ESD and the process. ESDA WG17 is working on documents and training materials with examples of applying the methodology and the measurement methods to processes in different applications.

Another ESDA document that addresses a new topic is *ESD TR19.0-01 – ESDA Technical Report for the Development of an Electrostatic Discharge Control Program for Protection of High-Reliability Electrical and Electronic Parts, Assemblies, and Equipment*. This document discusses best practices for defining, establishing, implementing, and maintaining an ESD control program for electronic items in high-reliability applications. High-reliability electronic items are defined in this document as items that serve functions where failures can have catastrophic effects, such as flight-critical, space, critical communication, weapons, and medical device/life science systems. This TR is intended to be used with ANSI/ESD S20.20 and to provide supplemental information and guidance on reducing risk when handling high-reliability electronic parts, assemblies, and equipment. ESDA WG19 has started developing an SP for an ESD control program for high-reliability electronic parts.

The oldest ESDA document, *ANSI/ESD S1.1 - ESD Association Standard for the Protection of Electrostatic Discharge Susceptible Items – Wrist Straps,* received minor updates in the 2021 release. There are no major developments in wrist straps; therefore, the changes are more editorial, such as aligning the units to the metric or SI system (for example, giving the break-away force now in N (Newton) instead of kg). Some figures have been added for clarity, and an alternative test method for the wrist strap continuity and resistance test is now included.

ANSI/ESD STM7.1 – ESD Association Standard Test Method for the Protection of Electrostatic Discharge Susceptible Items – Flooring Systems – Resistive Characterization changed its title from "Flooring Material" to "Flooring System" to highlight that the test is applied to a system of materials combined to make the flooring system and that those materials' interactions can affect the overall resistance measured. The definition of conductive flooring is now changed from previously "less than or equal to 1.0×10^6 ohms" to now "less than 1.0×10^6 ohms", and consequently, the definition of dissipative flooring from previously "greater than 1.0×10^6 ohms" to now "greater than or equal to 1.0×10^6 ohms and less than 1.0×10^9 ohms" – which has no practical implication. This is explained in a new Annex. As in all document revisions, boilerplate statements such as the definition of the meter have been updated.

ANSI/ESD STM9.1-2022 – ESD Association Standard Test Method for the Protection of Electrostatic Discharge Susceptible Items – Footwear and Foot Grounders – Resistive Characterization is now a consolidated document of ANSI/ESD/ESD STM9.1-2014 which addressed footwear and ANSI/ESD SP9.2-2019 which defined resistance test methods for foot grounders. Technically, the test methods for both footwear and foot grounders have not been changed.

The ESDA is always striving to achieve the highest quality standards. One important aspect is the alignment of verbiage and requirements amongst the different ESD standards. The ESDA's Manufacturing Ad-hoc Task team is working continuously to harmonize the ESD control standards. A minimum set of reporting requirements is defined and will be included in all revised standard documents. Recommendations on equipment calibration and verification, together with simple verification methods, will be added to new documents. All compliance verification tests have now been removed from standards and standard test methods and moved to ESD TR53 as a single source of compliance verification tests. There is no longer a requirement to qualify ESD control items at moderate humidity; it is sufficient to perform qualification tests under the most critical low-humidity condition at 12% ± 3% relative humidity and 23 °C ± 3 °C. The only exception is *ANSI/ESD STM11.31 – ESD Association Standard Test Method for Evaluating the Performance of Electrostatic Discharge Shielding Materials – Bags* ("shielding bag test"), for which a higher relative humidity is critical. You will see those changes in the next revisions of the documents.

Founded in 1982, EOS/ESD Association, Inc. is a not-for-profit, professional organization dedicated to education and furthering the technology of Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, and tutorials, and fosters the exchange of technical information among its members and others.

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