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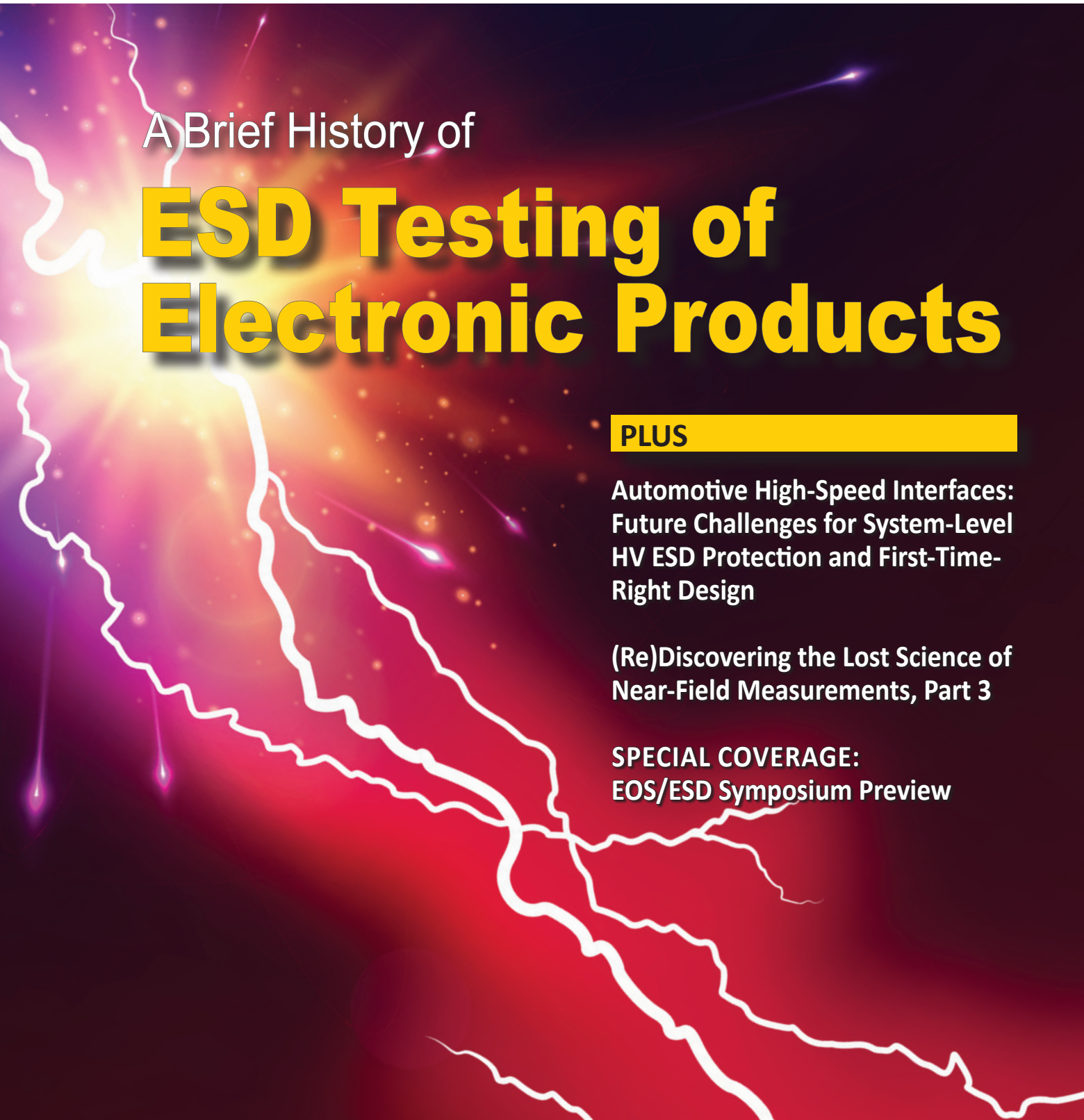

A Brief History of

ESD Testing of Electronic Products

PLUS

Automotive High-Speed Interfaces: Future Challenges for System-Level HV ESD Protection and First-Time-Right Design

(Re)Discovering the Lost Science of Near-Field Measurements, Part 3

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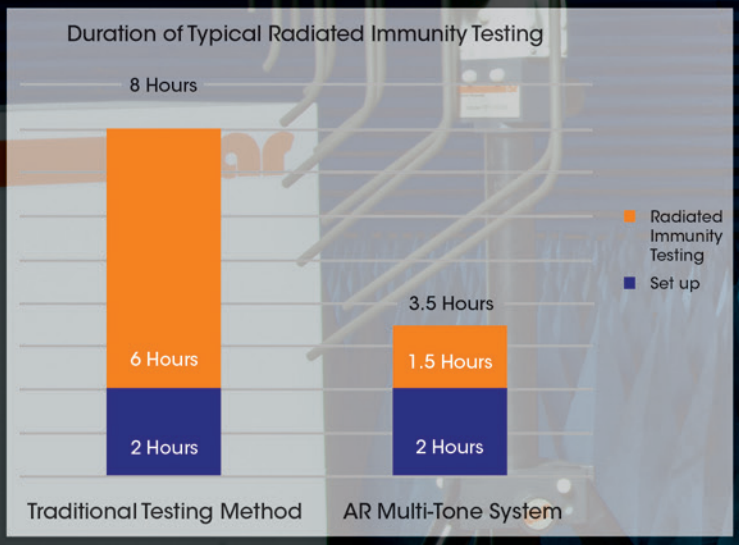

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FCC Proposes More Power Flexibility for FM Stations

The U.S. Federal Communications Commission (FCC) is taking steps to provide certain FM radio stations with more flexibility to increase digital power levels for their operations.

The Commission's Order and Notice of Proposed Rulemaking (NPRM) proposes to change the way FM stations determine their maximum permissible power level and, further, to give FM stations the authority to operate their digital sidebands at different power levels. According to the FCC, these changes would potentially expand the number of FM stations that can broadcast at higher digital power levels, while also giving them greater flexibility to maximize power while avoiding interference.

The Commission Order and NPRM were prompted by two petitions filed with the Commission, the first in 2019 by the National Association of Broadcasters (NAB), Xperi Corporation, and National Public Radio, and the second in 2022 by the NAB and Xperi.

The FCC says that there are currently over 2000 FM stations that broadcast digitally, providing listeners with enhanced sound quality and other data through digital signals. If the FCC's Order and NPRM are adopted, the Commission says that the changes would potentially encourage more FM broadcasters to adopt digital technologies, thereby making digital broadcasts available to a greater number of listeners.

FCC Proposes $20 Million Penalty for Failing to Protect Consumer Data

The U.S. Federal Communications Commission (FCC) has proposed a $20 million fine against two affiliated wireless companies for failing to adequately secure and protect the personal data of subscribers.

According to a Notice of Apparent Liability for Forfeiture, the companies, Q Link Wireless LLC, and Hello Mobile Telecom LLC, routinely relied on readily available biographical and account information to authenticate online customers. Customers authenticated in this way were then given access to "customer proprietary network information" (CPNI), placing customer information at risk of unauthorized access and disclosure.

FDA Updates List of Recognized Standards

The U.S. Food and Drug Administration (FDA) has updated its list of recognized international and national standards that can be used to demonstrate compliance with certain requirements for premarket review and authorization of medical devices.

In a Notice published in the *Federal Register*, the agency announced 29 additions and 25 modifications to the list of FDA Recognized Consensus Standards. Notable among the new standards added to the list are ISO 60601-2-35, which details requirements for the safety and performance of heating devices, and IEC 810001-5-1, which addresses the security in the product lifecycle of health software and health IT systems. Also newly added to the list of recognized standards is ISO/TS 11137-4, which addresses process control on the use of radiation in the sterilization of healthcare products.

FCC Backs U.S. Cybersecurity Labeling Program for Smart Devices

The U.S. Federal Communications Commission (FCC) is reportedly moving ahead with plans to develop and implement a voluntary labeling program for connected smart devices that meet rigorous cybersecurity requirements.

In remarks presented at the White House in Washington, DC, FCC Chair Jessica Rosenworcel announced that she has presented to the Commission a proposal to launch the first-ever voluntary "U.S. Cyber Trust Mark" Program. The proposed program, which would qualify connected smart devices to bear the Cyber Trust Mark, would help consumers to identify secure products while also creating incentives for device manufacturers to meet rigorous cybersecurity standards.

"Just like the 'Energy Star' logo helps consumers know what devices are energy efficient, the Cyber Trust Mark will help consumers make more informed decisions about device privacy and security," Rosenworcel noted. "What's more, because we know devices and services are not static, we are proposing that along with the mark we will have a QR code that provides up-to-date information on that device."

Rosenworcel said that the proposed Cyber Trust Mark Program is based on extensive work by the U.S. National Institute of Standards and Technology (NIST) to develop criteria for cyber secure devices.

Unintended Satellite Emissions May Interfere with Radio Astronomy

In the 21st century, we rely more and more on earth-orbiting satellites to support communications technologies here on the ground. But scientists are now discovering a potential problem with satellite emissions that may warrant attention.

A recent article posted to the *Sky & Telescope* website provides an overview of recent research conducted by space experts at the Max-Planck Institute for Radio Astronomy in Germany and other institutions associated with the Square Kilometre Array Observatory. According to the article, researchers looked for radio signals from satellites in SpaceX's Starlink fleet. Of the 68 satellites they observed, they detected radio emissions from 47 satellites in the 110-188 MHz frequency spectrum, well below the 10.7-12.7 GHz signals used for downlink communication signals from the satellites. The leaked signals detected by the researchers are stronger than those allowed under current regulatory limits, but current limits apply only to intentional emissions, with no stated limits applicable to unintentional emissions.

The obvious challenge for researchers, according to the article, is the additional time required to eliminate from their research data that may have been contaminated by the unintentional emissions. But the potentially larger issue is that weaker signals that hide under the underlying noise might lead to incorrect research assumptions and results.

Researchers say that the unintended emissions problem is not limited to Starlink satellites, but instead is a potential issue for each of thousands of the satellites that operate in earth orbits. This significantly raises the risk that the operation of ground-based radio telescopes will be impacted.

The solution, according to the researchers, is for scientists and industry to actively work together to develop effective mitigation strategies, while also campaigning for regulatory changes that address the root cause of the problem.

A BRIEF HISTORY OF ELECTROSTATIC DISCHARGE (ESD) TESTING OF ELECTRONIC PRODUCTS

Revisited and Revised as of 2023

Daniel D. Hoolihan is the founder and principal of Hoolihan EMC Consulting. He is the Immediate Past-Chair of the American National Standards Committee C63 on EMC. He is also a past president of the IEEE's EMC Society and the current Chair of the History Committee of the Society's Board of Directors. Hoolihan is also an assessor for the NIST NVLAP EMC and Telecom Laboratory Accreditation program. He can be reached at danhoolihanemc@aol.com.

By Daniel D. Hoolihan

With the inventions of the transistor in 1947 and the integrated circuit in 1958, and the utilization of these major solid-state breakthroughs in the development of computers and other electronic devices, industry began to worry about designing components and end-products that could survive the impact of electrostatic discharges to chips, printed circuit boards, and final packaged-products. The 1960s and 1970s saw individual companies developing their own ESD test values and laboratory test techniques. The International Electrotechnical Commission (IEC), which is closely related to the International Standards Organization (ISO), got involved in the 1980s with the release of IEC 801-2 in 1984 on ESD limits and susceptibility test methods. Since the late 1980s, most electronic companies test their end-products for ESD immunity in accordance with the specifications found in IEC 801-2 and its follow-on standard, IEC 61000-4-2.

IN THE BEGINNING

The electrostatic discharge (ESD) phenomena have been known since the Greek civilization was dominant thousands of years ago. Experiments with glass rods and cloth material produced ESD sparks. And people in colder climates were very familiar with the ESD effect due to a low-relative humidity environment inside a building or house. They frequently experienced an ESD event as they walked across a carpet in the winter season.

As electronic components changed from electronic tubes to solid-state electronics in the 1950s, companies became concerned with the potential for physical damage to solid-state electronic components, interference to, and interruption of normal operation of electronic equipment. This article primarily addresses the latter of those two situations, that is, the interruption effects of ESD on packaged electronic equipment.

THE 1960S AND 1970S

Most electronic companies in the 1960s and 1970s were aware of and concerned about ESD. The companies tended to have proprietary standards and test methods on ESD and were not interested in exchanging information with their competitors on ESD.

The Human Body Discharge model was commonly used by companies to test products with an ESD tester. The capacitance of a human being was estimated to be in the 100 to 250 picofarad range depending on the size of the person and the length and shape of the human's shoes. A common discharge value for early standards was 5000 volts. The discharge resistance was often taken as 500 ohms, the resistance of the human finger. The discharge was an air-gap discharge that closely simulated the actual ESD phenomena.

There were some companies that were using a contact discharge approach to ESD where the ESD tester was in physical (metal-to-metal) contact with the electronic equipment. The contact discharge was a more repeatable method than the air discharge method. Oftentimes, thousands of contact discharges were used to simulate the effects of one event, and statistical analysis was used to determine pass or fail criteria for the ESD test.

The common joke among EMC consultants in the 1970s was about the correct magnitude of the ESD discharge. In most cases, companies started at a recommended 5 kilovolts amplitude. Then, when all products could pass that level, consultants would increase their recommendation to 7500 volts amplitude so they could continue to consult with the customer and improve the design of the product.

KANGAROO LEATHER

A United States computer company in the 1970s began experimenting with ESD relative to its computers and computer peripherals. A Van de Graaf generator, some high-voltage sources, and a green nylon carpet were all tried as potential ESD generators. After experimenting with the three options, it was decided to go with the standard green nylon carpet concept. A number of volunteers were organized and asked to shuffle their feet on the carpet in a controlled humidity environment while holding onto a scientific electrostatic voltmeter. Again, in most cases, at relative humidity levels of 10% and greater, about 5 to 7.5 kilovolts was the maximum value measured on the human subjects.

One product made by the computer company had a wide distribution in Australia, and it had ESD problems while the same product shipped to other countries had no ESD problems. An engineer from the company who worked with the Australian customers visited the EMC lab and discussed the issue with the EMC lab engineers. The engineers took the Australian engineer into the controlled environment and asked him to shuffle his feet while connected to the electrostatic voltmeter. Much to the EMC lab engineers' surprise, the voltmeter registered 18000 volts!

After some discussions with the Australian native, it was discerned that he had normal clothing on his body with the exception of his shoes which were made of kangaroo leather. Needless to say, the lab made that fact known while in parallel developing an engineering fix to its product to allow it to pass 18 kilovolts.

THE 1980S

The 1980s saw the release of the IBM Personal Computer in 1981, which legitimized the PC market and led the computer industry to develop desk-supported computers (desktop, laptop, etc.) and similar desk-based electronic products for the manufacturers of medical equipment, laboratory equipment, etc.) based on international standards to help ensure satisfactory ESD product performance.

IEC 801-2 - 1984

The first edition of International Electrotechnical Commission (IEC) Publication 801-2 was released in 1984. It was titled "Electromagnetic Compatibility for Industrial-Process Measurement and Control Equipment – Part 2: Electrostatic Discharge Requirements."

The standard carefully pointed out in a note that:

> *"From the technical point of view, the more precise term for this phenomenon would be 'static electricity discharge.' However, the term 'electrostatic discharge' (ESD) is widely used in the technical world and in technical literature. Therefore, it has been decided to retain the term ESD in the title."*

The characteristics of the ESD generator in the 1984 edition were: energy storage capacitor - 150 pF +/- 10%; discharge resistor – 150 ohms +/- 5%; and an output voltage of 2 kV to 16.5 kV (the output voltage was a positive voltage only!). The rise-time of the discharge current was 5 ns +/- 30% at 4 kV and the pulse width was approximately 30 ns +/- 30%. The test was an air-discharge test only.

The 1984 edition did have a requirement for discharging to the earth reference plane to simulate discharges to objects in the vicinity of the equipment under test (EUT).

Figure 5 of IEC 801-2 illustrated the "test set-up for table-top-mounted equipment, laboratory tests." There was no "ground reference plane" on the floor; instead, the "earth reference plane" was on top of the table and grounded to a mains terminal (earth connection) via a cable. The insulating support between the EUT and the earth reference plane was 10 cm (4 inches) thick.

SECOND EDITION OF IEC 801-2 – 1991

The second edition of IEC 801-2 was released in 1991. One of the major changes in the standard was that the contact discharge was the preferred test method and not the air discharge method.

The energy storage capacitor remained at 150 pF but the discharge changed to 330 ohms plus or minus 10%. The output voltage was increased to 8 kilovolts for contact discharge and 15 kilovolts for air discharge (both positive and negative pulses were mandated!). The rise-time at 4 kilovolts had decreased to 0.7 to 1 nanosecond. The values of the parameters of the discharge current had to be verified with a 1 GHz oscilloscope. The grounding cables from the newly

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implemented vertical coupling plane (VCP) and its complement, the horizontal coupling plane (HCP) to the ground reference plane, had 470-kiloohm resistors located at each end of the cables.

VERTICAL COUPLING PLANE (VCP)

A VCP is called out in modern-day ESD standards. The basis for the VCP is a metal filing cabinet (usually four-drawer) that was commonplace in the offices of industry. The ESD charge simulated an employee walking across a floor, touching the handle of the metal filing cabinet, and discharging ESD energy to the cabinet, which would then re-radiate the field from the side of the cabinet.

HORIZONTAL COUPLING PLANE (HCP)

The development of the HCP started with a well-known cash-register company in the 1970s. At that time, they had an air-discharge ESD gun which was used for their product development testing. The EMC engineers very cleverly developed an all-plastic cash register and the ESD gun would not discharge to the cash register. Therefore, by definition, the product passed the ESD test.

The all-plastic cash register went into production and out into the real world with real customers. One of the first buyers of the all-plastic cash register was a fast-food restaurant that used an all-metal countertop to separate the customers from the employee/kitchen area. When winter came, the customers would enter the restaurant and discharge an ESD event to the 3-meter-long metal countertop. The countertop would then re-radiate the ESD energy, affecting the all-plastic cash register's electronics and immediately opening the cash drawer. The fast-food restaurant company was not pleased and returned the all-plastic cash registers to the manufacturer.

The EMC engineers went back to work. They placed a metal ground plane under the all-plastic cash register and discharged to the metal ground plane (now known as the HCP) to simulate the real-life experience. They eventually came up with design fixes that allowed the all-plastic register to pass the ESD test.

FIRST EDITION OF IEC 1000-4-2

The follow-on standard to IEC 801-2-1991 was IEC 1000-4-2 – *International Standard on EMC – Part 4: Testing and Measurement Techniques – Section 2: Electrostatic Discharge Immunity Test – Basic EMC Publication*, which was released in 1995.

(Note: European regulators put a "6" in front of the "1000-4-2" and the International Community followed suit in the 1996 timeframe. So all the "IEC 1000" series standards became the "IEC 61000" series.)

The parameters of the ESD generator remained the same as those found in the 1991 IEC 801-2 standard; that is, the energy storage capacitor was 150 pF, the discharge resistance was 330 ohms, and the output voltage of 8 kV for contact discharge and 15 kV for air discharge. The polarity of the output voltages was both positive and negative.

Figure 5 ("Example of test set-up for table-top equipment, laboratory tests") from the 1995 version of IEC 1000-4-2 showed a horizontal coupling plane on the tabletop that was larger than the earth reference plane on top of the table in the1984 standard, a vertical coupling plane (unmentioned in the 1984 standard), a ground reference plane on the floor, and grounding cables between the HCP and VCP and the ground reference plane (with 470 kiloohm resistors on both ends of the grounding cables.) Note that the insulating support between the EUT and the horizontal coupling plane was only 0.5 mm thick, reduced from 10 cm (100 mm) thick in the 1984 edition.

Released in 1998, Amendment 1 of IEC 61000-4-2 (1000-4-2) modified the language in Figure 5 to read "Example of test set-up for table-top equipment tests."

Released in 2000, Amendment 2 of IEC 61000-4-2 (1000-4-2) added a new clause (7.1.3) – "Test Method for Ungrounded Equipment," which included 7.1.3.1 – "Table-Top Equipment," and 7.1.3.2 – "Floor-Standing Equipment." It also replaced three paragraphs in 8.3.1 ("Direct Application of Discharges to the EUT"). Finally, it replaced Clause 9 with a new Clause 9, and it added Clause 10 – "Test Report."

SECOND EDITION OF IEC 61000-4-2

The second edition of IEC 61000-4-2 was released in 2008 and it nullified and replaced the first edition published in 1995, as well as Amendment 1 (1998) and Amendment 2 (2000). The key parameters of the

Electrostatic discharge testing has evolved from a company-based reliability test in the 1960s and 1970s to a performance test on electronic products in the 2023 timeframe.

ESD generator remained constant at 150 pF for the energy storage capacitor and the discharge resistance was set at 330 ohms. The output voltage for contact discharge remained constant at the highest value of 8 kilovolts and the air discharge at 15 kilovolts. The amplitudes were quoted in both the negative and positive polarities.

AMERICAN NATIONAL STANDARDS COMMITTEE (ANSC) C63 ON EMC (C63 COMMITTEE)

The C63 Committee produced a guide to electrostatic discharge testing in 2016, American National Standards Institute (ANSI) - C63.16-2016 titled "American National Standard Guide for Electrostatic Discharge Test Methodologies and Acceptance Criteria for Electronic Equipment."

The Introduction to the Guide states:

"This guide is intended to provide supplemental information for performing electrostatic discharge (ESD) testing to other established ESD standards by including information and test procedures that are not covered in those documents. It strives to improve product quality through proper operation in actual equipment installations. The suggestions provided herein should not be construed as mandatory and they should not be applied arbitrarily to all types of electronic equipment. Performance or acceptance test levels are not given in this guide. The specification of performance or acceptance levels for any particular type of electronic equipment remains the responsibility of the manufacturer and the users of the particular equipment."

The Guide's Scope is:

"This guide provides electrostatic discharge (ESD) test considerations that a manufacturer should use in assessing the expected ESD effects on products in a wide range of environments and customer use. The focus is well beyond that used to simply show that a product complies with a local, regional, or international standard or regulation. The following are included: charged peripheral testing, connector pin testing, and details on the use of ESD simulators. Finally, suggestions for assuring the safety of those who apply the ESD discharge are provided. The annexes include information on test method selection and more background on air and contact discharge for those who want to further understand the differences in these methods. This guide is not applicable to manufacturing, service, or maintenance of equipment. Personnel who perform these activities should be trained to avoid ESD effects or damage to the equipment. In summary, this guide has test techniques beyond those that are commonly used (e.g., IEC 61000-4-2), and hence it can be a significant tool for increasing the immunity of products to ESD events."

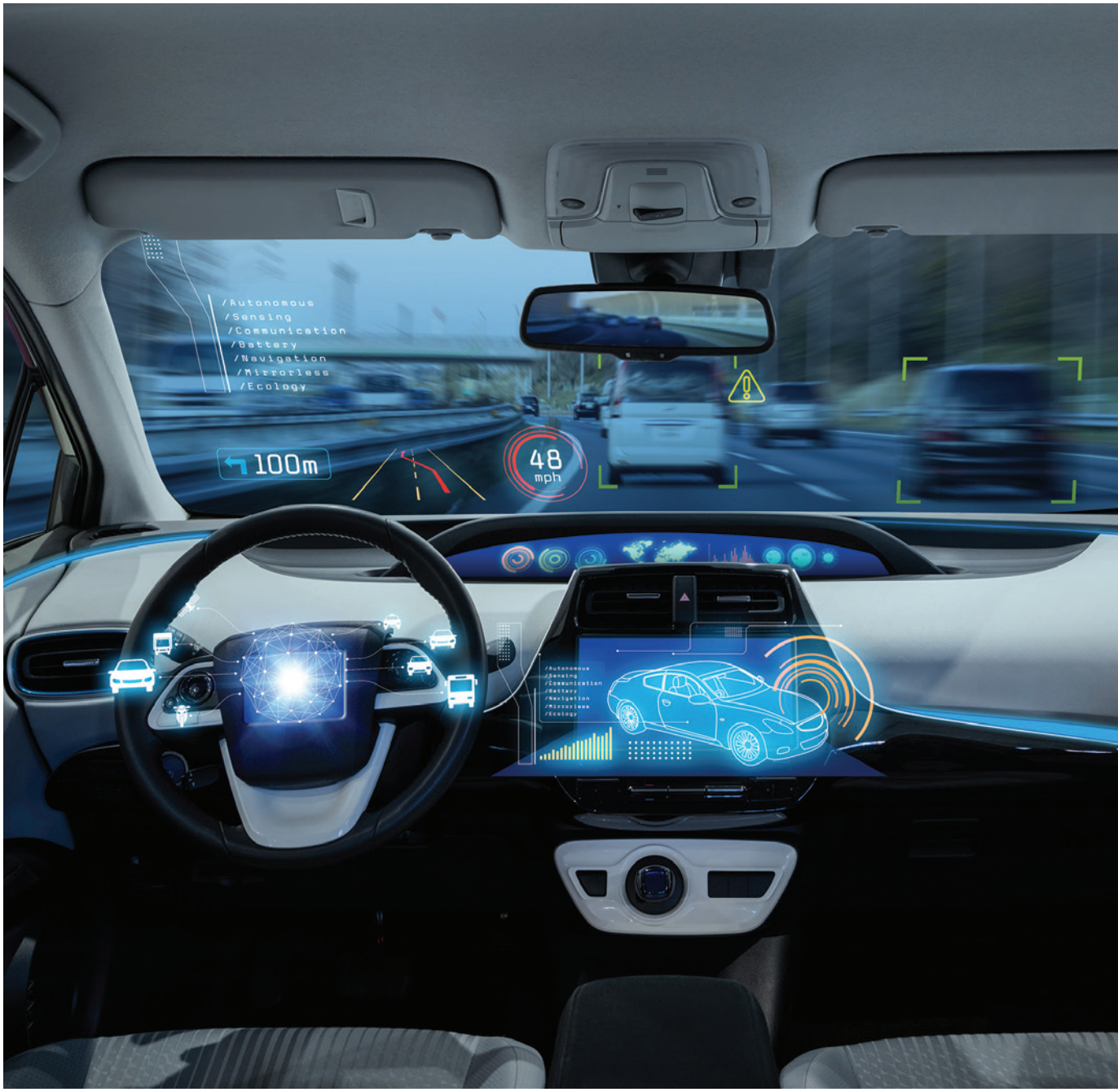
SUMMARY

Electrostatic discharge testing has evolved from a company-based reliability test in the 1960s and 1970s to a performance test on electronic products in the 2023 timeframe. The requirement is for electronic products to operate successfully when subjected to ESD phenomena representing the real-world environment as simulated in an electromagnetic compatibility testing laboratory. The emphasis has switched from the susceptibility of equipment to quoting how immune a product is to air-discharge and contact discharges from a portable ESD tester whose output is compliant with the latest international standard criteria.

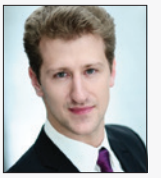
The next version of IEC 61000-4-2 is currently under development by the IEC. The third edition of the standard is expected to be published around April 2025.

A valuable Guide was published in 2016 by the ANSC C63 Committee on EMC to aid engineers in understanding and using the universally recognized IEC standard on ESD (61000-4-2).

AUTOMOTIVE HIGH-SPEED INTERFACES: FUTURE CHALLENGES FOR SYSTEM-LEVEL HV ESD PROTECTION AND FIRST-TIME-RIGHT DESIGN



Sergej Bub, the lead author of this paper, is a System Level ESD expert at Nexperia Germany GmbH in Hamburg. He works in the development department in the area of ESD protection and filtering, focusing on modeling and simulation of high-speed application systems and discrete ESD protection components, covering automotive, mobile, and computing areas. Sergej can be reached at sergej.bub@nexperia.com.



By Sergej Bub, Markus Mergens, Andreas Hardock, Steffen Holland, and Ayk Hilbrink

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INTRODUCTION

The automotive industry is experiencing a revolutionary transformation towards electrification, autonomous driving, as well as more connectivity and information. Thus, in-vehicle-network architecture is changing with an exploding amount of data cars need to process at high-speed. For example, infotainment content is rapidly increasing with an average of 20 cameras and 15 displays per vehicle. In addition, the new zonal architecture requires a new IP based protocol. Here, the automotive ethernet plays a key role for the links with data rates up to 1 Gbit/s today and multi-Gbit/s in the future. The so-called Open Alliance Committee defines a standard for those links in EHTERNET 100/1000BASE-T1, especially for the ESD protection device [1].

Figure 1 depicts the general trend (blue curve) of in-vehicle networks data-rates for different automotive protocols from the legacy LIN, CAN, FLEXRAY to the advanced protocols of ETHERNET up to SERDES. The orange curve shows the corresponding maximum of permissible parasitic capacitance of the discrete ESD component at the data line (partly from author's experience).

Significant ESD challenges result from the OPEN Alliance Ethernet specification [1], requiring the ESD protection device being robust for minimum of 1000 discharges at 15 kV ESD IEC 61000-4-2 pulse. At the same time, the discrete ESD capacitance is demanded to be continuously reduced for future high-speed protocols even below levels of 0.5 pF to ensure RF signal integrity. These two conflicting trends can only be met with highly advanced, discrete ESD architectures while on-chip ESD in the IC transceiver often does not suffice those requirements anymore.

In addition, the specification [1] recommends placing the external ESD component close to the connector, see Figure 3, instead of a position directly at the IC, i.e., behind the decoupling capacitors. The intention of this modification was to safeguard the overall system including all discrete components located in the signal path and to fulfill the EMC immunity requirements such as Direct Power Injection (DPI) acc. to IEC 62132-4 [2]. As a consequence of this placement, the new topology demands a more challenging high-voltage ESD specification with a high trigger V_{t1} > 100 V and high holding voltage V_{hold} > 28 V to prevent triggering of the ESD protection device during normal operation and disturbances. For earlier Ethernet links, those high-voltage values were not required since a low-voltage discrete ESD component protection was sufficient behind the decoupling cap directly at the IC.

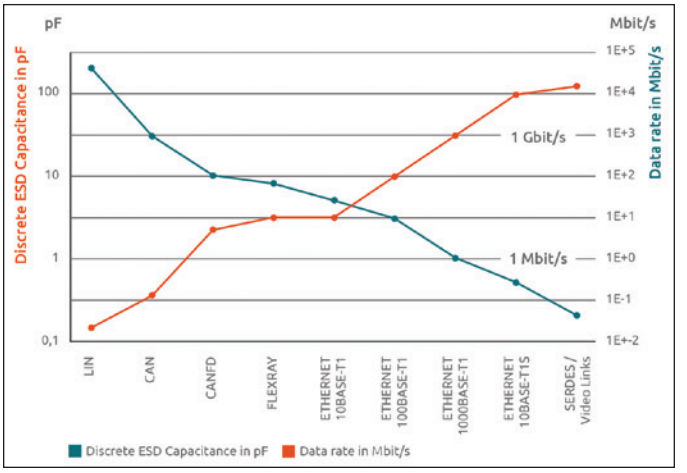

Figure 1: Automotive communication protocols with increased data rates from 20 kBit/s (LIN) to multi-Gbit (ETHERNET, Serdes). Impact on maximum permissible capacitance to be added by discrete ESD component to the high-speed data lines.

For those modern links described above, a silicon-based discrete ESD component (snapback-type) with $V_t \approx 140$ V, $V_{hold} \approx 35$ V, and $R_{dyn} \approx 0.1\ \Omega$ can be used, see Figure 2.

To measure the residual and potentially damaging current into a PHY (i.e., IC) for a system-level ESD event, a special PCB test network is recommended by OPEN Alliance 100BASE-T1 and 1000BASE-T1 applications [1]. This network is shown in a block diagram in Figure 3 with the discrete ESD component at the connector, a common mode termination (CMT), a decoupling capacitors, a common mode choke (CMC), and PHY (transceiver IC), more detailed in Figure 16.

Figure 4 displays an example for a measured residual IC current transient I_{IC} for 6 kV-ESD generator stress, acc. to [2], for two different protection device types, such as snapback and varistor, see TLP I-V characteristic in Figure 2. Apparently, the IC current can be safely limited applying the advanced snapback-type ESD protection device while the varistor admits an approximately 6x higher peak current into the IC due to the relatively high ESD voltage clamping.

This level violates even a 4 kV-HBM limit. It should be noted that the initial current spike demands a certain Charged Device Model (CDM) robustness-level from the transceiver IC for both cases, as discussed below in more detail. Apparently, limiting the systems ESD voltage exposure with appropriate discrete snapback clamps can be important for protecting advanced automotive high-speed interfaces.

Following system-level design challenges are addressed in this paper:

- CMC filters in the data-line play an important role also for ESD protection of the system IC as will be discussed in detail by measurement and simulation. Moreover, the CMC trend for smaller inductance L for higher data transmission may lead to a reduced ESD blocking capability of the CMC and this to a more critical ESD exposure to the entire system, as investigated by the transient SEED simulations Therefore, the ESD behavior of different CMCs is studied in detail and compared for the first time as well as its impact on system-level ESD protection .
- ESD discrete protection parameters become more challenging, since there is a trend towards an

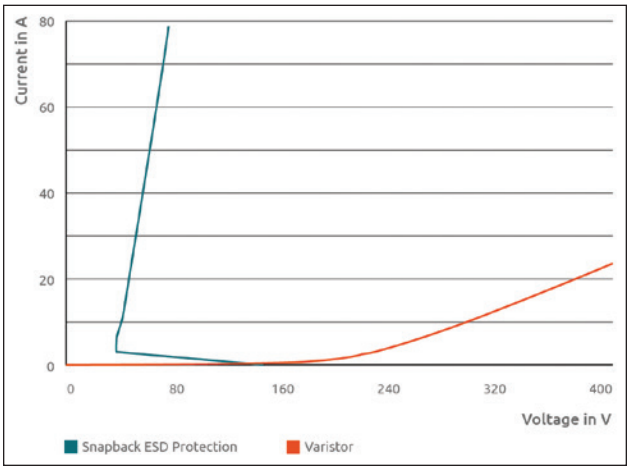

Figure 2: Transmission Line Pulse (TLP) I-V curve of discrete ESD devices for an Ethernet 1000BASE-T1 application: State-of-the-art silicon- based snapback device vs. varistor.

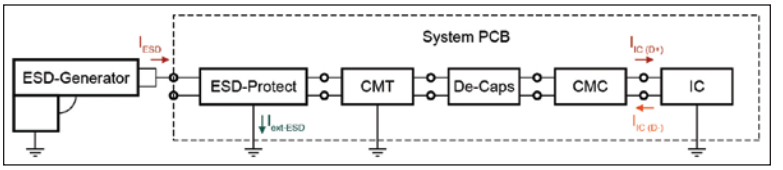

Figure 3: Equivalent circuit block diagram of system SEED model for the ESD current measurement.

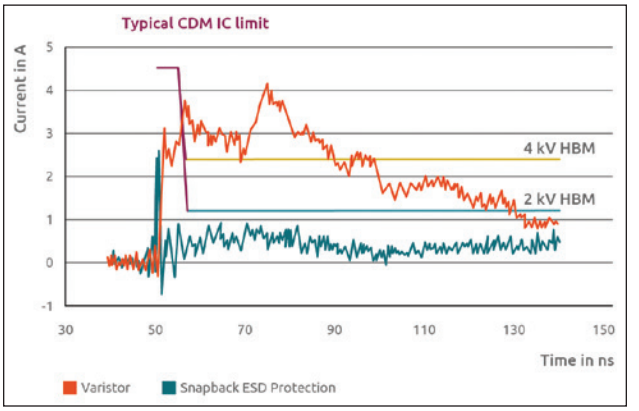

Figure 4: 6 kV ESD generator on ETHERNET test board: comparison of residual stress current into PHY (IC) for two discrete ESD protection types: silicon-based snapback device vs. varistor, see Figure 2. IC ESD limits: 2 and 4 kV as derived with respect to the discharge resistance of 1.5 kΩ in the Human Body Model (HBM) and typical CDM peak current IC robustness.

increased holding voltage, e.g., from 35 to 60 V or higher to comply for instance with a 48 V board nets and a robust system operation. This results in a larger ESD voltage stress for the system and thus higher currents into the RF-IO pins. In this paper, this behavior is investigated by system-level transient simulations based on the 1000BASE-T1 application.

ESD BEHAVIOR AND MODELING

This section outlines the ESD behavior and modeling of the relevant Ethernet system components for SEED with a special focus on CMC RF filter.

ESD Pulse Generator

A NoiseKen ESD generator was used for contact discharge of 1 kV into a 2 Ω Pellegrini target delivering a reference current waveform for model parameter extraction. Figure 5 shows a good fit between measurement and simulation [4].

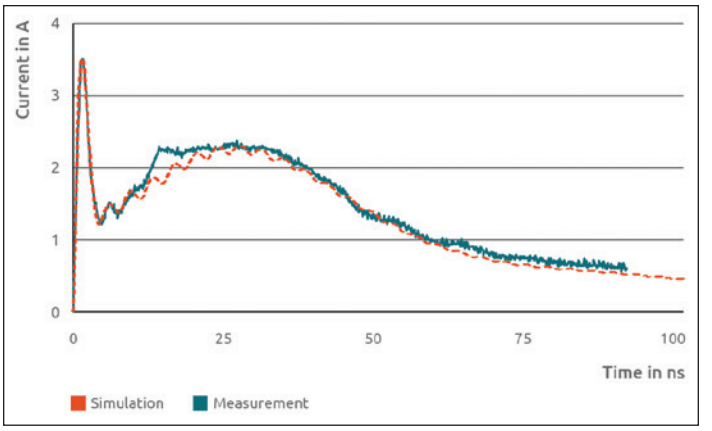

Figure 5: Current waveform of an ESD generator IEC 61000-4-2 [3] at 1 kV contact discharge through a 2 Ω reference target: simulation vs. measurement.

ESD Protection

To predict both the dynamic (ref. first IEC current peak) and quasi-static (ref. second IEC current peak) system ESD performance, a precise behavioral model of the external ESD protection was created [4].

Figure 6 shows an excellent match of the quasi-static measured TLP I-V with the simulation.

As already described in Section I, the capacitance constraints for discrete ESD protection at multi-Gbit/s data links shown in Fig. 1 requires minimizing the overall junction capacitance typically using lowly-doped Epi regions in these high-voltage transistors.

As a result, the turn-on time caused by conductivity modulation of the high-resistive region creates a relatively large transient trigger voltage overshoot, see Figure 7. Consequently, for a high simulation accuracy an adequate modeling of this transient ESD behavior is crucial and demonstrated by a comparison to the corresponding simulation.

Here, a behavioral dynamic model was tuned for accurate transient trigger voltage simulations making use of fast rise-time TLP curves [4].

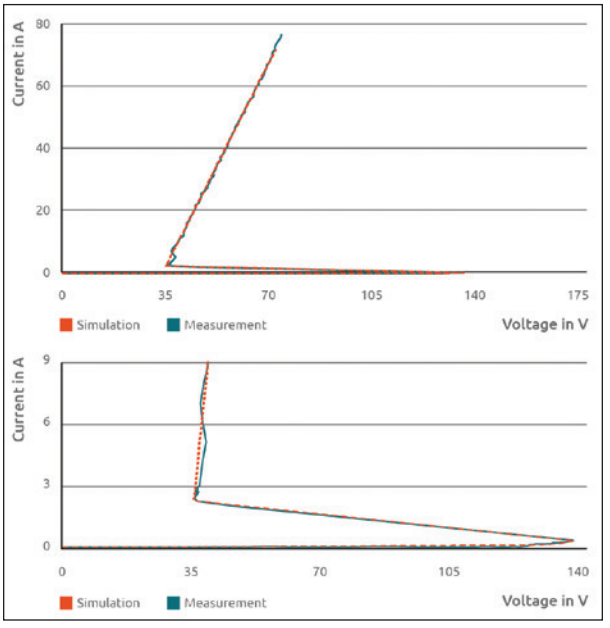

Figure 6: Discrete ESD protection (high-voltage snapback-type) TLP I-V characteristic in simulation vs. measurement.

Common Mode Choke

The CMC plays an important role not only to ensure RF signal integrity (SI) of the Ethernet application, but also to guarantee a certain system-level ESD robustness, as discussed in detail in this paper. The CMC architecture is in principle the same as in a transformer and based on two coils coupled thru a ferrite core, see Figure 8. Each coil connects thru the CMC terminals to one of the differential data-lines. During signal transmittance which is done simultaneously over both data-lines in a differential mode (DM), see Figure 8 a), the CMC appears to be in a low impedance state letting the signal pass through with minimal losses. This is because in the DM, roughly equal currents flow through both data lines and coils in opposite directions. The opposite current polarity creates a cancelation of related magnetic fluxes and a resulting minimum coil inductivity.

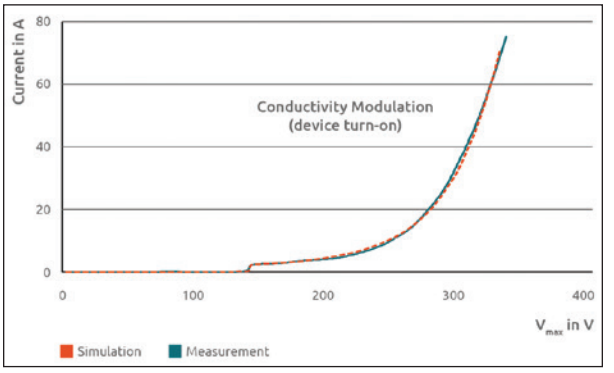

Figure 7: TLP I-Vmax characteristic in simulation vs. measurement showing the dynamic trigger voltage as a function of TLP current amplitude.

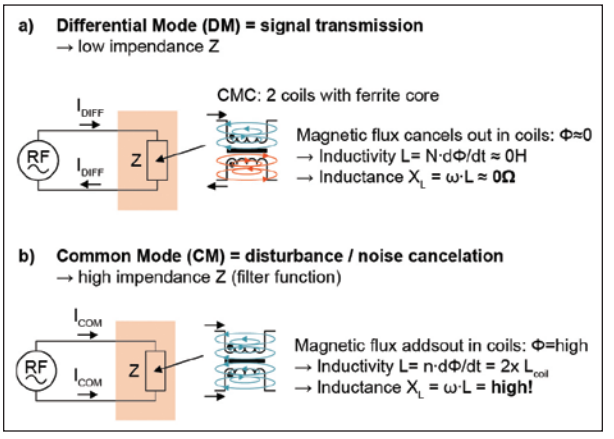

Figure 8: Principle of CMC modes for differential RF signal with low impedance (a) and common mode noise with high impedance (b).

The noise which is accommodating the signal on both data-lines corresponds to a common mode (CM) conduction, see Figure 8 b) i.e., non-differential. It will be suppressed by the CMC due to a high impedance. This ensures the overall RF signal integrity. Under the CM condition, both coil currents have the same direction while magnetic flux can add resulting in a maximum overall inductivity.

CMC operation during ESD

In the ESD stress case of one data line only, however, we can consider a third CMC operating mode. Here, the ESD pulse propagates only through one of the data-lines and thus coils, representing the so called "single-ended excitation" of the CMC, see Figure 9, with only one terminal being directly affected. To understand the behavior of the CMC in such an asymmetrical case of ESD disturbance, a TLP measurement method is applied as depicted in Figure 9.

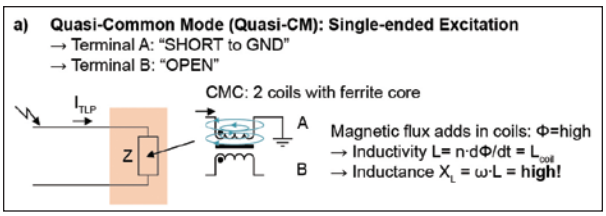

Figure 9: Single-ended Excitation of CMC by TLP: quasi-common mode with high impedance, Terminal B "OPEN."

Here rectangular pulses of different amplitudes and a constant pulse duration of 100 ns are injected into one of the two CMC terminals, while the remaining one will be kept in floating condition. A constant TLP rise time is set to be in the range between 600 ps and 1 ns which is very similar to the IEC61000-4-2 standard (see Figure 5) to ensure comparability.

Figure 10 on page 20 shows the resulting complex transient TLP current/voltage response of the CMC with L=100 µH in comparison to the corresponding simulation obtained with a CMC behavioral model (see dashed line), will be introduced later in this section.

Based on the transient curves, 3 characteristic regimes can be distinguished: dynamic (I) – voltage-dependent current overshoot in ns-range, a quasi-static regime of current blocking (II), and a current saturation (III). Those will be discussed in detail in the following.

Dynamic current overshoot (I)

It should be mentioned beforehand that a similar voltage dependent current overshoot in duration and amplitude as shown at the onset of the TLP current transient was observed in system-level ESD by the authors, see Figure 10, and reported in literature, see [7]. However, this 100 ns-TLP current peak is clearly related to a tester artefact caused by the distance of the CT1 current probe from the actual

DUT in the TLP setup, see HPPI application note [8]. In the first nanoseconds related to the propagation delay along the transmission line from the CT1 probe to the DUT and back, the 100 ns-TLP is blind to any current measurement except for the artefact peak.

Since such an initial peak cannot be measured with standard 100 ns-TLP, vf-TLP was performed in the same single-ended excitation of terminal A with terminal B fully floating. Figure 11 shows the only small capacitive displacement current of up to 30 mA for a slew rate of about dV/dt ~ 200 V/ns at this operation point. Using I = C x dV/dt a coil capacitance of C = 150 fF can be estimated. This value is well in line with the 140 fF reported in [6] for high-impedance CM conditions only. Note that under DM operation the parasitic coupling coil capacitance increases significantly to C~10 pF. [6].

As mentioned above and discussed in Section III in our IEC system-level experiments, we can clearly observe an initial fast current peak of high amplitude similar to the 100 ns-TLP artefact. This peak is very relevant for IC system-level protection as well and far larger in the amplitude than the small current peak we would expect based on the results shown in Figure 11, where the standalone CMC operates in quasi-CM. So why do we observe such an assumed contradiction in CMC behavior when used in a system circuitry showing a first current peak related to a large DM capacitance, but a current blocking behavior related to a quasi-CM state? This question will be addressed in Section III.

Current blocking regime (II)

In phase (II) the CMC reveals initially a high-ohmic current blocking condition similar to the CM case. The difference of the quasi-Common Mode regime for the single-ended excitation with one of the CMC terminals fully floating, i.e., terminal B in Figure 9, is that no current is induced into the coil connected to the floating terminal of the CMC. As a result, no magnetic flux can develop by the second coil and suppress the magnetic flux initiated by the first one. Therefore, the CMC coil of terminal A appears for the entering pulse in its single inductance of L=100 µH, as also reported in [5].

Saturation regime (III)

The onset of the CMC saturation is dependent on the voltage level across the excited CMC coil. The higher the voltage level, the earlier the magnetic saturation of the ferrite core occurs. Saturation leads to a significant increase of the current through the CMC, see Figure 10. In that case the current blocking capability

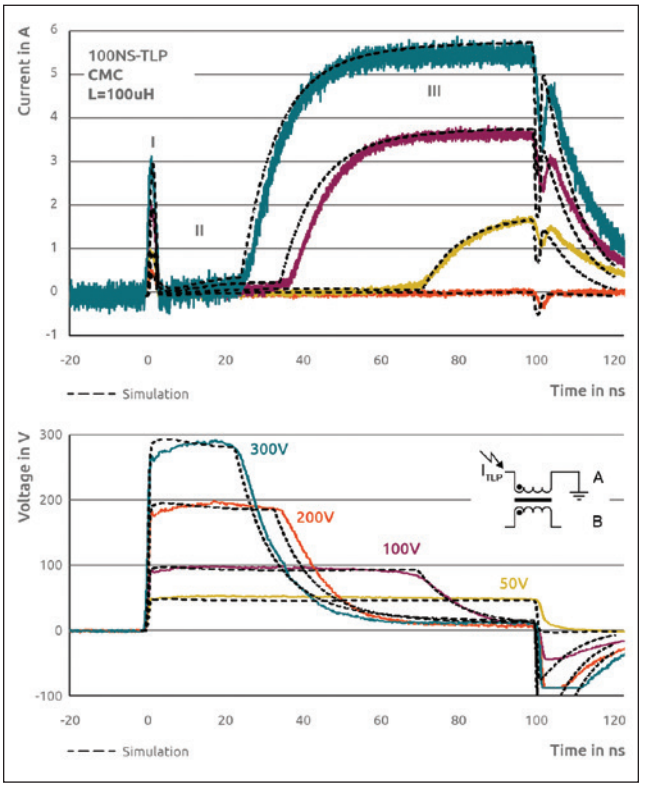

Figure 10: CMC with L=100 µH: Transient 100 ns-TLP current / voltage response for Trise = 600 ps indicating 3 operation regimes I-III. Simulation (dashed lines) is compared to measurements.

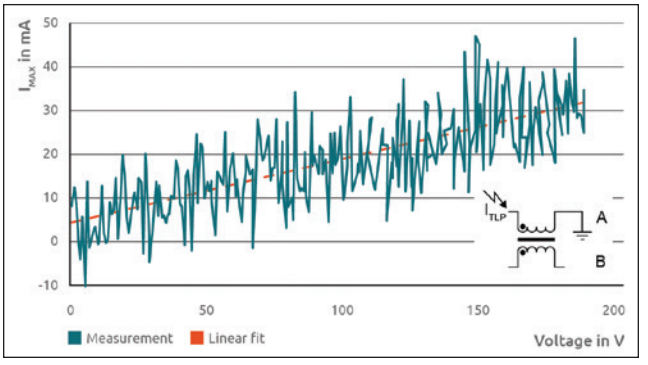

Figure 11: vf-TLP peak current measurement in single-ended excitation of line A, line B fully floating (Quasi-CM): only small Imax. The straight line shows a linear fit through the datapoints.

of the CMC will be lost due to transition into low-impedance or ohmic state. This detrimental behavior of the CMC for ESD should be carefully considered during the design of the Ethernet system and the ESD protection circuitry. Here, transient SEED simulation with an appropriate CMC model is a powerful tool for first-time right design. In the following, a behavioral CMC model will be introduced. Based on the observations, the Quasi-CM behavior of the CMC will be used for model tuning.

Behavioral model of CMC

In order to replicate the observed transient behavior of the CMC as shown in Figure 10 a dedicated behavioral model is implemented. Here, a modular approach is used to describe all 3 working regimes (I)-(III) of the CMC, see Figure 12. This block-diagram represents how the model is implemented for one of the CMC terminals. For incorporation of both CMC channels the extended circuitry can be just mirrored along the S-Parameters block.

The core of the simulation is represented by S-parameters block, which includes all parasitics of the device and describes the interaction between

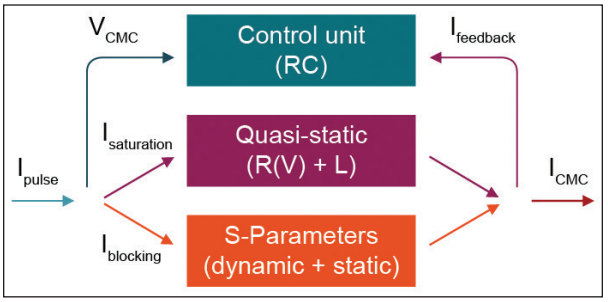

Figure 12: Equivalent circuit block-diagram for behavioral model of CMC (for one terminal) including (I) dynamic, (II) current blocking (static) and (III) saturation (quasi-static) working regimes.

the CMC terminals. This allows us to emulate both the dynamic (current overshoot) and static (current blocking) regimes of the CMC. To fine tune the voltage overshoot an additional capacitance can be added in parallel to the blocking path. Modeling of the quasi-static behavior (II) covers the onset of saturation in dependence of the applied voltage level over time with the subsequent low-impedance state. For this purpose, the S-Parameters model needs to be extended with additional circuitry.

To realize the resistance change of the signal path, a voltage dependent resistor (switch) is connected in parallel to the signal path of the CMC. To provide smooth transition from high- to low-impedance state and describe current rise and voltage decay over time properly, an inductor is connected in series to the voltage dependent resistor as well. In addition, to fine tune the voltage offset in the low-impedance state a DC voltage source can be placed in series with the switch and inductor. Finally, to control the voltage change at the switch a control unit circuitry represented by an RC network and extended by a feedback loop are implemented. The latter is required to keep the reached control voltage levels for the switch during the whole saturation regime constant.

CMC key criteria for system ESD design

Besides the initial current spike (I) two criteria are relevant for the CMC's ESD blocking capability: a) the duration after which the CMC becomes low resistive, i.e., transparent for ESD due to transition from (II) to saturation (III), and b) the saturation current in the low-ohmic regime. Figure 13 compares these voltage dependent values for two different CMCs with L=100 µH vs. 200 µH in a 1210 and 1812 package respectively.

As expected, the lower inductance CMC transits faster from high-resistive current blocking mode into onset of saturation, thus losing the ability to "isolate" the IC from the ESD exposure faster. Moreover, the saturation current is significantly larger for the same TLP voltage as compared to the larger L=200 µH due to a lower ohmic coil resistance. Furthermore, not only the nominal value of the inductance L of the chosen CMC impacts the ESD behavior as e.g., the onset point of saturation, but also the manufacturer specific package/dimensions and ferrite core geometry and material. Figure 14 gives an overview for CMCs in two different packages (of same manufacturer), but same inductance values characterized by TLP.

For same package configuration PKG (1812), we observe the same inductance dependence for saturation current and time to the onset of saturation as discussed above. However, it is important to note that different packages PKG (1812) vs PKG (1210) with same inductance exhibit entirely different ESD blocking capability. Consequently, to choose an appropriate CMC for system ESD protection we need to consider both inductance and package-type.

In the next chapter a system-level ESD analysis and risk assessment for multi-Gbit configuration will be performed taking into account the changed CMC

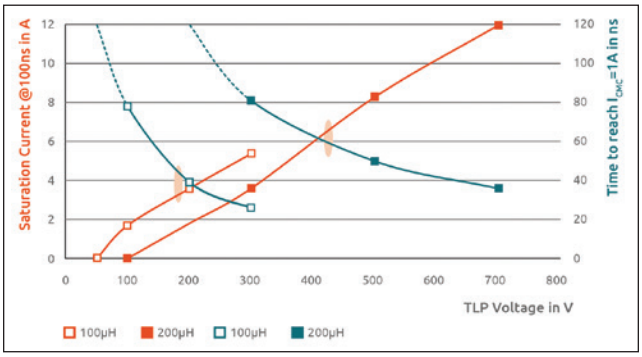

Figure 13: Comparison of two CMCs: L=100 µH vs. 200 µH regarding saturation current and time to the onset of saturation.

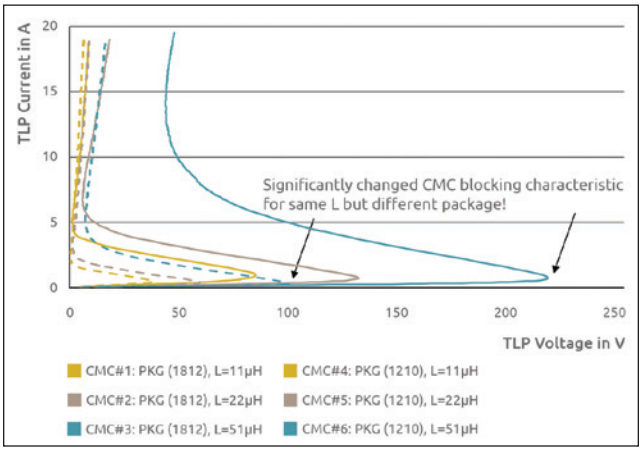

Figure 14: Comparison of CMCs in two different packages with: L=11 µH vs. 22 µH vs. 51 µH regarding onset of saturation.

ESD blocking characteristic due to more challenging SI requirements of the high-speed data links.

SYSTEM-LEVEL ESD ANALYSIS

For system-level measurements and SEED simulations Ethernet emulation network based on the specification [1] is used, see Figure 15. The decoupling capacitors of 100 nF are practically transparent for ESD pulses due to the very high dynamics of the ESD generator and, hence, do not impact the ESD behavior significantly. The CMT though seems to have an impact on the conduction state of the CMC as discussed below. The transceiver IC is emulated in a simplified but fairly critical way using a resistor network of 2-Ohm according to the OPEN Alliance specification [1].

Ethernet ESD Behavior

Figure 16 on page 24 shows a system level measurement and simulation for the residual current based on

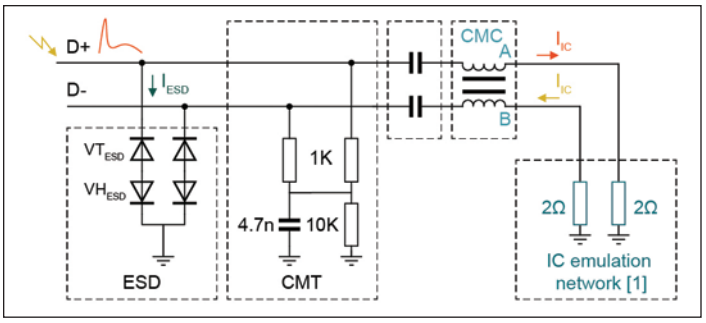

Figure 15: Ethernet ESD current test circuitry including standardized IC emulation network formed by resistors [1].

100BASE-T1 network using a 4 kV ESD pulse according to IEC 61000-4-2. In general, the agreement between measurement and simulation is fair. The main characteristics can be captured by the simulation very well. Also, here the first peak can be clearly observed but compared to the TLP measurement in section II it is real and can be explained as follows.

The system-level ESD scenario in the Ethernet circuitry, as shown in Figure 15, differs from earlier discussed CMC analysis using TLP with floating coil B:

- Coil B is not fully floating but connected to the IC I/O with its internal ESD protection circuitry as emulated by the 2 Ohm resistor, same as coil at terminal A.
- A CMT network is connected to the CMC terminals at D+/D- thru the dc block (which can be neglected in the ESD time domain due to capacitance value)

In this configuration (see Figure 17) a modified CMC response is expected. Figure 18 illustrates the results for both single-ended excitation cases, using TLP, where Terminal B is in one of two corner conditions: "OPEN" and "SHORT to GND".

The green curve represents the quasi-CM which was already introduced as a high-impedance state with transition into low impedance saturation. As opposed to this behavior, the red curve demonstrates the response of the CMC where terminal B is shorted to GND same as terminal A instead of floating.

Here we can observe that the CMC goes immediately into a low-impedance state with saturation regime, i.e., quasi-DM. Note that this configuration of terminal A and B on ground resembles the circuitry shown in Figure 15.

The result for quasi-DM condition contradicts the fact that we observe only a small residual current flowing into the IC, see Figure 16. That means, that CMC, being used in Ethernet circuitry acts in a high-impedance blocking state, as could be explained by quasi-CM, allowing the external ESD protection component to turn on and finally protect the IC.

Based on additional transient measurement on system-level, we developed a hypothesis to resolve this contradictory issue. Here, we considered the full board circuitry including the CMT network as a discriminating factor compared to our standalone CMC analysis. Figure 19 shows TLP time domain curves, where the CMT network including decaps is connected to the

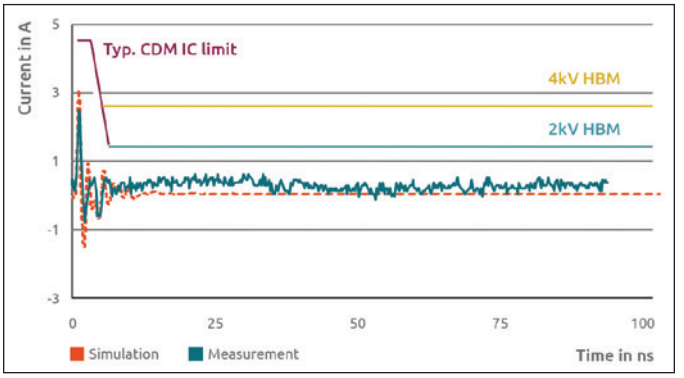

Figure 16: 4 kV ESD generator system-level measurement vs. simulation with snapback ESD device (see Figure 6) and a CMC L=200 µH [4].

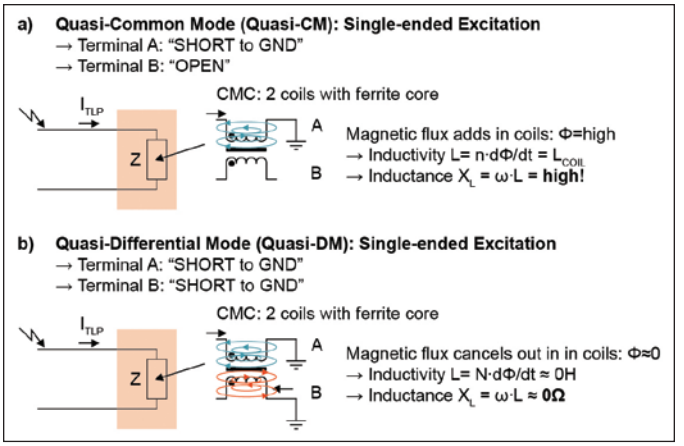

Figure 17: Single-ended excitation of CMC by TLP: quasi-common mode with high impedance (a), quasi-differential mode with low impedance (b).

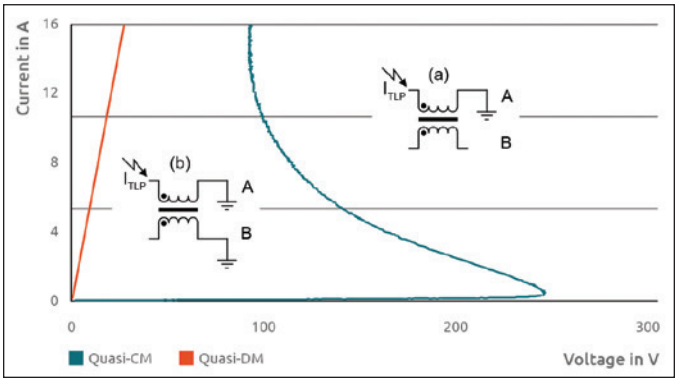

Figure 18: Single-ended excitation of CMC by 100 ns-TLP with T_r= 600 ps quasi-CM with second coil B fully floating, and quasi-DM with terminal A and B connected to ground, as illustrated in Figure 17 (a) and (b), respectively.

CMC from the left side and a 2 Ohm resistor terminates each of the CMC channels from the other side.

Here, no external ESD protection was connected between D+/D- and ground. Based on the results, we can conclude that a mix of two different operating modes occur for the CMC. At the onset of the pulse, during the first nanoseconds, the CMT is transparent and negligible for the entering TLP pulse. This is due to the fact the 1k-resistors are inflicted by parasitic inductance of several nH. Thus, the CMT circuit is an open which leads to a floating input of coil B. As shown in section III. A, this quasi-DM state has a low impedance and a high capacitance across the coil in the order of ~10 pF.

TLP measurement depicted in Figure 19 proves the differential operation mode due to the differential current peaks with same amplitude but different polarity. Those are likely a mixture of low-resistive DM response, plus as well as of capacitive coupling.

However, after some time the CMT network starts to shift the current phase between Terminals A and B of the CMC thus preventing the magnetic flux cancelation. As a result, the CMC transits into the high-impedance quasi-CM condition. Due to a relatively large time constant of the CMT $\tau = R \times C \sim 5\ \mu s$, the charging of the CMT capacitance should last during the entire ESD event keeping the CMC in the quasi-CM until saturation. In blocking mode, the CMC can strongly support the external ESD protection consequently avoiding any significant residual current into the IC during the entire ESD pulse, see Figure 19. In case the applied TLP voltage level is high enough, also the onset of saturation within quasi-CM regime can be observed.

For a system-level ESD protection it is obvious, that CMC alone is not capable to suppress the current initiated by the single-ended injection of ESD pulse and needs to be extended by an appropriate CMT network. In the full system circuitry, the CMC, CMT and the external ESD device are building a synergy significantly extending the entire system ESD robustness. On the one hand, the blocking characteristic of the CMC during the first nanoseconds helps to trigger the ESD protection

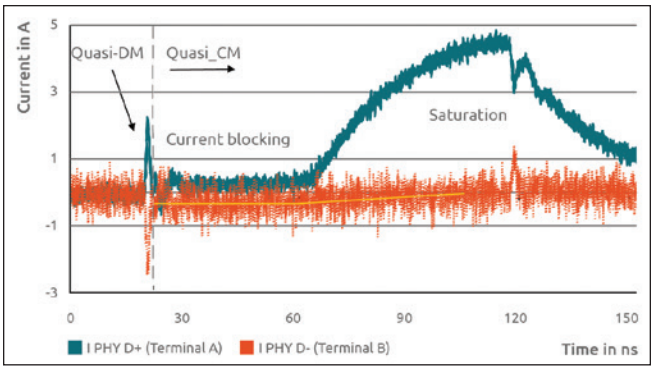

Figure 19: Single-ended excitation of D+ by 600 V 100 ns-TLP injection (system configuration see Figure 15 w/o ESD protection devices) where CMC shows a mix of two operating modes: Quasi-DM with current overshoot on both channels at first nanoseconds and Quasi-CM with current blocking and saturation regimes.

device. On the other hand, the ESD device takes the majority of the ESD current protecting consequently not only the IC, but rather the entire circuitry incl. CMC and CMT. A more detailed explanation based on a SEED simulation is given in the next subsection.

ESD Risk Analysis of Multi-Gbit Systems by SEED Simulation

Next generation multi-gigabit data links such as automotive Ethernet or SERDES will definitely require different ESD protection devices and CMCs. However, no well-defined specifications for those components are available yet. Therefore, the authors make some plausible assumptions for electrical parameters of the ESD and CMC components to investigate the synergy effects of both components, see section III A, by transient SEED simulations.

Firstly, a discrete ESD device with snapback and a larger holding voltage V_{hold} of 60 V is considered due to the trend to higher battery voltages for hybrids and electrical vehicles. Secondly, a CMC with reduced inductance L of 100 µH is used due to higher data rates, hence, less inductance and parasitics will be added to the D+/D- in the context of signal integrity [1]. Figure 20 on page 26 depicts the results of the transient simulation for this example for 4 kV-IEC system-level stress.

As can be seen in Figure 20 (green curve), the non-linear behavior of the CMC in conjunction with the ESD protection device turn-on behavior and clamping dynamics creates a critical current profile thru the

sensitive IC I/O. Due to increased ESD clamping voltage (larger V_{hold}) and the lowered CMC blocking capability (smaller L), the current into the IC I/O connected to the D+ data-line, would slightly exceed in its peak value at 60 to 70 ns a 4 kV-HBM IC robustness level.

In conclusion, this example of SEED simulation, extended with non-linear dynamic models of ESD protection devices at D+ /D-, confirms the CMC working regimes from Section III.A when used within Ethernet circuitry: a) at the beginning CMC works in quasi-DM, as indicated in the simulation by two opposite current peaks at the onset of the pulse, followed by b) quasi-CM (current blocking mode), where the ESD current into the IC is almost blocked entirely. As a consequence, the voltage at the ESD protection starts to increase to the triggering level, at which it turns on and starts to shunt almost the entire IEC pulse to GND.

After a duration of approximately 40 ns, the CMC enters saturation, thus gradually losing its blocking capability. As a result, the current into the IC interface at D+ increases (green curve). Due to this competitive conduction with the CMC, the ESD device eventually starts to turn off at 60 ns, as soon as current and voltage levels at the ESD protection get too low to keep it further on. At this time, the CMC also reaches saturation (i.e., lowest impedance) while the current into the IC attains its maximum. This peak current slightly exceeds the 4 kV-HBM limit.

This simulation example clearly demonstrates the important synergetic protection mechanism of the ensemble of CMC and ESD within a complex system circuitry. Important to note in this context is that an enhanced ESD voltage clamping limits the residual IC current by two effects: a) the more trivial lower voltage exposure to the IC, b) the subtle effect of keeping the CMC for a longer duration in a current blocking mode before reaching low-impedance saturation.

The latter effect is highlighted by system-level simulation with a varistor in comparison to the snapback ESD protection in Figure 21. The higher clamping voltage of the varistor obviously provokes a much earlier onset of CMC saturation at

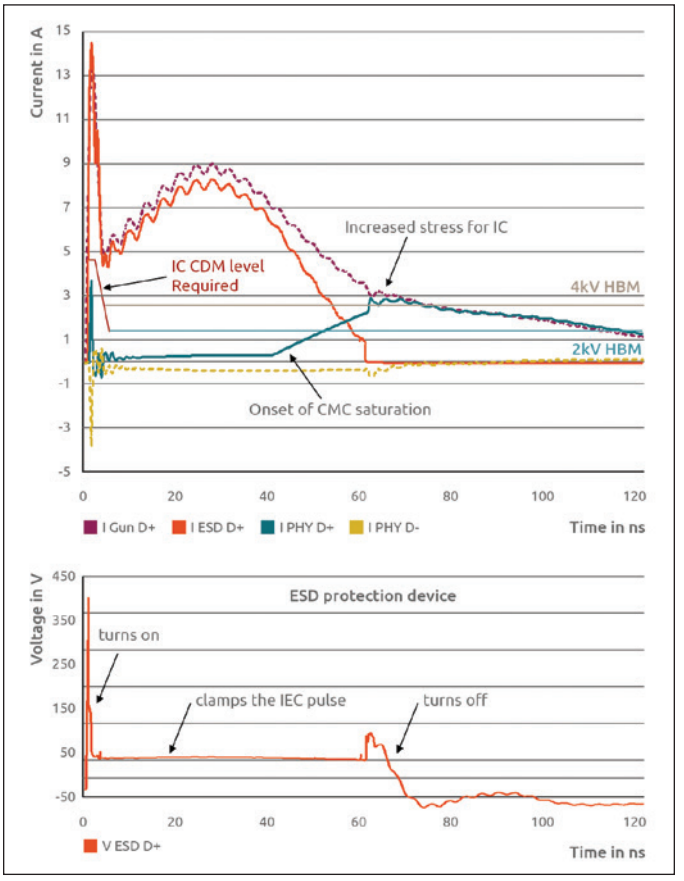

Figure 20: System-level 4 kV IEC simulation of Ethernet circuitry, see Figure 15, for a snapback ESD protection with V_{hold} = 60 V and a CMC with reduced inductance to L = 100 µH. (a) Injected ESD pulse current, current through the ESD device at D+ and currents through both data lines (D+/D-). (b) Voltage at ESD protection at D+ node.

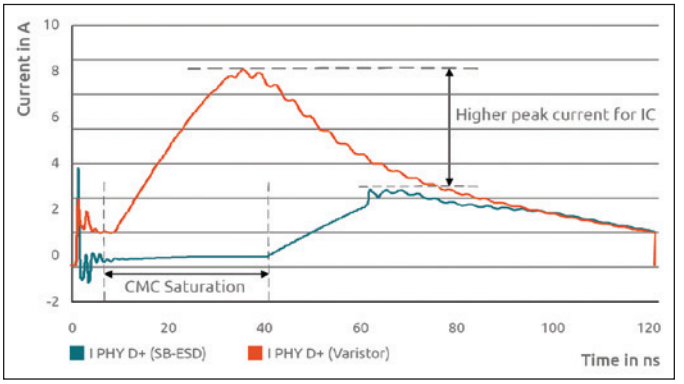

Figure 21: System-level 4 kV IEC simulation of Ethernet circuit, see Figure 15, with CMC L = 100µH and different ESD protection: snapback ESD (same as in Figure 20) vs. varistor (Figure 2).

about 10 ns instead of 40 ns observed for the more effective snapback clamp. As a result, the current into the IC (PHY) reaches an almost three times higher peak value compared to the snapback protection as well as a significantly longer stress duration almost during the entire energetic part of the IEC pulse. Thus, the overall IC stress energy and risk of failure significantly increases.

CONCLUSION

This paper analyzes the future design challenges of system-level ESD protection for automotive high-speed data-links such as multi-gigabit Ethernet and SERDES. In particular, the impact of the changed ESD device requirements (increased holding voltage e.g., for higher board net voltage) and CMC limitations (lower inductance for better RF signal integrity) is investigated. Here, a special focus is put on an in-depth understanding of CMC operation during ESD event as standalone CMC and as device applied in the system. A clear CMC working regime classification is identified showing transitions from low-resistive quasi-DM to high-impedance quasi-CM to low-impedance saturation. In addition, the impact of inductance L and package variation for different CMC is investigated. As expected, the device reveals an increased ESD blocking capability with higher L for the same package type. However, also a different package appears to have a major impact on it even for the same manufacturer. Consequently, the inductance L is not the only figure of merit for choosing an appropriate CMC in view of protection against ESD during the initial system design phase.

For the SEED simulations on system-level described in the paper, the complex high-current CMC characteristic was incorporated into a non-linear behavioral CMC model. Applying both CMC and ESD non-linear dynamic behavioral models, the system simulation results clearly illustrate the synergy effects of CMC and the discrete ESD protection as also confirmed by appropriate measurements (TLP, IEC 61000-4-2). As major finding, it turned out that a lower ESD clamping voltage enabled by a well-tuned, high-voltage snapback device offers a superior protection not only due to the trivial effect of less voltage exposure to the IC. Another strong second benefit is that the lower ESD voltage exposed to the CMC keeps the inductance for a longer duration in a blocking state. Thus, the IC is perfectly shielded from the ESD until the CMC enters the low-resistive saturation mode. Such a prolonged blocking time can be sufficient to keep out the high-current, high-energy IEC peaks in conjunction with a well-designed ESD component.

The paper highlights the benefit of a SEED simulation-based pre-design phase of the more advanced automotive high-speed links. Moreover, the tool allows an appropriate selection of external ESD and passive components to achieve a first-time right system ESD design in compliance with RF signal integrity.

ACKNOWLEDGMENTS

The authors would like to thank Shubhankar Marathe for valuable feedback during the paper review process.

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Join us in person at the 2023 EOS/ESD Symposium

The last three EOS/ESD Symposiums were offered in a hybrid format for presenters and attendees – facilitating virtual connection for those strongly impacted by pandemic-related travel restrictions. In 2022, more than 200 attendees and 36 exhibiting companies traveled to the Peppermill in Reno, NV, USA, and only 50 attendees participated virtually. The shift of attendees attending virtually in 2020 and 2021 to in-person in 2022 demonstrates the value and importance of face-to-face events and activities.

After considering many variables influencing a decision to host face-to-face-only events, the EOS/ESD Symposium will be on-site with no livestream connection in 2023. This decision means the Symposium strategy team can explore new ways to increase the interactivity that attendees truly value – the face-to-face and networking opportunities provided by an in-person event.

These opportunities include enhancing already established interactive sessions, such as workshops and hands-on demonstrations, and adding new initiatives. One focus is revamping the format of workshops with a task team already evaluating innovative solutions, such as interactive polling, a panel of invited speakers, and a new standalone session on the upcoming revision to the EOS/ESD Association, Inc. Technology Roadmap. We are introducing a new interactive session with members of the Association's standards working group activities and a new exciting electronic format for the

Author's Corner posters. Other exciting ideas include expanding the exhibit hall offerings with introductory tours to meet the exhibitors and demonstrations by exhibitors in their booths.

We appreciate your understanding and trust that EOS/ESD Association, Inc. has carefully considered the many impacts of hosting an in-person-only Symposium in 2023. With your support, EOS/ESD Symposium will continue to be the premier industry event. The 2023 Symposium Strategy and Steering Teams are excited about what's to come, and we hope you are as well!

We look forward to seeing you in person at the 2023 EOS/ESD Symposium at the Riverside Convention Center in Riverside, CA, USA

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Schedule of Events

September 30 - October 5, 2023

With the focus on *Quality over Quantity*, the Symposium strategy team heard your schedule concerns and suggestions. In an effort to not dilute the quality of the event and address the lower attendance in Thursday sessions, we have restructured and streamlined the previous 3.5–day, three–parallel track event schedule. The 2023 EOS/ESD Symposium will be condensed to 3 full days – Monday morning, October 2, through Wednesday evening, October 4. Additionally, the parallel sessions will be reduced to two tracks for the entire duration of the event. We will continue to offer a selection of tutorials and the program manager certification exam before and/or after the Symposium. This redesigned schedule reduces the number of sessions required to fill the program, thus, allowing the team to focus on the quality of the event rather than the quantity.

SATURDAY, September 30	
8:00 AM - 5:00 PM	FC340: ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) - Day 1
8:00 AM - 5:00 PM	ESD Compliance Verification Technicion to TR53 - Day 1
8:30 AM - 4:30 PM	FC100: ESD Basics for the Program Manager

SUNDAY, October 1	
8:00 AM - 5:00 PM	FC340: ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) - Day 2
8:00 AM - 5:00 PM	ESD Compliance Verification Technicion to TR53 - Day 2
8:30 AM - 12:00 PM	DD/FC240: System Level ESD/EMI (Principles, Design Troubleshooting, & Demonstrations)
8:30 AM - 4:30 PM	FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements
1:00 PM - 4:30 PM	DD134: Fundamentals of ESD System Level

MONDAY, October 2	
8:00 AM	Welcome
8:00 AM - 8:35 AM	Device Testing Invited Talk
8:00 AM - 5:00 PM	ESD Compliance Verification Technicion to TR53 - Day 3 (Exam)
8:10 AM - 8:35 AM	German ESD Forum E.V. Best Paper
8:35 AM - 9:25 AM	Device Testing Papers 1A.1 & 1A.2
8:35 AM - 9:25 AM	GaN Invited Talk
9:25 AM - 9:45 AM	Author's Corner
9:55 AM - 10:45 AM	Device Testing Papers 1A.3 & 1A.4
9:55 AM - 10:45 AM	GaN Invited Talk
10:45 AM - 11:05 AM	Author's Corner
11:15 AM - 12:30 PM	Device Testing Papers 1A.5, 1A.6, & 1A.7
11:15 AM - 12:30 PM	GaN Papers 2A.1, 2A.2, & 2A.3
12:30 PM - 12:50 PM	Author's Corner
12:30 PM - 1:30 PM	Emerging Professionals and First Time Attendee Reception
1:30 PM - 3:10 PM	Presentation & Interactive Workshop - Automotive
1:30 PM - 3:10 PM	Manufacturing Papers M1.1, M1.2, M1.3, & M2.2
3:10 PM - 3:30 PM	Author's Corner
3:30 PM - 4:20 PM	EMC Invited Papers
3:40 PM - 4:00 PM	Manufacturing Invited Talk
4:00 PM - 4:55 PM	Manufacturing Hands-on Measurement Session
4:50 PM - 5:40 PM	EMC Papers 1B.1 & 1B.2
5:00 PM - 6:00 PM	Professional and Technical Women's Reception
5:05 PM - 6:00 PM	Manufacturing Hands-on Measurement Session
5:40 PM - 6:00 PM	Author's Corner
6:00 PM - 9:00 PM	Welcome Reception - Exhibits Open

TUESDAY, October 3	
7:30 AM - 9:00 AM	Breakfast and Awards Presentation
9:00 AM - 9:50 AM	Keynote
9:00 AM - 9:50 AM	Exhibits Open (Coffee available in the Exhibit Hall)

Schedule of Events

September 30 - October 5, 2023

TUESDAY, October 3 *continued*	
9:50 AM - 10:35 AM	Guided Introduction Tour(s) to Meet the Exhibitors (9:55 - 10:30) (Light refreshments available)
10:35 AM - 11:15 AM	Manufacturing Invited Talk
10:35 AM - 11:25 AM	Emerging Technologies Invited Paper
10:35 AM - 11:25 AM	Exhibits Open (Coffee available in the Exhibit Hall)
11:25 AM - 11:55 AM	20-minute In Booth Demonstrations (11:30-11:50) - Parallel Sessions
11:55 AM - 12:55 PM	Manufacturing Hands-on Session - Handtools
12:05 PM - 12:55 PM	Emerging Technologies Papers 3A.1 & 3A.2
12:55 PM - 2:05 PM	Author's Corner
12:55 PM - 2:05 PM	Lunch in the Exhibit Hall
2:05 PM - 3:20 PM	Exhibits Open (Coffee available in the Exhibit Hall)
2:05 PM - 3:20 PM	Workshop - EDA
2:05 PM - 3:20 PM	Workshop - Handtools
3:20 PM - 4:00 PM	10-minute Exhibitor Showcases (3:25-3:55) - Parallel Sessions
4:00 PM - 5:00 PM	Standards Corner - Learn more about EOS/ESD Association, Inc. Standards
4:30 PM - 6:00 PM	Student Mentoring Event
5:00 PM	Exhibits Close
5:00 PM - 6:00 PM	Volunteer Showcase Reception - Open to All Attendees
6:00 PM - 7:00 PM	Discussion Group - Fab Certification

WEDNESDAY, October 4	
8:00 AM - 9:15 AM	Presentation & Interactive Workshop - ESDA Technology Roadmap
8:30 AM - 9:15 AM	Exhibits Open (Coffee Available in the Exhibit Hall)
9:15 AM - 9:55 AM	10-minute Exhibitor Showcases (9:20-9:50) - Parallel Sessions (Light refreshments available)

WEDNESDAY, October 4 *continued*	
9:55 AM - 10:45 AM	Automotive Invited Talk
9:55 AM - 11:10 AM	Device Testing Papers 5A.3, 5A.4, & 5A.5
9:55 AM - 11:10 AM	Exhibits Open (Coffee Available in the Exhibit Hall)
10:45 AM - 11:35 AM	Automotive Paper 2B.1 & 2B.2
11:10 AM - 11:30 AM	Author's Corner
11:10 AM - 12:05 PM	20-minute In Booth Demonstrations (11:05-11:25 & 11:30-11:50) - Parallel Sessions
11:35 AM - 11:55 AM	Author's Corner
11:55AM - 12:45 PM	Device Testing Papers 5A.1 & 5A.2
12:05 PM - 12:40 PM	Exhibits Open (Coffee available in the Exhibit Hall)
12:05 PM - 12:55 PM	Manufacturing Papers M2.1 & M2.3
12: 40 PM - 2:00 PM	Lunch in the Exhibit Hall
12:45 PM - 1:15 PM	Author's Corner
2:00 PM	Exhibits Close
2:00 PM - 3:15 PM	Workshop - Importance of Standards
2:00 PM - 3:15 PM	Workshop - Foundry Support
3:35 PM - 4:05 PM	Manufacturing Invited Talk
3:35 PM - 4:25 PM	Communications Invited Talk
4:05 PM - 5:35 PM	Manufacturing Hands-on Session
4:25 PM - 5:40 PM	Communications Papers 4A.1, 4A.2, & 4A.3
5:40 PM - 6:00 PM	Author's Corner
6:00 PM - 8:00 PM	General Chair's Reception including TeSD talk - Open to All Attendees

THURSDAY, October 5	
8:00 AM - 5:00 PM	ESD Professional Program Manager Certification Exam Part 1

Always refer to the Symposium official program for final details.

(RE)DISCOVERING THE LOST SCIENCE OF NEAR-FIELD MEASUREMENTS, PART 3

Understanding Radiated Emissions Measurements Made at One-Meter Separation: It's Not What You've Been Led to Believe

This is the third part of our article "(Re)Discovering the Lost Science of Near Field Measurements." Part 1 of this article (see *In Compliance Magazine*, July 2023) explained what near and far field measurements entail, and that one-meter measurements are very much near field. Part 2 (*In Compliance Magazine*, August 2023) explained the evolution of the earlier 12" and present-day one-meter separation measurements, considerations in antenna selection, the difference between antenna-induced and field strength limits, and the evolution from one to the other. This third part investigates practical problems arising from the misapplication of field intensity and far-field concepts to near-field phenomena.

PRACTICAL PROBLEMS ARISING FROM THE USE OF FIELD INTENSITY LIMITS IN THE EXTREME NEAR FIELD[23]

The term "extreme near field" has a specific quantitative meaning in this context. It means that the transmit-receive antenna separation is of the same

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By Ken Javor

magnitude as its physical aperture, or less. In the case of radiated emission measurements made one meter away from a test sample with 1.5 m or longer attached cables, not even the Hertzian dipole equations suffice to describe the near field. The Hertzian dipole field equations only apply when the separation distance is much larger than the radiating structure dimensions.[24]

SAE ARP-958 uses the physical model of two identical antennas in each other's far field (Friis equation) to calculate an "effective" gain at one-meter separation. This is an effective gain because the antennas are in each other's extreme near field. Therefore, the antenna factor so derived is only valid for measuring the field at that distance, and the standard of value is that antenna's response to its own field at that distance. There is no particular value to comparing the "field intensity" measured by (for example) a biconical to the field intensity that biconical would see from another biconical a meter away. In fact, it is quite harmful in that there is an unspoken (and incorrect) assumption on the part of many EMC engineers that the field intensity measured at one-meter separation is scalable in some prescribed manner so as to be able to predict what the measured field intensity would be at another distance.

Figure 8 presents data gleaned from an old EMCO catalog. The same sort of information may be found on the ETS-Lindgren website antenna page.[25] If one-meter "field intensity" measurements were scalable, the antenna factors would be identical. Now proponents of field intensity measurements and one-meter antenna factors will rebut the use of such data, saying that one- and three-meter antenna factors are measured differently. And this is true, but it is not fundamental.

What is fundamental is that the assumption that extreme near-field intensity measurements are scalable violates one of the most fundamental laws of physics, namely the conservation of energy or power. And only some high school physics and algebra is necessary to comprehend this.

Based on the diagram of Figure 9, the Friis equation may be written as:

$$P_R/P_T = G_T\, G_R \lambda^2 / (4\pi r)^2$$

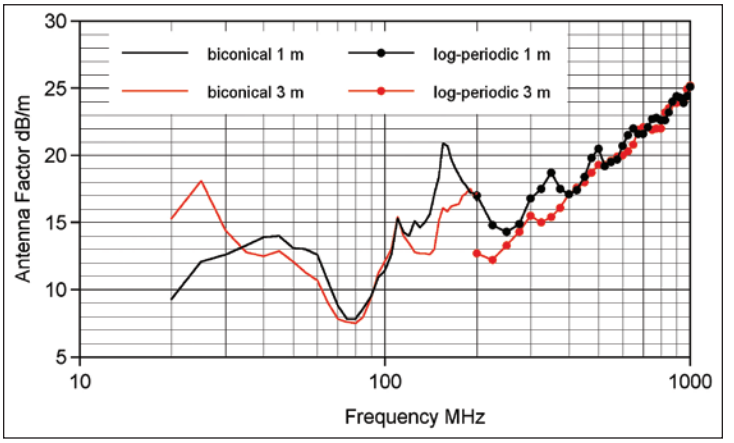

Figure 8: One- and three-meter antenna factors

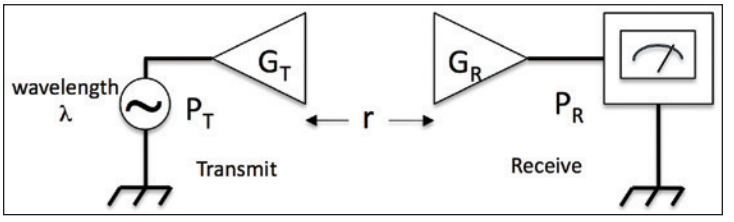

Figure 9: Set-up for understanding Friis equation

The Friis equation assumes that the separation distance places the antennas in the far field. In that asymptotic condition, the gain values are independent of separation, which is what makes far-field antenna calibration useful. But two elementary observations are apparent:

- The left-hand side ratio is bounded by unity, and in practice will always be less than unity, or 0 dB; and
- The right-hand side increases without bound as the separation decreases unless the gain values decrease commensurately.

The inescapable conclusion is that in close, gain is in fact a function of antenna separation. While gain or antenna factor asymptotically approaches a fixed far field value, this means nothing when the antennas are closer in than that.

Assuming half-wave dipoles (far field gain = 1.64 numeric, 2.15 dBi), one may solve the Friis equation for the distance at which the left-hand side ratio is unity, or 0 dB.

r = 0.13λ, or
r = D/4
where D is the half-wave dipole length

This is a purely theoretical construct that just says the gain must roll off at closer separations than this. Of course, the gain begins to roll off well before this calculated separation. The measured received power levels plotted in Figure 10 were taken using the set-up of Figure 9, with separation "r" variable between 2 meters and 30 cm. Two different frequencies were evaluated: 400 MHz (λ = 75 cm, D = 37.5 cm) and 1 GHz ((λ = 30 cm, D = 15 cm). Figure 10 shows measured vs. theoretical far field P_R/P_T ratios as a function of separation distance and wavelength. An inspection of Figure 10 shows that long before the far field calculation of received power shows it equal to transmit power, the response has rolled off.

There are complicating factors involved in the close placement of two wire-type antennas, which include dipoles and biconicals. In very close proximity, there is capacitive coupling with which to contend and, above a ground plane, inductive coupling. Further, the direction

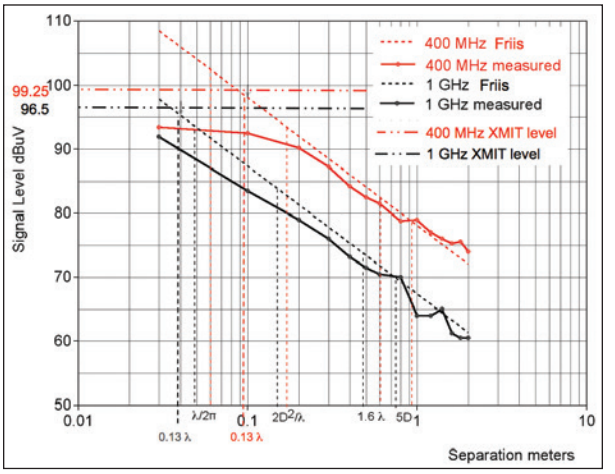

Figure 10: Ratio of received vs. transmit power vs. half-wave dipole separation comparing the Friis equation and measured data

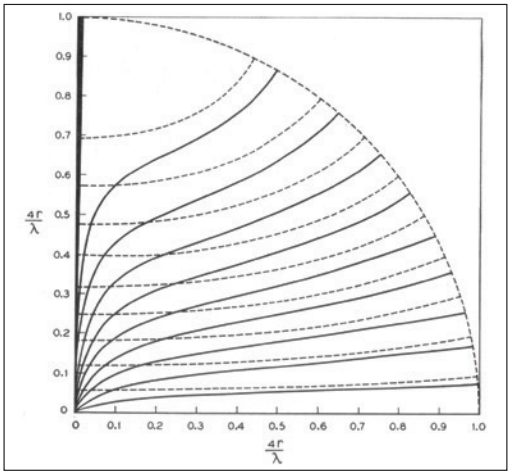

Figure 11a: Poynting vector direction as a function of position along the antenna and distance from the antenna. The solid lines are for an antenna element with a practical length-to-diameter ratio. The dashed lines are for a theoretical antenna element of vanishing diameter. (Reference 26, page 124)

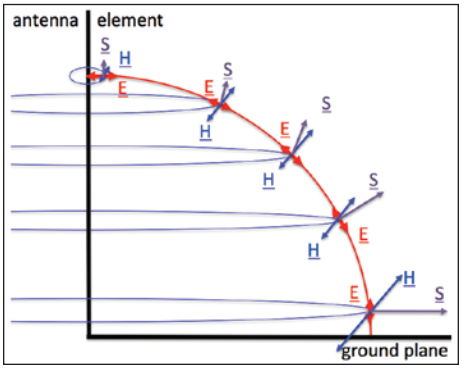

Figure 11b: The ordinate axis represents a quarter wave stub over the abscissa ground plane. Electric field lines are constrained to be at right angles to a perfect conductor. The orientation of the electric field and the circulating magnetic field sets up the Poynting vector direction, as shown in the direction of the two axes. Note that the current vanishes at the tip of the quarter-wave stub, so no current means the Poynting vector amplitude vanishes, as well.

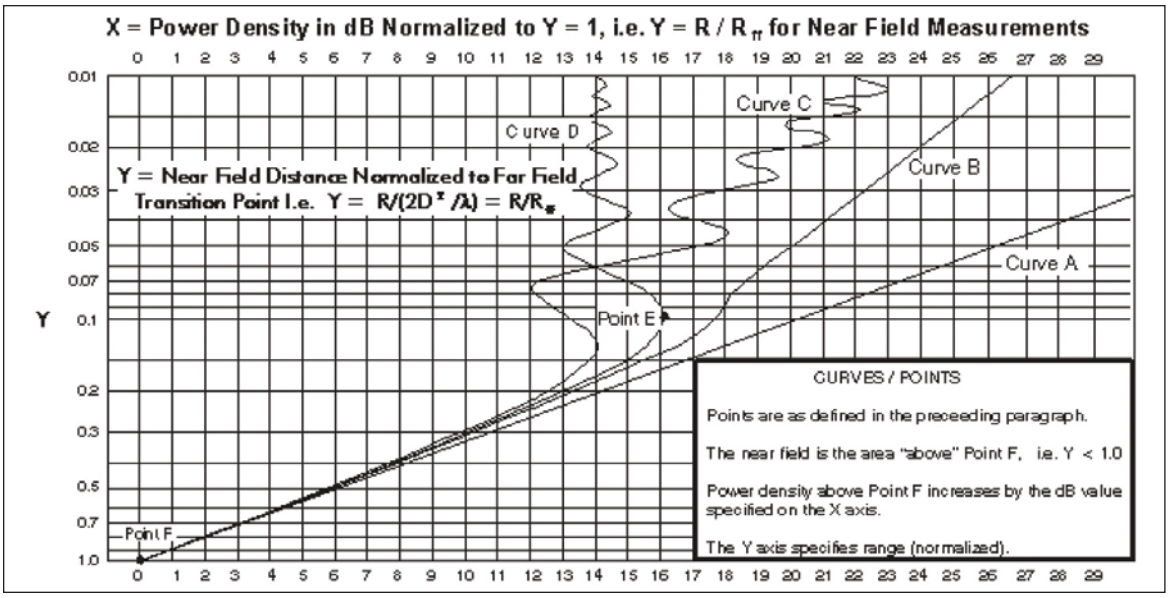

Figure 12: Fresnel zone power density from high gain aperture-type antennas normalized to the power density obtained at the far field boundary (copied from Reference 27).

of energy flow away from the antenna is different close to the antenna than farther away. Schelkunoff and Friis pointed this out long ago.[26] Figure 11a is copied from Reference 26 and shows the direction of energy flow (Poynting vector) away from the antenna element as a function of distance along the quarter-wave long antenna element itself and as a function of distance from the antenna. While the mathematics behind Figure 11a are complex, the notional Figure 11b drawing of the electric and magnetic fields from such an antenna provides an intuitive grasp.

The exact same effect is seen with higher gain antennas: gain derates rapidly from the far field values at separations less than a tenth of the far field distance ($2D^2/\lambda$).[27] Figure 12 is copied from Reference 27 and shows gain derating for both dish and horn aperture-type antennas. Figure 12 is used in the following manner.

Power density or equivalent field intensity is calculated using the far field gain at the $2D^2/\lambda$ far-field boundary. Then the appropriate curve is followed inward to the Fresnel zone distance of interest. Here there are no complicating near-field effects from capacitive or inductive coupling, and the quasi-static and inductive regions are contained well within the antenna feed point or phase center. They do not propagate down the waveguide to reach the antenna aperture itself.

The Reference 27 handbook citation is not the origin for this work. It goes back over sixty years and is hardly new.[28]

The fourth and final installment of this article will list theoretical misunderstandings arising from the erroneous substitution of field intensity for antenna-induced concepts and show the serious practical results of these theoretical mistakes.

ENDNOTES

23. One prominent physicist refers to what the author terms the "extreme near field" as "inside the dipole."
24. A complete mathematical treatment may be found in a companion article in this magazine issue, entitled "Journey To The Center Of The Dipole."
25. https://www.ets-lindgren.com/products/antennas?page=Products-Landing-Page
26. Schelkunoff, S.A. & Friis, *H.T. Antennas, Theory and Practice*, John Wiley & Sons, Inc. 1952.
27. NAWCAD TP 8347, *Electronic Warfare and Radar Systems Handbook*, October 2013
28. Hansen, R.C., and Bailin, L.L., "A New Method of Near Field Analysis," IRE Transactions on Antennas and Propagation, December 1959.

JOURNEY TO THE CENTER OF THE DIPOLE

Being an Account of Explorations Into an EMC-Forbidden Zone

By Ken Javor

The electrical engineering sub-discipline of electromagnetic compatibility has been described as the study of second-order effects that were ignored in college. Investigating electromagnetic fields next to a dipole is one such topic. Don't cite Hertz and his dipole – he didn't go there.

INTRODUCTION

This short article provides mathematical background for the longer "(Re)Discovering The Lost Science of Near Field Measurements" article presently serialized in this magazine.

This brief, lightly mathematical treatment demonstrates the true nature of the quasi-static electric and magnetic fields in the immediate vicinity of an excited dipole. The results are quite different than those presented in electromagnetics texts and electromagnetic compatibility handbooks.

ELECTROMAGNETIC RADIATION – BACKGROUND PRIMER

Classical physics tells us that electromagnetic radiation comes from accelerated electric charges. An accelerated charge (dI/dt or d^2Q/dt^2) requires the existence of both a moving charge (dQ/dt or I, current), and the charge itself, Q.

Beginning with a net static charge alone, there is a static electric field (Gauss & Coulomb). If the charge is moving at a constant rate – direct current – there is a magnetic field (Ampere and Biot-Savart). Finally, if the current changes with time, then there is induction and radiation (Faraday/Maxwell).

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HERTZIAN DIPOLE FIELDS

In equation set (1) – the fields of the Hertzian dipole – the $1/r^3$ contributions are from the static or quasi-static charge separation. The $1/r^2$ terms are from the induction field, and the 1/r terms represent the radiated fields.

$$\bar{E}_r = \frac{2I_0\,dl\cos\theta}{4\pi\varepsilon\omega}\left(-\frac{j}{r^3}+\frac{\beta}{r^2}\right)e^{-j\beta r} = \frac{2\beta^2\eta I_0\,dl\cos\theta}{4\pi}\left[-j\frac{1}{(\beta r)^3}+\frac{1}{(\beta r)^2}\right]e^{-j\beta r} \quad \text{Eqn. 1a}$$

$$\bar{E}_\theta = \frac{I_0\,dl\sin\theta}{4\pi\varepsilon\omega}\left(-\frac{j}{r^3}+\frac{\beta}{r^2}+\frac{j\beta^2}{r}\right)e^{-j\beta r} = \frac{\beta^2\eta I_0\,dl\sin\theta}{4\pi}\left[-j\frac{1}{(\beta r)^3}+\frac{1}{(\beta r)^2}+j\frac{1}{\beta r}\right]e^{-j\beta r} \quad \text{Eqn. 1b}$$

$$\bar{H}_\phi = \frac{I_0\,dl\sin\theta}{4\pi}\left(\frac{1}{r^2}+\frac{j\beta}{r}\right)e^{-j\beta r} = \frac{\beta^2 I_0\,dl\sin\theta}{4\pi}\left[\frac{1}{(\beta r)^2}+j\frac{1}{\beta r}\right]e^{-j\beta r} \quad \text{Eqn. 1c}$$

These equations are all derived from the expression of the vector potential equation for the field geometry of Figure 1.

APPLICATION LIMITATIONS

Equation set 1 – found in every electromagnetics textbook and EMC handbook – is based on Figure 1 and provides an inaccurate portrayal of the field very near the dipole. "Very near" means where the distance to the dipole is less than a few multiples of the dipole length itself. This is where, as we shall see, the classical Hertzian equations don't apply – as Hertz himself pointedly noted.

Hence, the way equation set (1) is most often interpreted within the EMC industry is simply wrong. Engineers (and textbook writers) look at these terms and say that, in close proximity to the antenna, the $1/r^3$ term will dominate. Then, moving out the $1/r^2$ terms, and then finally in the far field, all you have left is the $1/r$ term.[1] This implies that field intensities increase without bound as the dipole is approached – which is again simply wrong. This error in interpretation is based on ignoring a key limitation in the Hertzian dipole field equations' derivation. Furthermore, the Hertzian dipole amplitude relationships between quasi-static, induction, and radiation field expressions are unique to electrically

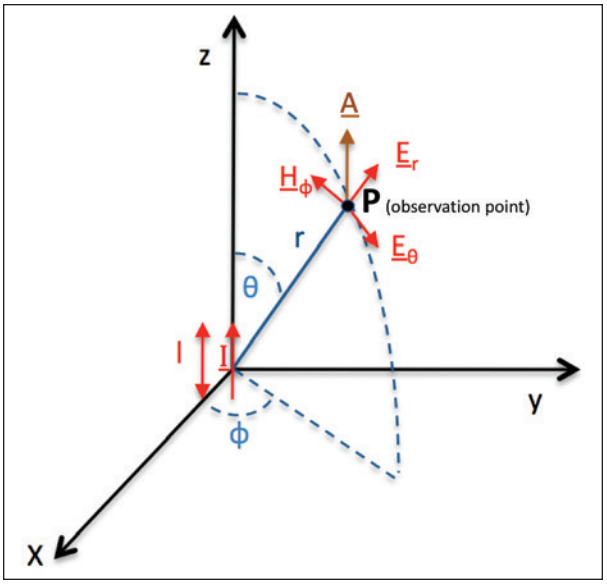

Figure 1: Geometry for calculating fields of Hertzian dipole (after Adamczyk). Dipole is at origin, oriented along the z-axis.

short dipoles. Paul warns that the boundary of near vs. far field is different for electrically-large antennas from that calculated for the infinitesimal dipole.[2] In fact, it is more complex than that. They are certainly different. But we also mean something completely different by far field when talking about electrically large antennas. This is described in the companion article on "(Re)Discovering the Lost Science of Near Field Measurements."

The relevant electric and magnetic field vectors are derived from the expression for the magnetic vector potential, which for the geometry of Figure 1 is:

$$A(P) = \frac{\mu_0}{4\pi} \int I\, dz/r, \text{ where } I = I_0 \cos \omega(t - r/c) \qquad \text{Eqn. 2a}$$

where the integral is evaluated over the length of the dipole oriented along the z-axis.[3, 4]

In order to derive the Hertzian equation set (1), the following simplifications are made (and dutifully ignored) within the EMC community:

The model is simplified such that the distance from the dipole to the point "P" in Figure 1 at which the field intensity is derived is so large with respect to the dipole length that it is the same from point P to any point along the dipole; and

Similarly, the dipole length is so short relative to wavelength that the current is constant along its length.

Given these two assumptions, the equation (2a) magnetic vector potential expression reduces to the much simpler equation:

$$A = \mu_0 Il/4\pi r \qquad \text{Eqn. 2b}$$

because both "r" and "I" are constant over the integration, and the integral of dz over the dipole length is just "l."[5]

If the vectors drawn from any point along a dipole to a point in space all have the exact same length, this is tantamount to making the dipole length zero – a point source. This is the basis of any far-field radiation pattern. Therefore, the Hertzian equations don't apply when the distance from the dipole is not a large multiple of the dipole's length, i.e., when we are in the very near field. A single EMC resource (FRC handbook) mentions that:

"The point that is frequently forgotten is that the validity of the statement made above (referring to the $1/r^n$ components of the Hertzian radiation predictions) depends entirely on the relation between (the distance to the point of observation and the size of the radiator). The statement holds when the (distance to point of observation is much larger than the dimensions of the radiator) …"

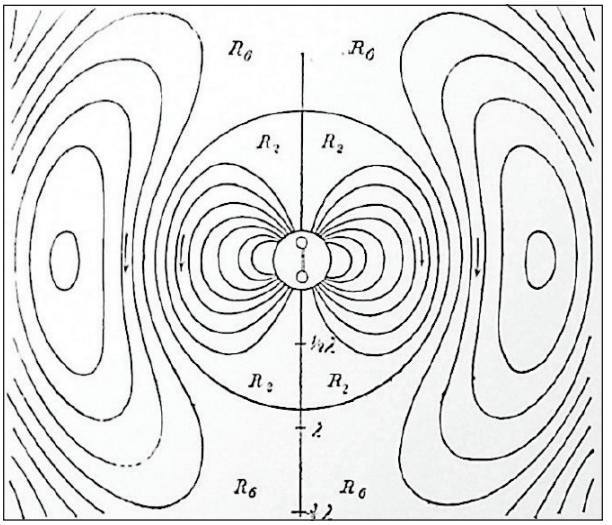

Figure 2a: One of Hertz's original drawings of the radiation from an electrically short dipole

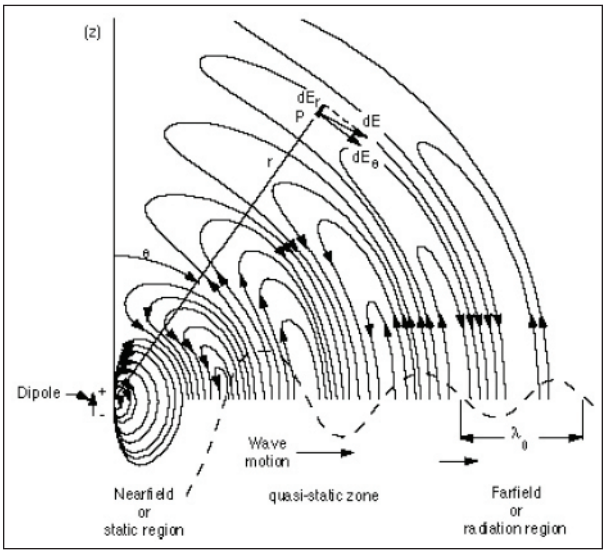

Figure 2b: Hertzian dipole geometry, copied from Johnk

It is worth stopping at this point and looking at Hertz' original derivation, both as to purpose and result.[6] The stated reason for the model and derivation is to prove that Maxwell's equations may be used to demonstrate that electromagnetic radiation arises from changing current on a wire. There is no mention of interest in the near field. When he produces a close cousin of what we today call the magnetic vector potential, with an inverse distance proportionality, he specifically states, "And it must be noticed that the equation referred to is satisfied everywhere, except at the origin of our system of coordinates."

Figure 2a is excerpted from the same paper and emphasizes the exception near the origin showing an exclusion zone drawn as a circle about the dipole, at which all the electric field lines start, or stop, depending on point-of-view. Explaining this, Hertz says:

> *"At the origin is shown, in its correct position and approximately to correct scale, the arrangement which was used in our earlier experiments for exciting the oscillations.[7] The lines of force are not continued right up to the picture, for our formulae assume that the oscillator is infinitely short, and therefore become inadequate in the neighborhood of the finite oscillator."*

Note that in the Figure 2b Johnk drawing (copied because it was about the best modern representation the author could find), no such exclusion zone is marked, and the inapplicability of the model in close to the dipole is left unremarked.[8]

Although, if the point source assumption is not made, the math rapidly becomes complex with the vector potential and its derivative electric and magnetic field vectors, it is very easy to compute the exact near field for the quasi-static electric and magnetic fields, for certain specific cases. So doing reveals the exact behavior of these fields at any distance from the dipole, including zero.

The quasi-static electric field is described by a $1/r^3$ distance dependence in equation set 1. The $1/r^3$ dependence is all that one can "see" looking in from a great distance, because of the assumption that the source is a point.

THE QUASI-STATIC ELECTRIC FIELD

The quasi-static electric field is described by a $1/r^3$ distance dependence in equation set 1. The $1/r^3$ dependence is all that one can "see" looking in from a great distance, because of the assumption that the source is a point. But if, instead of working from the outside inwards, we start at the source and work outwards, we get the whole story. This analysis is for simplicity limited to the field as a function of distance along a perpendicular through the dipole's center, as shown in Figure 3.

Coulomb's Law describes the field from each of the dipole charges: $E = kQ/r^2$.

The choice of P on the perpendicular bisector of the dipole means that the component of the electric field perpendicular to the dipole is zero, due to equal and opposite components from Q and –Q. Further, the vertical components are identical in magnitude and have the same direction, so that the vertical electric field component at P is twice what it would be from either charge alone.

$$E^{+,-}(P) = kQ\,(\cos\theta)/r_{1,2}^2$$

$$r_1 = r_2 = \sqrt{(R^2 + (D/2)^2)}$$

$$\cos(\text{angle at Q}) = (D/2) / \sqrt{(R^2 + (D/2)^2)}$$

$$\cos(\text{angle at -Q}) = (-D/2) / \sqrt{(R^2 + (D/2)^2)}$$

$$E^+(P_1) = \frac{kQ}{R^2 + (D/2)^2} \cdot \frac{(D/2)}{\sqrt{(R^2 + (D/2)^2)}} = \frac{kQD/2}{(R^2 + (D/2)^2)^{3/2}}$$

$$E^-(P_1) = \frac{-kQ}{R^2 + (D/2)^2} \cdot \frac{(-D/2)}{\sqrt{(R^2 + (D/2)^2)}} = \frac{kQD/2}{(R^2 + (D/2)^2)^{3/2}}$$

$$E_{net}(P_1) = E^+(P_1) + E^-(P_1) = \frac{kQD}{(R^2 + (D/2)^2)^{3/2}}$$

In the limit where R is large with respect to D, we can perform a factorization to see that, in that limit, the electric field depends on the inverse cube of distance:

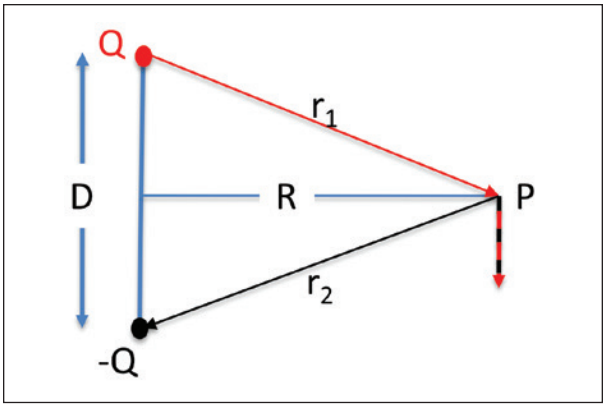

Figure 3: Geometry for the derivation of quasi-static electric field

$$E_{net}(P_1) = \frac{kQD}{(R^2 + (D/2)^2)^{3/2}} = \frac{kQD}{R^3(1 + (D/2R)^2)^{3/2}} \approx \frac{kQD}{R^3}, \text{ when } R \gg D$$

This is what we get for the quasi-static part of the Hertzian dipole electric field based on this same limiting case.

But we can play the same game in reverse where we factor out D and let the field point become very close to the dipole, where R<<D:

$$E_{net}(P_1) = E^+(P_1) + E^-(P_1) = \frac{kQD}{(R^2 + (D/2)^2)^{3/2}} = \frac{kQD}{(D/2)^3\,(1 + (2R/D)^2)^{3/2}}$$

Now when we let $R \to 0$, the electric field between the charges is simply:

$$E_{net}(P_1) = E^+(P_1) + E^-(P_1) = \frac{kQD}{(D/2)^3} = \frac{8kQ}{D^2}$$

which is a finite constant value exactly what the field would be computed down the length of the dipole midway between the two charges. Figure 4 shows the exact behavior, contrasted with the $1/r^3$ asymptotic behavior, which is only valid at long distances. It does not blow up in close, as per the conventional Hertzian dipole $1/r^3$ extrapolation. At a distance to dipole length ratio of two, the $1/r^3$ approximation is 3 dB high. In closer, the error grows without bound – note the vertical scale is delineated in decibels. Many EMC engineers routinely ignore such staggering errors in close or are simply ignorant of the true behavior.

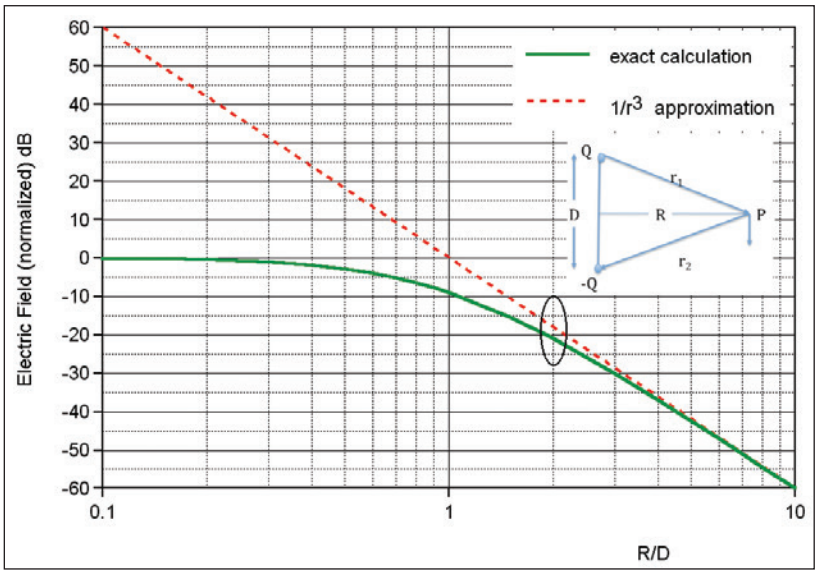

Figure 4: Exact and Hertzian dipole approximation of quasi-static electric field level perpendicular to the dipole through its center (values normalized to the electric field at the dipole's center)

The Hertzian dipole is a model, constructed for a particular purpose. It served that purpose admirably, and its shortcomings close to the dipole were noted by its author, and then dutifully ignored by generations of scientists.

THE QUASI-STATIC MAGNETIC FIELD

Per the Biot-Savart law, the magnetic field at point P from a current in the wire of Figure 5 is:

$$H = (I/4\pi) \int \frac{I\, dx \times a_r}{r^2} = (I/4\pi) \int \frac{I \sin\Theta\, dx}{r^2}$$

where the integral is taken down the length of the wire.

$$r^2 = R^2 + x^2$$

$$\sin\Theta = R/\sqrt{(R^2 + x^2)}$$

Therefore, the integral evaluates as:

$$H = 2(I/4\pi) \int \frac{R\, dx}{(R^2 + x^2)^{3/2}}$$

with limits of integration from 0 to D/2 (instead of –D/2 to D/2).

$$H = (I/2\pi R) \frac{x}{\sqrt{(R^2 + x^2)}} \Big|_0^{D/2} = \frac{I}{2\pi R} \frac{D/2}{\sqrt{(R^2 + (D/2)^2)}}$$

$$= \frac{ID}{4\pi R \sqrt{(R^2 + (D/2)^2)}}$$

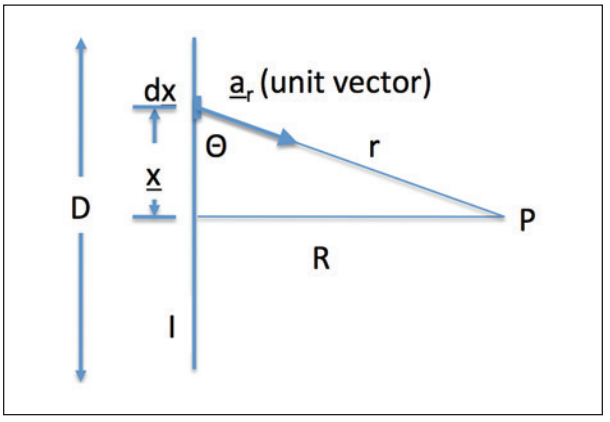

Figure 5: Geometry for calculating the magnetic field of dipole

We may factor R out from under the square root operator in order to investigate the asymptotic behavior as R increases without bound:

$$H = \frac{ID}{4\pi R^2 \sqrt{(1 + (D/2R)^2)}} \cong \frac{ID}{4\pi R^2} \quad \text{when } R >> D$$

This is the magnetic field dependence found from the Hertzian dipole derivation, with the dipole very short relative to the distance at which the magnetic field is measured.

But when the wire is long (D>>R), then the more useful factorization is:

$$H = \frac{ID}{4\pi R(D/2) \sqrt{(1 + (2R/D)^2)}} \cong \frac{I}{2\pi R} \quad \text{when } D >> R$$

which is the expected result (Ampere's Law) for the magnetic field close to a long wire.

CONCLUSION

There is nothing novel presented in this short primer, and the mathematics is at the high school and introductory integral calculus level. Yet the conclusion shows results many orders of magnitude different than those presented in electromagnetics and EMC texts, and as understood by generations of practicing EMC engineers.

The Hertzian dipole is a model, constructed for a particular purpose. It served that purpose admirably, and its shortcomings close to the dipole were noted by its author, and then dutifully ignored by generations of scientists. A model is an abstraction of reality, simplified so that analytical techniques may be fruitfully brought to bear (the proverbial spherical chicken in a vacuum). Although scientists claim their models are science, they are not science in the sense of basic principles. Einstein said that "everything should be made as simple as possible, but not simpler."

John von Neumann, commenting on attempts to model fluid flow using the relatively primitive computers in his day, said that "we are in danger of modeling dry water."

Engineers should likewise beware, and understand that the common wisdom, when confronted by common sense, must yield the floor.

ENDNOTES

1. While the static and quasi-static electric fields depend on charge, not current, the quotient I/ω in the expressions for E_r and E_θ substitutes for charge, given the time derivative relationship of the two and the assumed sinusoidal current dependence.
2. Much earlier works (Pierce 1920, Skilling 1942) use the word "doublet" instead of antenna. Given the specific meaning attributed to the term, the statement is then correct. A doublet means a charge separation distance that is very small compared to the distance at which the field is measured. In that case, as derived herein, the static field does decrease with the cube of distance. But close in to a doublet means far enough away that the approximation holds. That is several doublet lengths away.
3. Some authors (e.g., Adamczyk) state that the Hertzian dipole field quantities are appropriate for electrically large antennas as well as small ones. That this is not so is easily demonstrated qualitatively without any appeal to higher mathematics. Nothing is necessary but ordinary circuit theory and conservation of energy. Consider a signal source with 72 Ω output impedance, connected to a half-wave dipole (72 Ω impedance) through a 72 Ω balanced two-wire transmission

line. Now reduce the frequency by a factor of a thousand, so that the dipole is now λ/2000 electrical length. The antenna impedance is now effectively an open circuit. That means that the applied potential is twice what it was in the matched impedance configuration, but also the current is reduced by several orders of magnitude, because the impedance of an electrically short dipole is going to be numbered in the single to low double-digit picofarads, and present an impedance on the order of tens to hundreds of kiloohms. With no current into the dipole, there is no power delivered to it, and if no power is delivered, none can be radiated. Thus, with an identical dipole structure, only changing the driving frequency, we can see that the ratio of the traveling wave electric field to the quasi-static electric field is orders of magnitude higher with a half-wave dipole than with a Hertzian dipole.

4. Time dependence is critical here. If time dependence doesn't exist, we have the static case. If we have time dependence, but no retarded time, we have the quasi-static and induction case. The retarded time term (t-r/c) gives rise to radiation. This was noted in but one EMC text, the half-century-out-of-print FRC Handbook, Volume 1.
5. Equation set 1 is derived from an expression for the magnetic vector potential, commonly designated A. In EM texts the magnetic vector potential is typically introduced via vector calculus manipulations, i.e., as an entirely mathematical construct. In fact, the magnetic vector potential has a physical meaning that becomes clear using dimensional analysis. We will explore that meaning via an analogy to the commonly understood concept of electrical potential, or voltage.

   The unit of electrical potential, the volt, is the per unit charge energy stored in a set of charges. In the SI measurement system, it has units of joule/coulomb. Since the magnetic vector potential is defined by the equation

   $B = \nabla \times A$

   the dimensional analysis relationship of magnetic flux density to magnetic vector potential is the same as for electric field to electric potential. That is, electric potential is in volts, and its gradient the electric field has units of volts per meter or newtons per coulomb. Similarly, magnetic vector potential is a weber per meter, and the magnetic flux density is a weber per square meter (or Tesla). And a weber per meter is dimensionally equivalent to a joule per amp-meter. So, the analogy between the unit of electric potential and magnetic vector potential is that they are measures of energy per unit of charge (electric) and per unit current (magnetic), with the necessary addition of the length factor, because current is charge movement in a conductor, and that conductor has both length and direction: hence the vector nature of the magnetic potential.
6. Equation set 1 is derived from (2b) using vector calculus relations between the magnetic vector potential and the electric and magnetic fields themselves. This derivation is presented in every text on electromagnetics, antennas, and EMC, and will not be repeated here in extent. Adamczyk provides the most detailed, step-by-step derivation in the author's experience.
7. "The Forces of Electric Oscillations, Treated According to Maxwell's Theory," published in 1889 is the paper where the Hertzian dipole model and derivation first appear. The point of the exercise was to show that the received signal was indeed radiated, and not coupled via capacitive or inductive means. Hence Hertz needed to show that given the separation between his transmitting and receiving apparatus, the radiation term dominated.
8. Here Hertz references the experiment generating electromagnetic radiation intentionally for the first time, for which achievement of the unit of frequency is given his name.
9. Similarly, Adamczyk considers the dipole to be at the origin, ignoring its length. Later, he states that the equation set (1) apply at any distance r from the dipole. This modern treatment is in distinct contrast to earlier texts, such as Pierce, where the dipole was carefully and precisely described as an oscillating doublet, as noted in endnote (2).

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RETURN-CURRENT DISTRIBUTION IN A PCB MICROSTRIP LINE CONFIGURATION

Part 2: Reference Plane with Discontinuities

By Bogdan Adamczyk and Scott Mee

This is the second article of a two-article series devoted to the return current distribution in a PCB microstrip line configuration. The previous article [1] presented the CST simulation results in the case of a solid reference plane. This article addresses the case where the reference plane contains several discontinuities: edge slot, internal slot, slot holes, and via cutouts.

1. BASELINE RESULTS

In [1], we presented the baseline results for a solid reference plane and showed the return current path (forward current trace is hidden) flowing in the reference plane at different frequencies.

The results showed that at 10 Hz the return current spreads wide over the reference plane, flowing both

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Scott Mee is a co-founder and owner at E3 Compliance which specializes in EMC & SIPI design, simulation, pre-compliance testing and diagnostics. He has published and presented numerous articles and papers on EMC. He is an iNARTE certified EMC Engineer and Master EMC Design Engineer. Scott participates in the industrial collaboration with GVSU at the EMC Center.

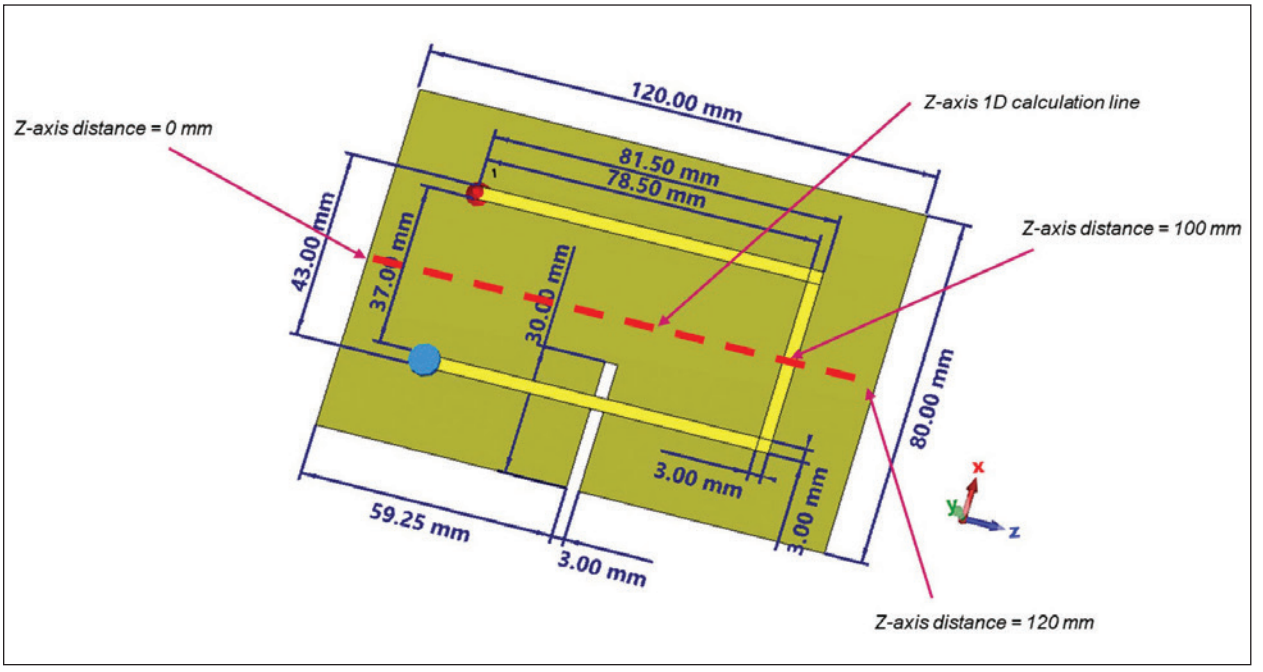

Figure 1: CST Model – Two-layer PCB with an edge slot in the reference return plane

under the top trace and directly from the load port to the source port. As the frequency increases to 100 Hz, more of the return current flows under the trace (with a narrower spread), and less of it flows directly from the load port to the source port. This trend continues as the frequency increases to 1 kHz. As the frequency increases beyond 10kHz, the return current path remains virtually unchanged, predominantly flowing beneath the forward trace. In other words, the return current path and current density no longer depend on frequency.

The results were confirmed by plotting the normalized current distributions.

2. PCB WITH EDGE SLOT

Figure 1 shows the CST Studio model of a two-layer PCB with an edge slot in the reference plane.

Figure 2 shows the return current path (forward current trace is hidden) flowing in the reference plane at different frequencies.

The results show that the edge slot forces current to go around it and flow in a larger loop (higher inductance). The return current exhibits the frequency-dependent behavior similar to the solid reference plane case.

At lower frequencies (below 1 kHz), the return current spreads wide over the reference plane, flowing both under the top trace and directly from the load port to the source port. This trend continues as the frequency increases to 1 kHz. As the frequency increases beyond 10 kHz, the return current path remains virtually unchanged, predominantly flowing beneath the forward trace, the return current path and current density no longer depend on frequency.

This is confirmed by the normalized current distributions shown in Figure 3.

3. PCB WITH INTERNAL SLOT

Figure 4 shows the CST Studio model of a two-layer PCB with an internal slot in the reference plane.

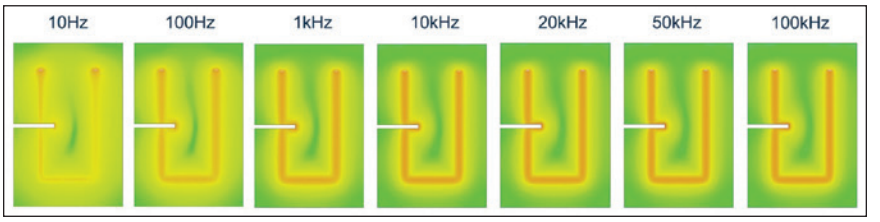

Figure 2: Edge slot - return current path at different frequencies

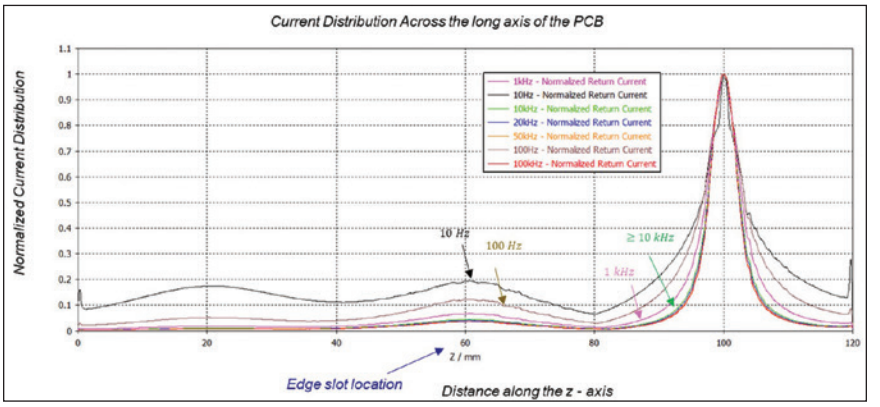

Figure 3: Edge slot - normalized current distributions at different frequencies

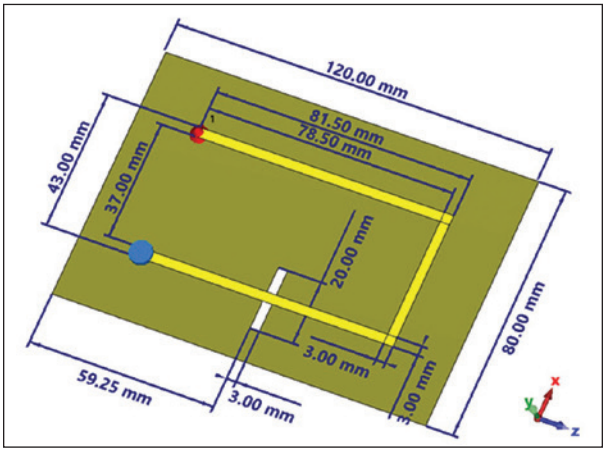

Figure 4: Internal slot in the reference return plane – CST model

Figure 5 shows the return current path flowing in the reference plane at different frequencies.

The results show that current returns around both sides of the slot and thus does not 'bulge' as much as the edge slot case. The return current exhibits the frequency-dependent behavior similar to the edge slot and the solid reference pane case. As the frequency increases beyond 10 kHz, the return current path remains virtually unchanged, predominantly flowing beneath the forward trace, the return current path and current density no longer depend on frequency.

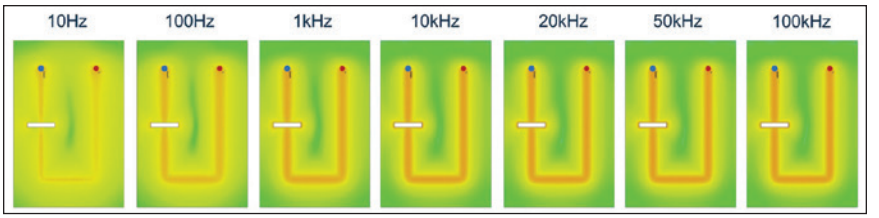

Figure 5: Internal slot - return current path at different frequencies

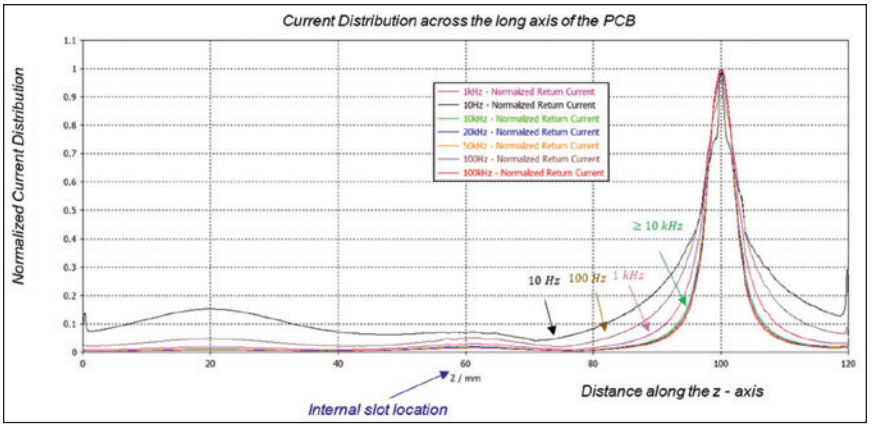

Figure 6: Internal slot - normalized current distributions at different frequencies

This is confirmed by the normalized current distributions shown in Figure 6.

4. PCB WITH SLOT HOLES

Figure 7 shows the CST Studio model of a two-layer PCB with slot holes in the reference plane.

Figure 8 shows the return current path flowing in the reference plane at different frequencies.

The impact of the holes is minimal compared to the solid reference plane case. Return currents are permitted to flow between and around the holes and therefore the current does not bulge away from the return path out toward the middle of the PCB. The results are very similar to the previous cases: as the frequency increases beyond 10 kHz, the return current path remains virtually unchanged, predominantly flowing beneath the forward trace, the return current path and current density no longer depend on frequency.

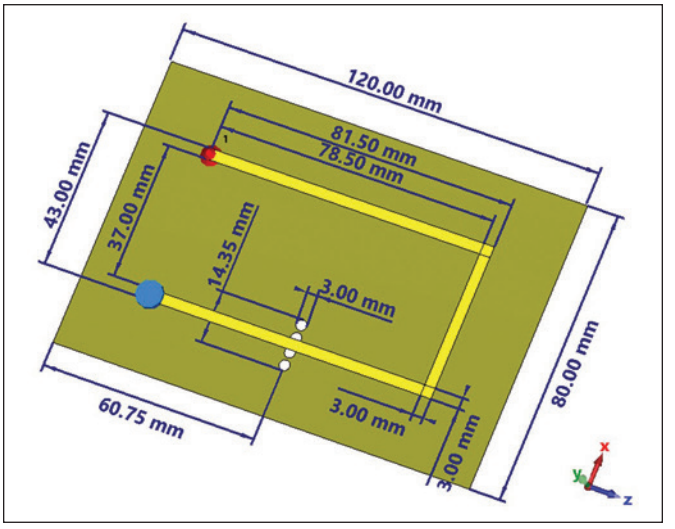

Figure 7: Slot holes in the reference return plane – CST model

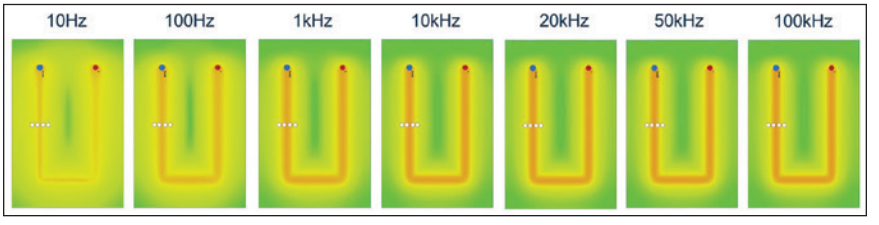

Figure 8: Slot holes - return current path at different frequencies

This is confirmed by the normalized current distributions shown in Figure 9.

5. GROUND VIA CUTOUTS

Finally, we investigate the PCB with several ground via cutouts. Figure 10 shows the CST Studio model.

Figure 11 shows the return current path on the reference plane at different frequencies.

The results are similar to the previous cases and are confirmed by the normalized current distributions at different frequencies, shown in Figure 12.

CONCLUSIONS

Ground plane discontinuities do affect the return current path to various degrees by increasing the loop area, and thus increasing the inductance. In all cases, however, the return current exhibits very similar frequency-dependent behavior. As the frequency increases beyond 10 kHz, the return current remains virtually independent of increasing frequency. IN

REFERENCE

1. Bogdan Adamczyk and Scott Mee, "PCB Return-Current Distribution in a PCB Microstrip Line Configuration, Part 1: Solid Reference Plane," *In Compliance Magazine*, August 2023.

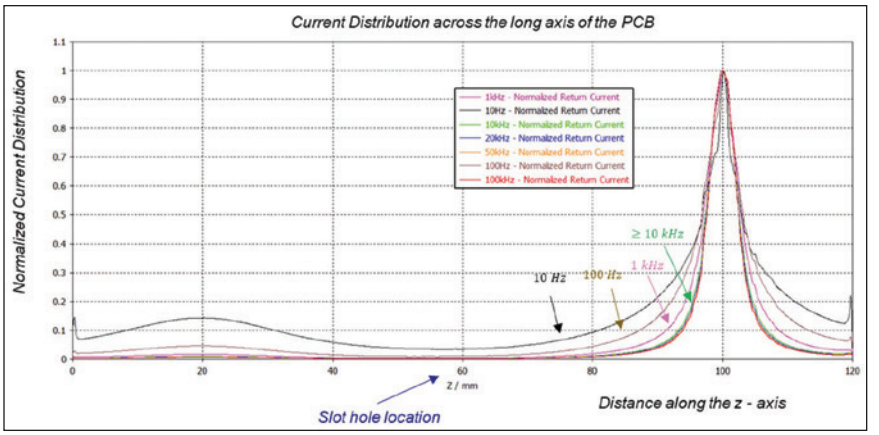

Figure 9: Slot holes - normalized current distributions at different frequencies

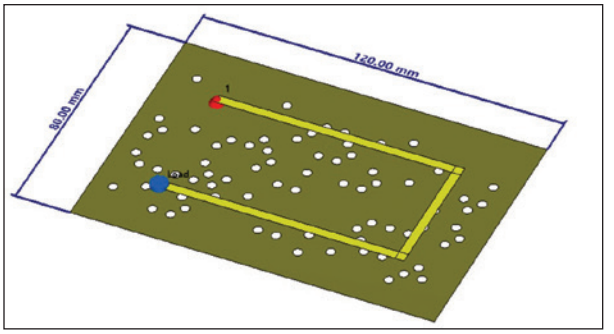

Figure 10: Two-sided PCB with via cutouts in the reference plane

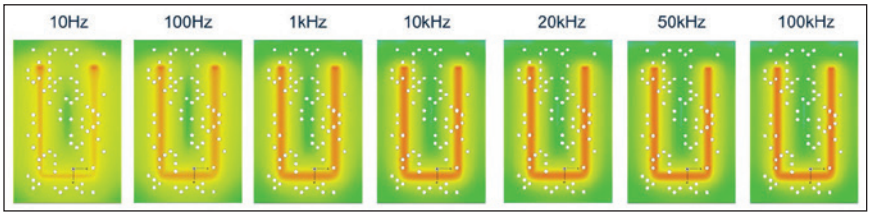

Figure 11: Ground via cutouts - return current path at different frequencies

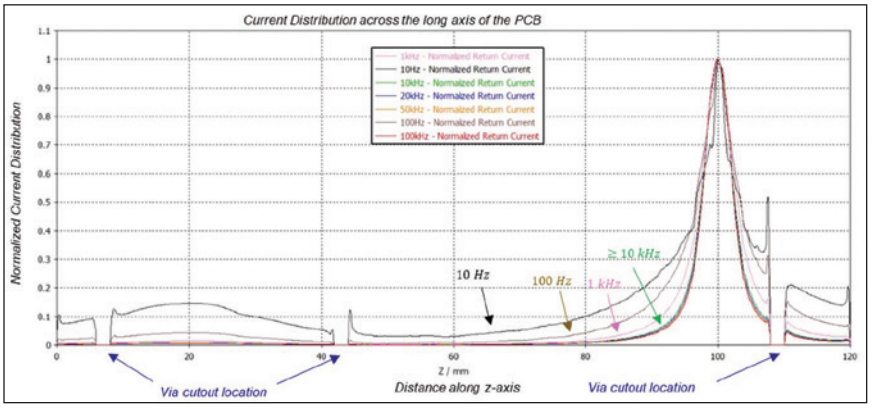

Figure 12: Ground via cutouts - normalized current distributions at different frequencies

CAN ELECTROSTATIC DISCHARGE DESIGN PROBLEMS BE SOLVED WITH ELECTRONIC DESIGN AUTOMATION TOOLS ALONE?

Part 2: What are the limitations of EDA tools?

By Michael Khazhinsky, Eleonora Gevinti, Krzysztof Domanski, Guido Quax, and Matthew Hogan for EOS/ESD Association, Inc.

In Part 1 of the article, we reviewed what EDA tools are good for. Here we will discuss EDA tool limitations.

A complete ESD solution is never made by EDA tools alone. Certain ESD design aspects are so specific for a product that it does not pay to make an EDA code for it (although it could fundamentally be done).

ESD is a complex phenomenon and ESD design verification involves checking a wide range of initial conditions and requirements (e.g., available area, stress tests validations conditions, single or cumulative stresses, special bonding or package conditions, external metallization levels, etc.). These require special inputs and appropriate initializations in EDA tools which often prevents ESD EDA from being a push-button solution. ESD protection strategies vary, and an EDA tool cannot always establish a priori the best strategy out of several existing ones.

Many ESD events are characterized but not properly modeled. An example is a parasitic thyristor or bipolar which is triggered during ESD stress (Figure 1). There is no "full" model available which can be integrated into an EDA tool. The trigger and holding properties of the device (V_{t1} and V_H in Figure 2 on page 52) depend on the geometry, the substrate currents, and many other parameters. The ESD designer, however, can still manage the design by interpolation of test structure data, or rely on experience from previous products. This "data gap" sets a fundamental limitation to the use of EDA tools for complete ESD design.

It is important to use the most suitable type of EDA tool for a given verification task.

Static ESD checks are based on predefined, hard-coded ESD rules. The rules are usually defined with worst-case assumptions that can lead to over-engineering and unnecessary design margins. Moreover, the ESD rules encoded in static check tools are usually suitable for typical driver architectures or power-supply protection. Custom ESD codesign (e.g., for specialized high frequency, mixed voltage, fail-safe, or low leakage designs) may not be supported by standardized

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Founded in 1982, EOS/ESD Association, Inc. is a not for profit, professional organization, dedicated to education and furthering the technology Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, tutorials, and foster the exchange of technical information among its members and others.

static checks. For those non-standard interfaces, the ESD codesign relies on electrical simulations of circuit performance with the ESD network for better matching. The utilization of static checks may not guarantee the required circuit performance.

Dynamic ESD checking tools are more suitable for the ESD codesign. These tools perform ESD circuit simulations using regular schematics or schematics with extracted s-parameter or resistive networks. These simulations require the expertise of a design

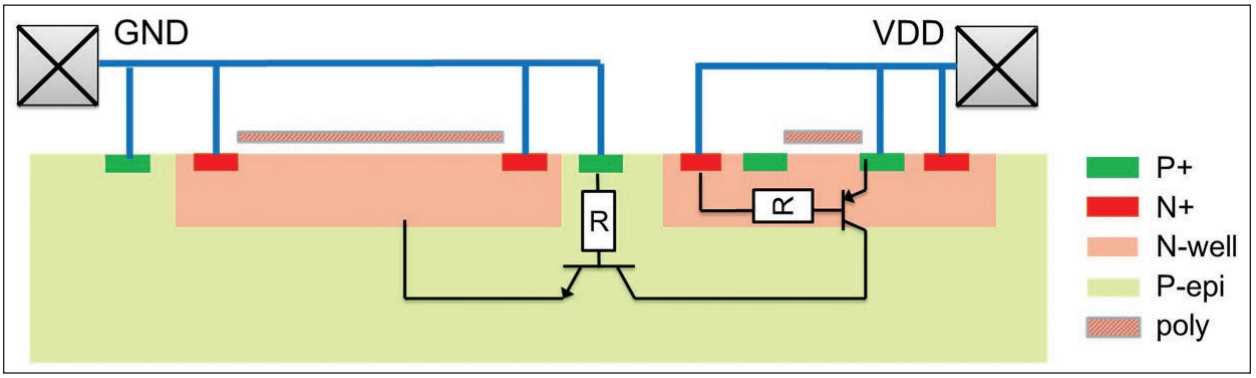

Figure 1: Cross-section of a parasitic thyristor between a PMOS at VDD and a grounded n-well cap. This phenomenon is well-known, but prediction of the exact trigger point and holding voltage is hard due to the many parameters involved.

engineer and ESD specialist to correctly set them up and analyze the results.

Still, dynamic EDA tools run into multiple limitations, especially when simulating ESD events for full chips rather than special IPs. These limitations are especially obvious when meeting complex ESD requirements, such as Charge Device Model (CDM) ESD in low-cap high-frequency design [1].

Current paths in bulk and metallization are not always accurately assessed. For example, the fast CDM current transients in the range of even 20-300ps in power and ground line cause voltage overshoots on inductance of metal lines. Contemporary dynamic ESD simulators are not capable of performing inductivity extraction for the power and ground mesh on a full chip or even a large power mesh. Thus, dynamic CDM simulations might be inaccurate or executed only on a part of the IP.

While the energy of CDM discharge usually stays the same for different pins, the waveform shape can vary significantly for different pins. Package trace can change its duration between 0.5-2ns [2]: for longer CDM pulses, current magnitude will be reduced to maintain the same energy. Different circuit components may be sensitive to either higher voltage drop originating due to higher current, or higher thermal dissipation during longer CDM discharge pulse. Setting appropriate voltage/current limits in the simulation/verification poses additional EDA challenges.

In conclusion, defensible design decision-making is data-driven. We may not always have all the data that we want, but understanding design margins and areas of risk (particularly during IP design and full-chip assembly) is key to providing guidance for the creation of robust and reliable IC designs. ESD engineers often provide that guidance to circuit and layout designers. Over the last decade, EDA tools and the coverage that sign-off EDA rule decks provide have come a long way in creating a robust baseline for reliability (especially in the field of ESD) for full-chip designs where simulation and less robust techniques (visual inspection) are not practical or advisable [3]. Some of these rule decks are provided by foundries. For those companies that do not prescribe to foundry-provided methodologies, many have invested in automating

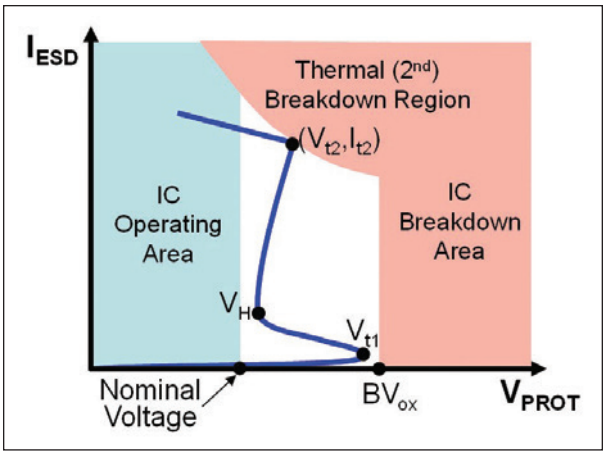

Figure 2: Trigger and holding characteristic in a generic ESD design window [3].

checks themselves, based on their own custom criteria. There will always be corner cases and requests to waive a specific rule as part of larger design considerations. EDA tools significantly improve productivity and confidence within the design community, but there will always be a need for specialist oversight and evaluation of results against reasonableness and provide professional judgment for waivers. This is particularly true for results that are close to or failing agreed-upon design margins. EDA Tools alone? No! But coupled with capable engineers, EDA tools provide an incredible productivity gain and insight into at-risk areas of IC designs.

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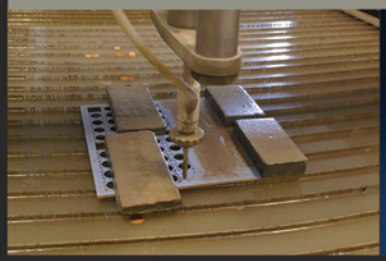

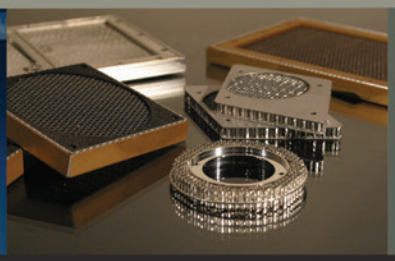

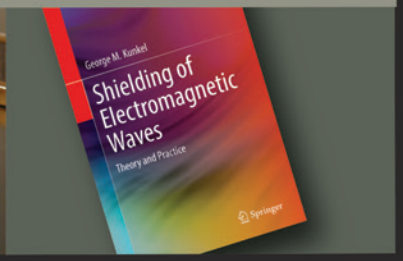

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