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In Compliance Magazine
ISSN 1948-8254 (print)
ISSN 1948-8262 (online)
is published by

Same Page Publishing Inc.
451 King Street, #458
Littleton, MA 01460
tel: (978) 486-4684
fax: (978) 486-4691

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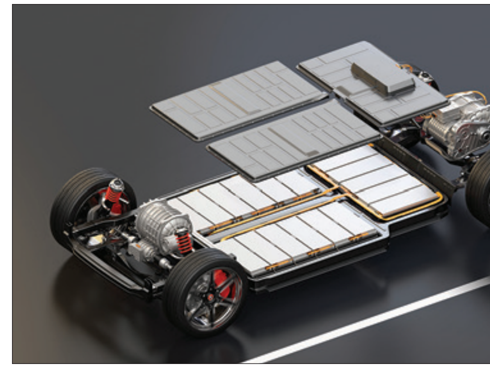
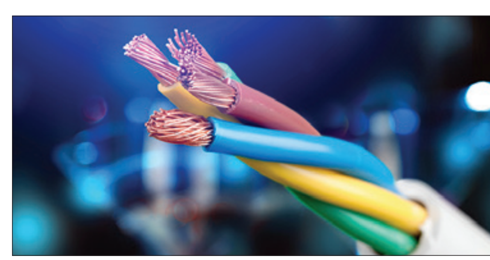
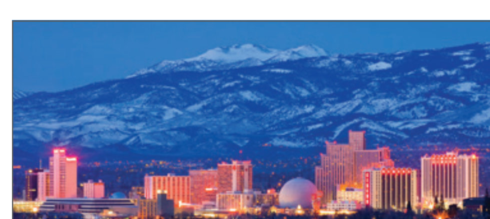
SEPTEMBER 2022 CONTENTS

Volume 14 | Number 9







EU Commission Publishes Updated "Blue Guide" on Product Rules

The Commission of the European Union (EU) has recently published an updated version of its guide on the application of EU rules and regulations to a wide range of products.

The EU's "Blue Guide on the implementation of the product rules 2022" provides a detailed explanation of current regulations applicable to toys, measuring instruments, radio equipment, low voltage electrical equipment, medical devices, and other types of products. The Blue Guide offers readers explanations and non-binding advice on navigating the EU's conformity assessment systems, CE marking requirements, and market surveillance activities.

The Blue Guide was originally published in 2000 and was most recently updated in 2016. According to a Commission press release, the current revision represents "a substantial update" to prior editions, addressing the specifics of the EU's Market Surveillance Regulation (2019/1020) and expanding on information not previously available.

FDA Launches New Premarket Submissions Tracker

The U.S. Food and Drug Administration (FDA) has now made available an online platform for uploading and tracking the progress of premarket submissions for medical devices.

According to a posting on the FDA's website, the updated Customer Collaboration Portal went live in mid-July and now allows medical device manufacturers to upload medical device submission files for 510(k) and De Novo applications in both eSTAR and eCOPY formats. This eliminates the need for device manufacturers to create and mail compact discs or flash drives to the FDA.

Once files have been uploaded, a manufacturer's designated "Official Correspondent" can then access the Portal to track the progress of their submission.

The updated Customer Collaboration Portal is in its trial phase, and the FDA is actively soliciting feedback on its use from submitters.

New EMC Standard Takes Effect in China

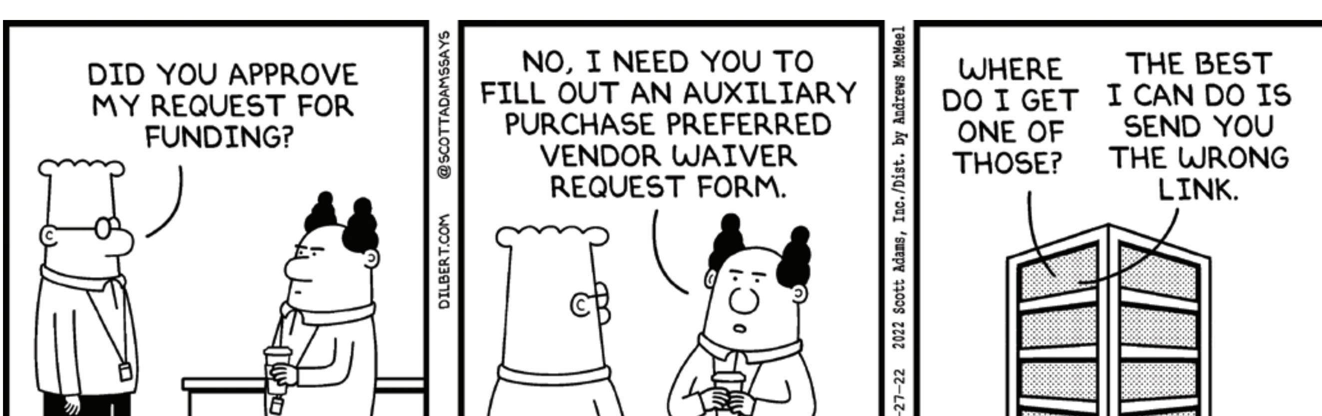
A new EMC standard is now in effect in China. The new standard, GB/T 9254.1-2021, "Information technology equipment, multimedia equipment and receivers—Electromagnetic compatibility—Part 1: Emission requirements," is the equivalent of CISPR 32:2015, the internationally-accepted standard for EMC. The new standard replaces the former version of the standard (GB/T 9254-2008) as well as GB/T 13837-2012.

The new standard includes more supplementary tests for certain AV products, including power supplies. As such, the standard's release is expected to impact manufacturers of devices that have previously received China Compulsory Certification (CCC).

More Crackdowns on Pirate Radio Operations

The U.S. Federal Communications Commission (FCC) is continuing its aggressive enforcement efforts to restrict unlicensed radio operations and illegal pirate radio broadcasts.

In one day, the FCC's Region One Enforcement Bureau issued five separate notices to individuals linked to illegal pirate radio broadcasting in the greater New York metro area. Each of the recipients was notified of their potential liability for financial penalties of up to $2 million for continuing their illegal broadcasting operations and instructed to confirm with the FCC that such broadcasting activities had ceased.



WEF Releases 25 Facts About Recycling Efforts

Seeking to fill the void with updated information about the current state of global recycling efforts, the World Economic Forum (WEF) has compiled some recent facts and statistics on how we're progressing in this important initiative.

The WEF findings were reported in their article, "Top 25 recycling facts and statistics for 2022," posted on the WTF website. Unfortunately, the news is not good!

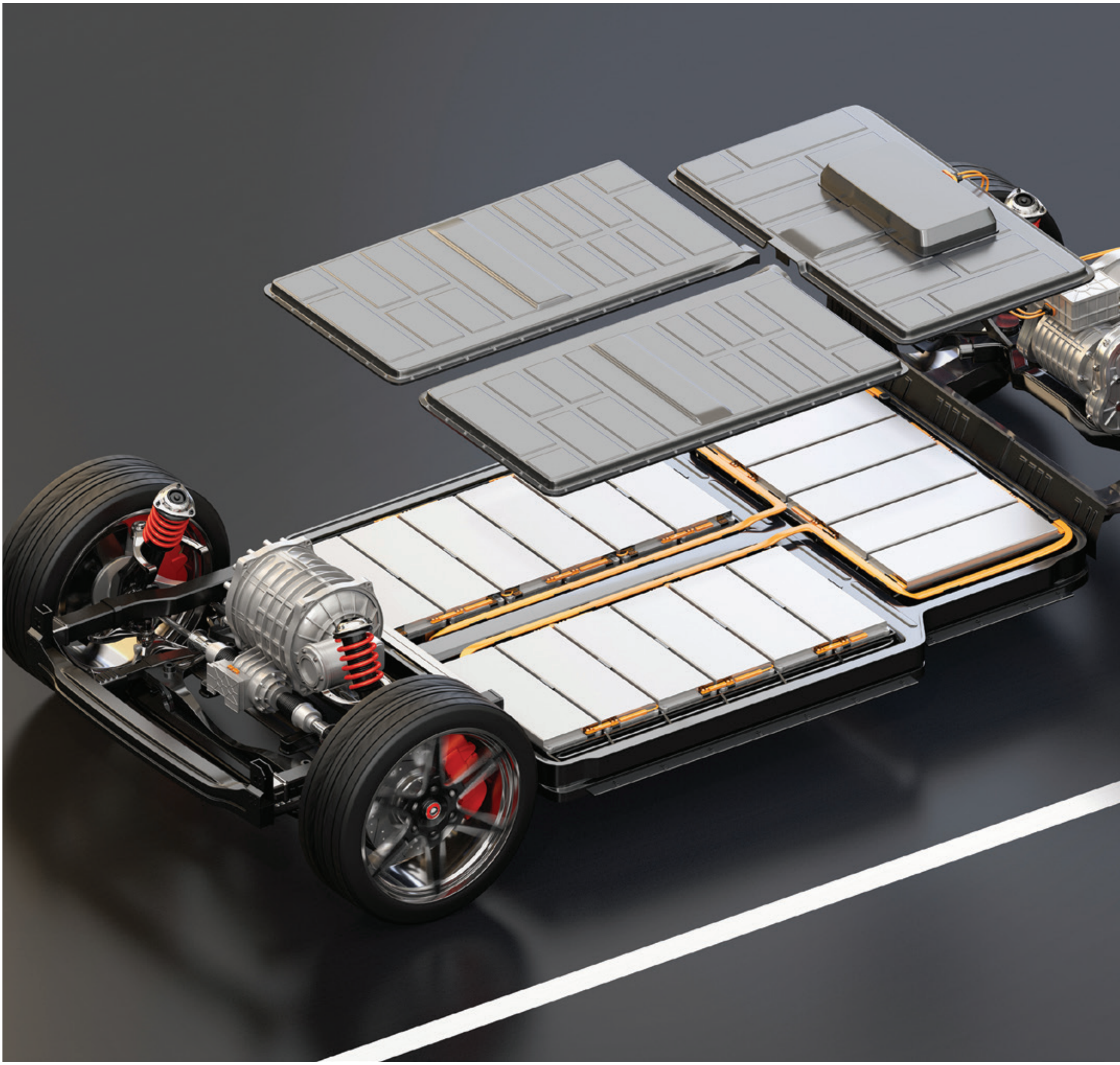
Here is a brief summary of the "lowlights" of their report:

- The world produces about 400 million tons of plastic waste a year, but we're recycling plastic at lower than previously estimated rates. In the U.S., in 2021, we recycled just 2 million tons of the estimated 40 million tons of plastic waste generated, about 5-6% of the total.
- Electronic waste (e-waste) is the fastest-growing source of waste globally. E-waste volumes increased to 53.6 million tons in 2019, an estimated 21% increase in just five years. Yet, only about 17% of discarded e-waste was recycled in 2019.
- The rate of E-waste recycling in the U.S. is trending even lower than global efforts. Only about 15% of the estimated 5 million tons of e-waste discarded here in 2019 was recycled.
- The largest category of waste reported is related to chronic food misallocation and inefficiency. The WEF reports that 40% of the food produced globally is wasted, enough to feed every unnourished person in the world four times over. Further, food waste generates around 10% of global greenhouse gas emissions.

On the plus side, the WEF reports that aluminum and paper recycling efforts have gained the most traction in recent years. Currently, aluminum accounts for only 1% of the U.S. waste stream, despite steady growth in the demand for and consumption of the material. And paper and paper products such as corrugated cardboard achieved a 68% recycling rate in 2021.

LARGE FORMAT CELL TESTING FOR ELECTRIC MOBILITY APPLICATIONS

Challenges and Best Practices for Cell-Level Testing



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By Michael C. Strzepa

The lithium-ion cell is the heart of the modern-day electric vehicle. Proper cell selection, supported by analysis and testing, can make or break a vehicle's performance in the market. Consumer concerns of range anxiety, performance in extreme climates, and long-term reliability directly translate into brand image and warranty costs for producers.

This article will review some of the challenges and best practices associated with cell-level testing. Although the focus is on electric vehicle applications, the material presented shares applicability with other market segments in electric mobility as well as energy storage applications, both residential and grid-level.

THE CELL-TO-VEHICLE HIERARCHY

When considering an electric vehicle as a system, there is a natural hierarchy to the key components that enable the vehicle's electrification. In simple terms, it all begins with the cells. Cells, in turn, are integrated into modules. Modules are combined to produce a battery pack. Finally, the battery pack is merged with other key components of the drive train comprising the motive aspects of the vehicle.

Although this sounds simple in concept, the reality is that any modern electric vehicle is a highly complex device fabricated from thousands of parts that is expected to perform safely in a multitude of stressful environments over the course of a relatively long lifetime and with minimal maintenance and repair. To achieve such lofty goals, a rigorous process of designing and testing the vehicle and its electrification subsystem must be faithfully followed. Not doing so risks the loss of life, property damage, and corporate liability, including financial losses and negative impacts on a company's brand.

Note the criticality that cell testing plays in the hierarchy shown in Figure 1. The output data provides actionable information on upstream system performance. Individual cell storage and cycling aging behavior will define the corresponding module life performance, affecting the projected vehicle performance. For example, an early cell performance issue caught in the concept validation (CV) phase can drive changes in the pack, the battery management system (BMS), or even vehicle performance or warranty targets. This build-test-optimize flow is a

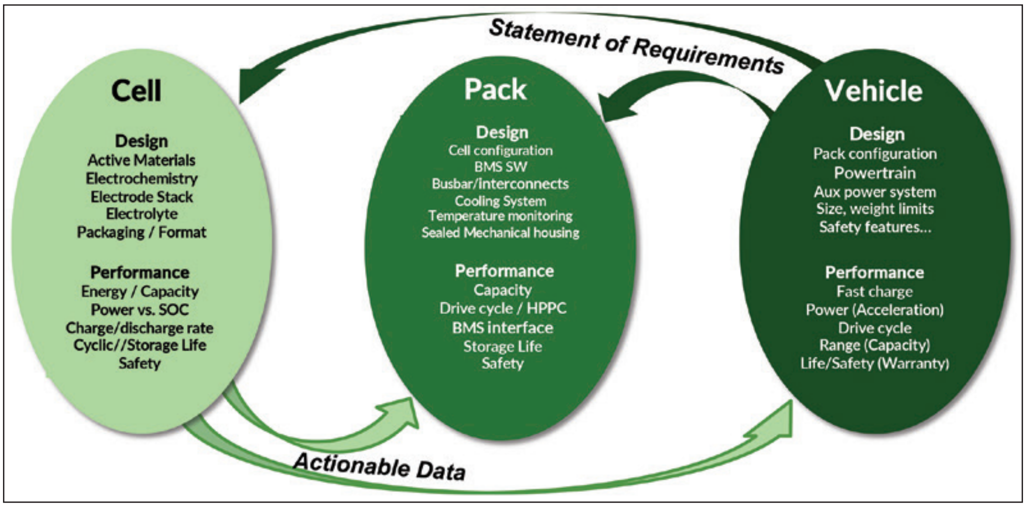


Figure 1: EV design definition and optimization flow

cycle that works in both directions, from component to higher-level systems, but also “top-down,” from vehicle level down to the cell.

Testing and evaluation specific to the design and use of the cells can be evaluated and fed back into a design and validation loop. Think about this process as a way to complete multiple iterations early in the program to identify potential problems and validate proposed solutions for that design and future designs. This may seem complicated, but there is a structure that EV program teams use to carefully manage this maturation process.

STRUCTURE OF THE EV PROGRAM DEVELOPMENT

The validation testing of a vehicle system follows a sequence of development maturity phases known as advanced product quality planning or APQP for short. APQP is a well-established methodology followed by the automotive industry (and many others) for developing a new product intended for high-volume manufacturing and under strict quality levels, schedules, and cost targets.

Figure 2 outlines the phase gate maturity levels managed throughout a program’s lifecycle. Note the high degree of variability in test validation plan durations.

APQP Phases	Phase 0 Cell R&D	Phase 1 Plan and Define	Phase 2 Product Design and Dev.	Phase 3 Process Design and Dev.	Phase 4 Product & Process Valid.	Phase 5 Production
AIAG Phase	N/A	Program Approval	Prototype	Pilot	Launch	Production
Sourcing Status	Cost Estimation	Prototype Sourcing	Production Sourcing Strategic -> Component-> Commodity			Value Eng.
Phase Duration	3-6 mos	3-9 mos	6-12 mos	6-12 mos	3-6 mos	2-5 yrs
	Note: Cell validation test duration can be up to 3.5 yesrs					
Key Cust. Activities	Sourcing-> Kick-off	System Dev.	Design Reviews	Process Reviews	Ramp / Interim PPAP	Yearly Project Health Review
Key Core Activities	Roadmap Alignmt.	Concept Dev.	Design Validation	Process Validation	Ramp / Interim PPAP	Yearly Project Health Review
Test Valid. Deliverables	Pre-CV Test Results	CV Test Results DV Test Plan	DV Test Summary / Issues PV Test plan	Key PV Tests complete	PV Test Summary / Issues	

Figure 2: APQP phase gate overview

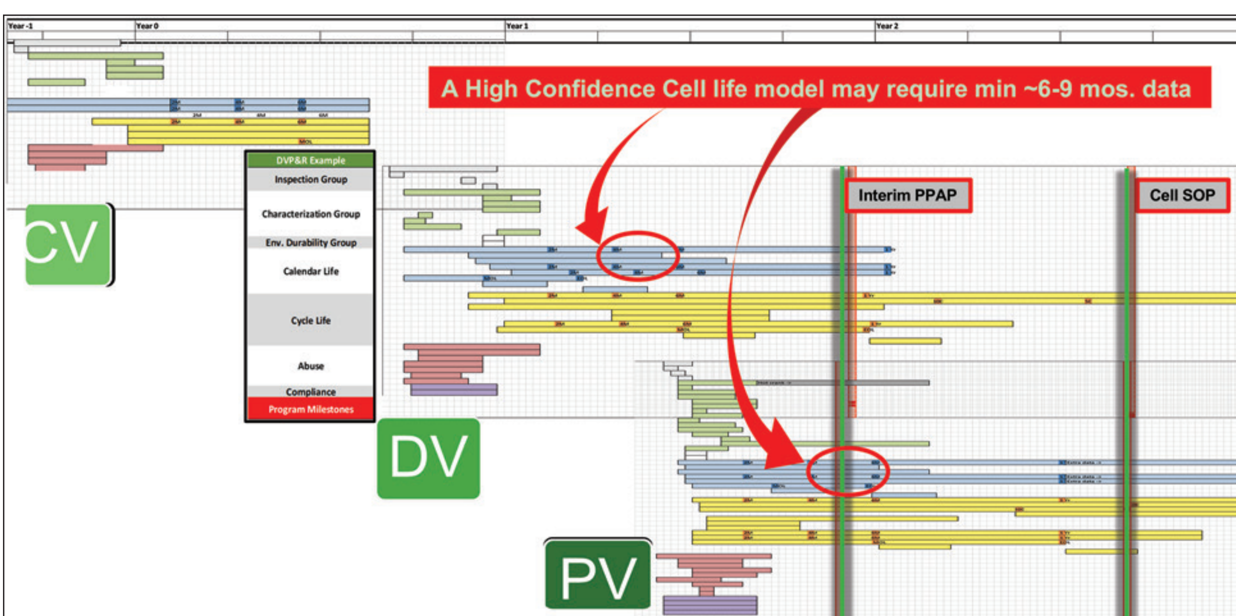


Figure 3: Example of CV/DV/PV test plan schedule

Beginning with concept validation (CV or A-sample) and running through process validation (PV) and the full production part approval process (PPAP), the validation duration may exceed three years. The full scope of an EV program requires an immense commitment of resources, time, and budget to successfully complete such testing.

Typically, the structure of cell-level validation testing falls into seven general categories of testing:

1. *Beginning of Life inspection (BoL)*—Basic mechanical measurements, cell OCV, 1-kHz ACR, and thickness or volume
2. *Characterization group*—OCV, rate mapping/ HPPC, DCIR.
3. *Environmental durability*—Customer-specific corrosion, glycol immersion, or other customer-defined requirements.
4. *Calendar life*—Storage at multiple temperatures and multiple states of charge (SoC).
5. *Cycle life*—Various cycling at specified C-rates, depth of discharge limits (DoD), and temperatures. May include specific drive cycle profiles.
6. *Abuse group*—Overcharge, hot box, short circuit, drop, crush, nail penetration, GBT-31485.
7. *Compliance*—Regulatory testing per UN38.3.

Each of these testing categories is executed during an EV program's respective phase gates. This work then proceeds in a stair-step progression from the early phases (CV) to the later phases (DV and PV). Figure 3 conveys this sequencing. Note again that the genericized timeline covers nearly 3.5 years from the early CV phase through to cell start of production (SoP).

- When we think about the actionable data that feeds into the system-level design, one of the most important activities is to gather enough cell data to input into a life model. A general guideline to establish a reasonable confidence life model for storage and cycling is to have 6-9 months of testing data in hand. Many research and development efforts are underway to employ machine learning and AI techniques to establish more refined modeling with a shorter duration of testing. However, this work still requires harvesting large volumes of meta-data that may not be readily available in some customer programs, for example, working with new chemistries or designs. Even if such data is available, there may still be important challenges with data quality. Examples include:
- Cell-to-cell consistency at low pre-production volumes
- Small sample sizes (cell availability may be very limited in R&D phases)
- The quality of the testing execution itself

It is this last point regarding test quality that especially drives consideration in the use of a third-party test lab. While in-house testing holds many clear benefits (control of schedules and priorities, known equipment/personnel, and in-depth knowledge of product under test), an independent lab affords improved impartiality of results, additional test capacity, independent accreditations, and enhanced credibility with unbiased external testing reports.

APPROACHES FOR DATA MANAGEMENT

Keeping in mind the framework of the APQP process and the complexities of executing and compiling all those categories of data in Figure 3, a key best practice is to adopt a robust information management process. For EV cell testing, many multichannel test cyclers are connected to networked servers for data aggregation. The cyclers and channels are further configured with an array of chambers, incubators, and temperature-controlled rooms to maintain temperature stability during testing. Finally, a variety of other stand-alone equipment is used for periodic state-of-health (SoH) and reference performance tests (RPTs). With such large amounts of disparate data, proper data management strategy and execution are critical.

So how is this accomplished? All validation testing must have solid traceability for each individual cell serial number throughout all steps in test progression, from incoming inspection through long-term cycling or calendar aging. We have found that, where possible, the use of the complementary capabilities of an internal battery test database (BTD) and a high-resolution cloud-based battery intelligence platform (such as Voltaiq®) achieves this important goal. All cells are scanned and assigned to a single test ID code. All downstream data is linked to the test ID from that point onward. Report data can then be processed and filtered based on individual cell IDs or lots as desired. Enabling customer access to real-time data enhances communication on test status and provides a range of reporting options and advanced analytics.

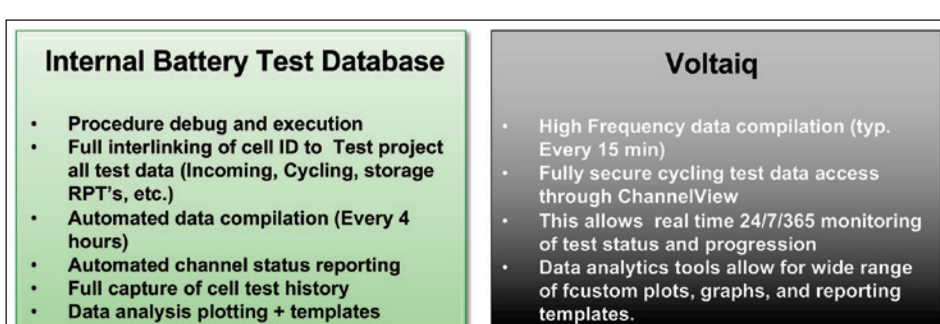


Figure 4: Database capabilities

The explosion in activity in the adoption of EV technologies has led to a huge demand for third-party laboratory cell performance test capacity. Given this, planning external test needs early and carefully is important. To that end, an internal BTD provides automatic daily updates on channel availability and status (including tracking of ganged channels for higher current cycling or those blocked due to specific chamber conditions). These reported states are key inputs for providing accurate scheduling, customer guidance during the quotation, and agility during the test planning process.

Why agility? Well, in a perfect world, an overall program goal per APQP is to achieve a stable design after CV and then move on to validate through DV. But problems will occur, including unexpected process excursions, material supply variability, and unforeseen interactions in the results. Testing agents must be responsive to changes in any given test plan to meet unforeseen customer issues or requests. Using appropriately designed and implemented data management systems allows such responsiveness, permitting the quick identification of possible solutions to issues that arise during the test process.

TEST PROCEDURE DEVELOPMENT

The cycling testers are at the center of most of the performance testing, including storage RPTs and the range of cyclic aging conditions. It is important to have staff trained and experienced with this equipment. Different models of cycler testers (Maccor, Bitrode, Chroma, Neware, etc.) have unique designs (especially system hardware capabilities) and resultant functional sensitivities. Some operational modes may be prone to causing interrupts, holds, and errors.

An example of this might be where relay switching between charge and discharge steps causes a lost current control failure, which can be mitigated by incorporating a short duration (~<1s) "phantom" 0A charge step. It is important that such sensitivities be fully understood and abated before embarking on a customer's testing. Such knowledge comes through proper training and experience. Failure to account for such testing equipment anomalies, particularly during long-term aging studies, can have cumulative confounding effects on the overall data quality.

It is important to work with the customer at the earliest stages of the project to identify whether the customer will supply build-test procedures or need to be written by the lab based on a general outline. If they must be lab generated, planning may need to include lead time to allow for a draft-review-revise iteration before final approval. Another consideration is that some procedures are more complex and may contain advanced constructs that limit the efficacy of offline procedure reviews. Experience shows that an initial debug run with a "proxy" cell can avoid significant test problems later due to undetected programming errors.

The bottom line is that it's best to adopt a "measure twice, cut once" philosophy. Be rigorous in procedure development, conduct de-bug testing before initiating the actual test protocol, and closely work with test equipment suppliers to identify equipment idiosyncrasies and develop appropriate mitigation strategies.

FIXTURING CONSIDERATIONS

Whether pouch or canned prismatic, cell performance testing must have clearly defined fixture requirements. Keep in mind that a main objective for cell-level testing is to approximate application-relevant conditions. Li-ion cells will age and generate internal pressure over their lifetime. Depending on the combination of environmental and cycling parameters, this rate of swelling and gas generation will vary.

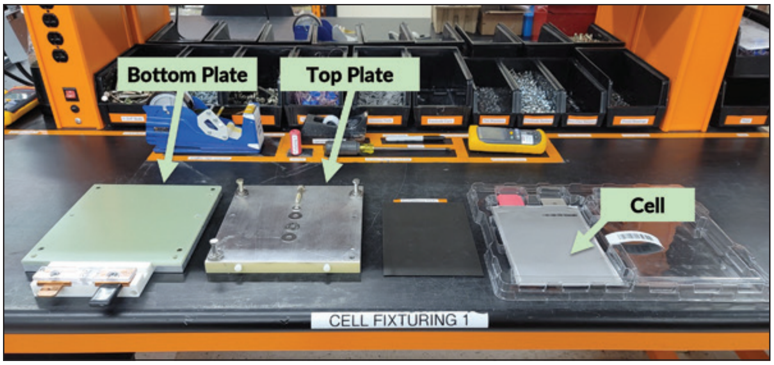


Figure 5: A typical large-format cell fixture

The standard practice for such testing is to use a compression fixture designed to apply controlled pressure to the cell. Typically, this assembly is composed of a 10mm thick aluminum top and bottom plate with bolts (see Figure 5). Ideally, this should be representative of the module or pack enclosure boundary conditions, including the use of identical compression pads or similar contact materials used in the pack assembly.

- *Testing agents can benefit from utilizing an inventory of fixtures* that cover a range of format sizes but should also have the internal capability or external vendor partnerships that support the rapid fabrication or modification of existing designs.
- *Define clear fixturing requirements ASAP* so that plans will factor in potential fixture lead times (i.e., target compression, cell spec sheet/size). For solid-state applications, load requirements can be much higher than standard Li-ion (75 psi vs. 8-14 psi). Confirming that the fixture assembly equipment can meet higher loading targets is important.
- *Fixture assembly equipment* must allow for a repeatable and reproducible load (very important as the cell may be re-fixtured multiple times as part of a test plan).

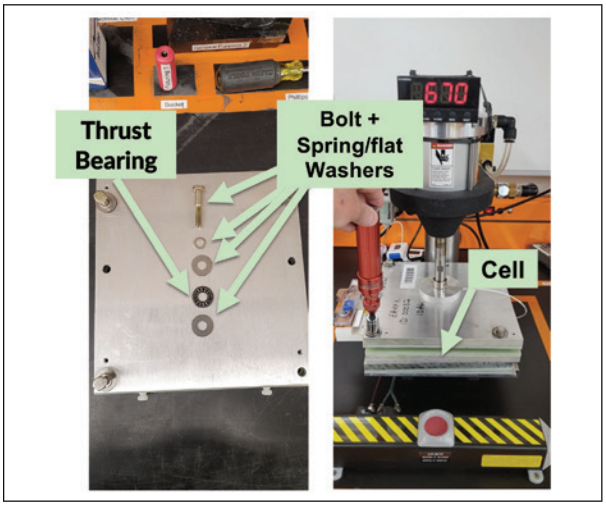


Figure 6: Fixture hardware and load cell equipment

As shown in Figure 6, it is highly recommended that a calibrated load cell and hydraulic or pneumatic piston at an appropriate rating be used. Sole reliance on bolt pattern tightening may not guarantee that intended loads are achieved. Even worse, it may induce unbalanced loading across the cell under test, resulting in potentially unattributable test variances.

Additional points:

- *Use of thrust washers* allows only normal compressive force between plates while eliminating distortion effects between the interface of the bolt and plate;
- *Ensure plates are clean* of debris and copper tabs are not oxidized before proceeding;

5-S Step	Definition
Sort	Eliminate whatever is not needed by separating needed tools, parts, and instructions from unneeded materials.
Set in order	Organize whatever remains by neatly arranging and identifying parts and tools for ease of use.
Shine	Clean the work area by conducting a cleanup campaign.
Standardize	Schedule regular cleaning and maintenance by conducting *seiri*, *seiton*, and *seiso* daily.
Sustain	Make 5S a way of life by forming the habit of always following the first four S's.

Figure 7: 5-S practices

- *Thermocouple routing* to minimize stress concentrations on cell surfaces;
- *Improve redundancy and traceability* by writing the request ID and cell ID on the top seal of the cell to enable easier verification that the correct cell is in the fixture;
- *Check and check again* to confirm that the fixture flat washers and thrust bearing are not loose after tightening.

GENERAL LAB 5-S PRACTICES

The 5-S is a standardized approach to facility organization and cleanliness. Proper implementation leads to the smoother operation of the laboratory. This effort should be complemented with a continuous improvement versus a "one and done" mindset. Experience has shown improved safety, higher equipment availability, and lower defect and error rates can result. 5-S also creates a positive feedback loop, creating an enhanced enterprise image to customers, suppliers, employees, and management.

Figure 8: General lab 5-S implementation at measurement stations

Figure 7 provides an overview of standardized 5-S practices. Figures 8 and 9 illustrate examples of 5-S in the general lab area and with equipment set-up practices. For example, lab benches have marked areas for needed tools and equipment, and standard environmental chamber 80-20 rack set-ups have clearly labeled cable connections, leads, and clean layouts throughout.

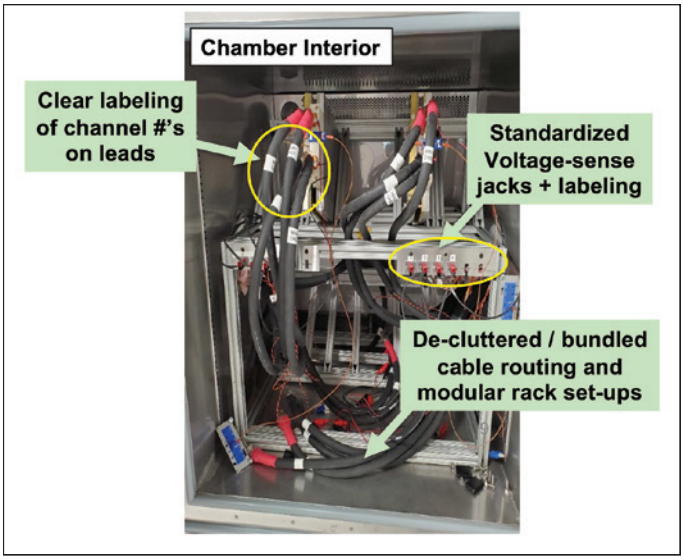


Figure 9: Test chamber interior showing 5-S compliance

THE 8-D PROCESS AND FAILURE ANALYSIS

By its nature, cell validation for EVs is intended to underpin expected performance and identify failure modes. Understanding such failure modes provides more value to the product's body of knowledge than just a series of passing tests. The 8-discipline or "8-D" process developed by Ford Motor Company provides a systematic method for analyzing failures. By carefully analyzing the failure modes, more can be learned about the intrinsic design margin and what the root cause may be. Then, appropriate mitigation steps can be taken with the cell design or with modification of certain operating conditions to reduce or even eliminate the chance of recurrence.

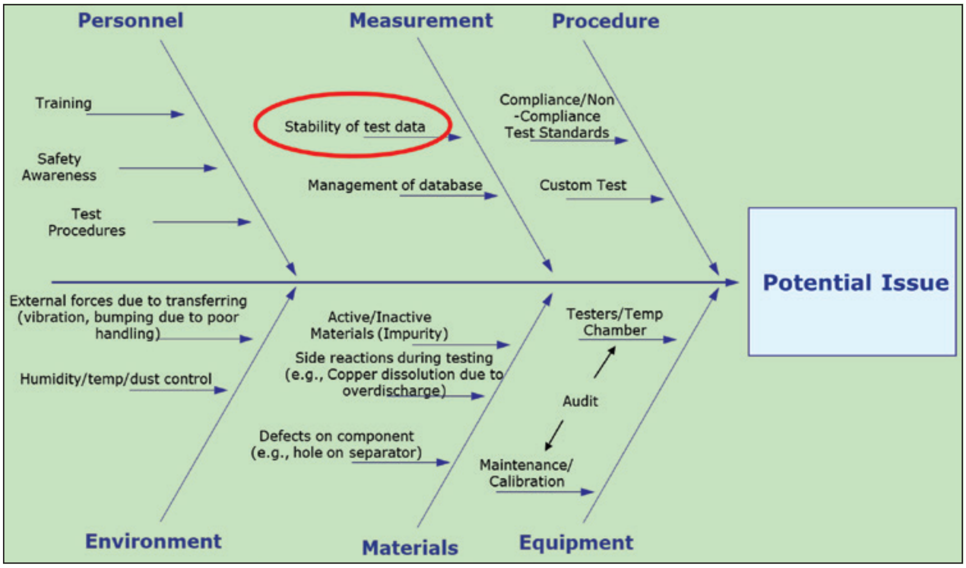


Figure 10: 8-D Fishbone diagram example

Several analysis tools can be used as a part of the 8-D process. The Ishikawa or fishbone diagram is one of the most commonly used structures to help organize data to arrive at a root cause (see Figure 10). Each of the main legs of the diagram documents the hierarchy of failures related to a certain category within the cell development space. Topline categories include personnel, measurement, procedure, environment, materials, and equipment.

Another important part of the root-cause investigation is cell-level failure analysis. Cell teardowns are a fundamental tool that allows for gathering empirical information on the state of a cell's packaging, internal electrode stack, and other components at critical points in the cell's life cycle or after failures. Cell teardowns are sometimes an integrated part of a cell's test plan, but not always.

There are generally two classes of teardowns:

- *Proactive*—In these cases, the customer may want to quantify warranty risks or understand and optimize cell performance; and
- *Retrospective*—Here, a failure has occurred, and a root cause analysis needs information on the condition of the cell and its components. Material samples may be collected for deeper forensic analysis.

UN 38.3 CONSIDERATIONS

Recall that the compliance testing requirements in the cell test plan must include a suite of tests for UN 38.3 transportation testing. This requirement is needed for any cells in development that fall outside of the R&D prototype classification waiver. Depending upon laboratory backlogs, this set of tests may require 1-3 months lead time to get the final certificate.

Particularly for a cell in development, suppliers should carefully review any changes to the design that could trigger the need for a UN38.3 retest. It is helpful to refer to the decision flowchart within the UN standard and the specific criteria described. It may be possible to apply a new part number with the change onto an existing transportation certificate for minor changes that do not meet the retest criteria. However, for international shipments (for example, China), customs inspection criteria can be murky. For this reason, it is critical to rigorously review the changes to clearly understand whether this constitutes a new design, thus triggering the need for retesting.

CUSTOM TESTS

Custom testing considerations can fall into a variety of validation testing types:

- *Abuse*—An abuse test is any test that subjects the product to non-normal stress. This can be electrical, thermal, mechanical, or chemical, to name a few. An example is custom nail penetration testing. Certain customers may specify unique penetrator details such as diameter or point dimensions, process parameters like nail speed or penetration depth, or environmental factors such as preconditioning or test temperatures. They may also seek supplemental data on response factors such as gas composition, gas volume, or pressure vs. time.
- *Drive cycle*—This refers to subjecting the cell to the specific charge and discharge profiles to

which it will be exposed in the supported vehicular environment. Custom environmental or mechanical conditions could further supplement this. Such testing requires careful alignment of test procedures to the intended service and environmental histograms.

- *Accelerated testing*—Most commonly, test acceleration is achieved through elevated temperature. In the case of electrical testing, this may be further supplemented with higher charge or discharge currents. Note that many other acceleration strategies can be employed to meet a given test situation.
- *Unique DOEs*—Designed experiments are used to investigate design or process concerns throughout the process. Early in the design cycle, custom experimentation might include characterization tests on new cell design features. Some examples include thermal mapping vs. high current pulse discharge, Env. Soak, or Li-plating studies).

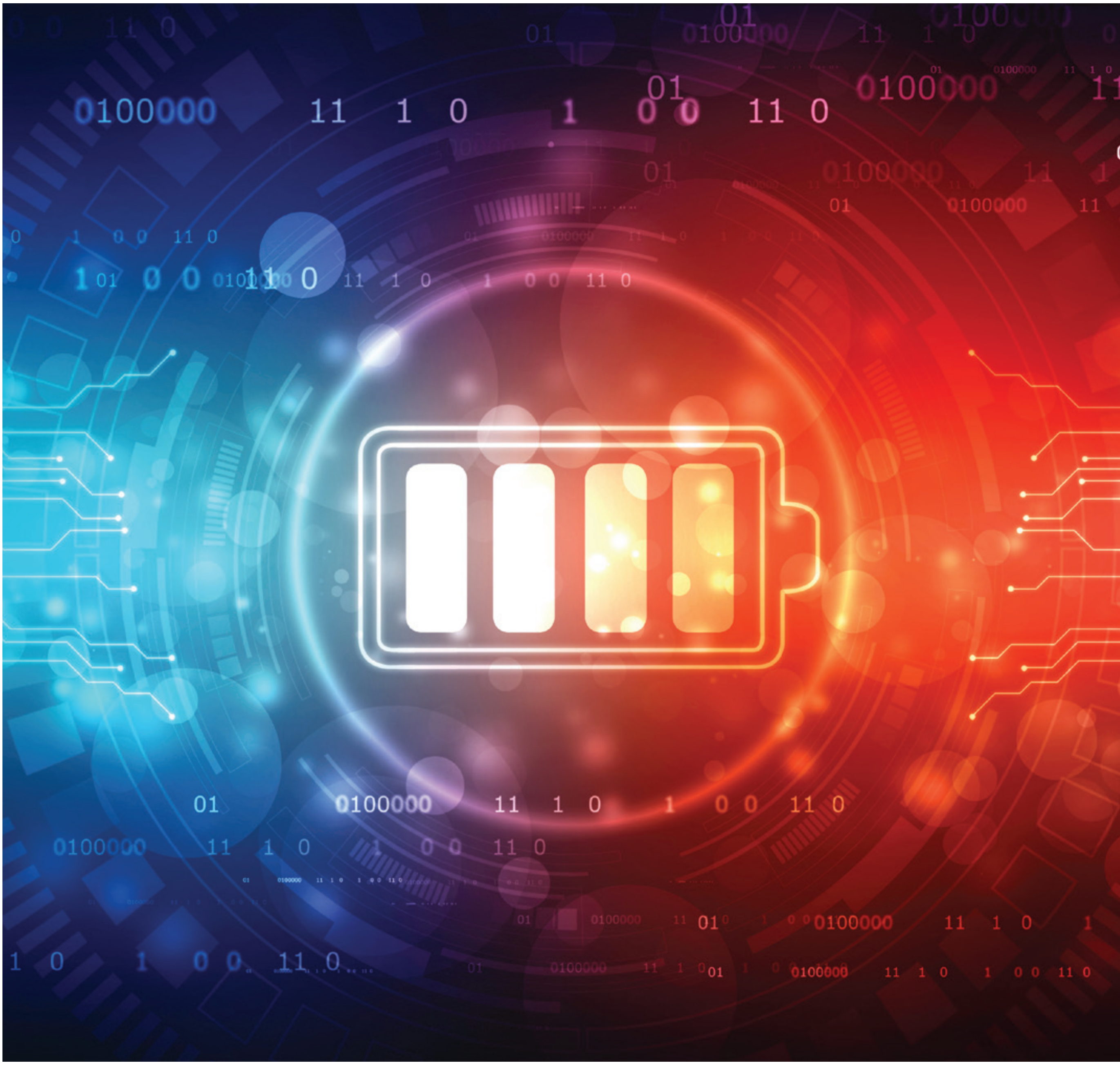
A general recommendation is to prioritize early detailed reviews between testing agents and customers on potential custom testing needs. This will help to ensure alignment regarding both capability and available capacity.

CONCLUSION

EV cell performance testing involves a large, multifaceted scope of planning, activities, and deliverables. A common and critical thread is rigorous and transparent communication with the customer from the earliest point in the quotation and kick-off through key milestones and final reporting. Applying lessons learned with procedure development, fixturing, failure analysis, and information management can help ensure that consistent and high-quality testing is executed. Ultimately, it is about delivering high-confidence results that can be used as actionable data to help the customer make the best decisions on a program.

EMC MANAGEMENT IN CHARGING APPLICATIONS

Managing the EMC Process So You Can Pass the First Time



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By Dr. Min Zhang

INTERPRETING EMC STANDARDS

Picture yourself as part of a team of engineers who are specialized in designing chargers. A new project comes along. How do you ensure the final design will pass the standard EMC tests the first time?

A typical first step is to interpret the relevant EMC standards that are applicable to the specific application. (Quality, safety, and environmental standards are equally if not more important, but they are not in the scope of this discussion.) One must look at the commercial EMC standards if the product is a fast charger for mobile phones and laptops. The automotive EMC standards should be applied if the product is an on-board charger (OBC) used in an electric vehicle. If it is a product based on wireless power transfer (WPT), one should refer to relevant standards and stay alert to changes as the standards are still being developed.

As an example, Table 1 lists the typical EMC test requirements that are applicable to an OBC.

Test Items	Standard
Radiated emission – Broadband sources	ECE R10.6 Chapter 7.10 & Annex 7
Radiofrequency disturbance voltages on AC or DC power lines	ECE R10.6 Chapter 7.13 & Annex 19, average and quasi-peak detector IEC 61000-6-3
Radiated immunity	ECE R10.6 Chapter 7.18 & Annex 9
Transient disturbances conducted along 12V/24V supply lines	ECE R10.6 Chapter 7.19 & Annex 10
Fast transients – burst conducted along AC and DC power lines	ECE R10.6 Chapter 7.15 & Annex 21
Surge conducted along AC and DC power lines	ECE R10.6 Chapter 7.16 & Annex 22
Immunity to low frequency conducted disturbances – voltage dips and interruptions on AC supply lines	IEC 61000-4-11 <16A per phase IEC 61000-4-34 >16A per phase
Immunity to electrostatic discharger	ISO 10605

Table 1: Standards and regulations applicable to on-board charging systems

AN OVERVIEW OF THE EMC DESIGN PROCESS

Once the requirements have been agreed upon by the design company and their customer, the design process follows. This design process typically follows a staged approach, as shown in Figure 1. It is highly

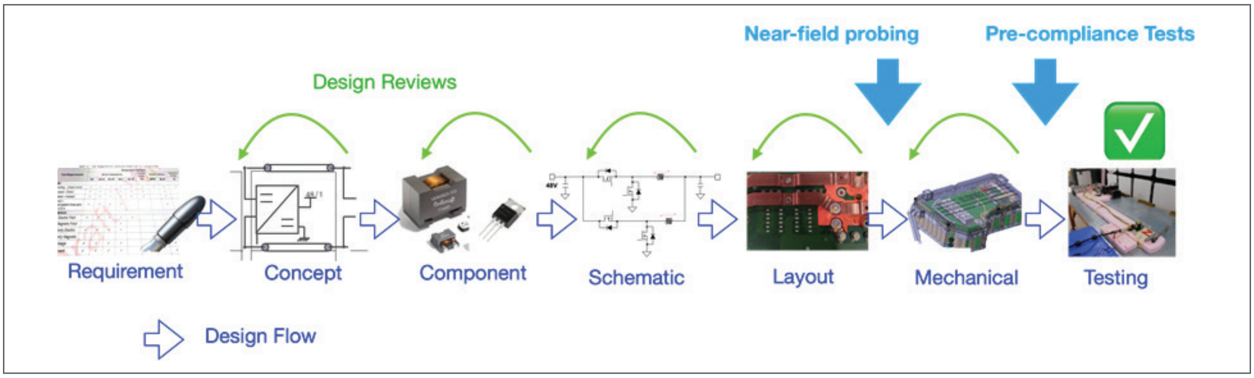

Figure 1: A typical design process showing design stages

At the concept stage, engineers evaluate and select the topology of a charging converter based on the product requirements. It is essential to review the design with EMC in mind.

recommended that the EMC design reviews should be performed at each stage of a product's design and preliminary tests should be arranged as soon as the prototype of the PCB is ready. It is perhaps the only way to ensure strict EMC control to avoid major design changes at a later design stage.

In this article, we discuss how to implement EMC management during the design and development stage using practical demonstrations.

THE CONCEPT STAGE

At the concept stage, engineers evaluate and select the topology of a charging converter based on the product requirements. It is essential to review the design with EMC in mind. A popular power converter topology for charging applications is a power factor correction (PFC) stage followed by a resonant circuit. Common PFC circuits include interleaved boost converters, bridgeless totem-pole converters, and interleaved totem-pole converters. Popular resonant circuits are an LLC, a phase-shifted full-bridge converter with current doubler rectifier, and so on. Figure 2 illustrates the converter topology of a 12 kW OBC (for demonstration purposes, only rail 1 of the converter is shown).

It is essential to have a PFC stage to improve the power factor of the grid and to achieve lower total

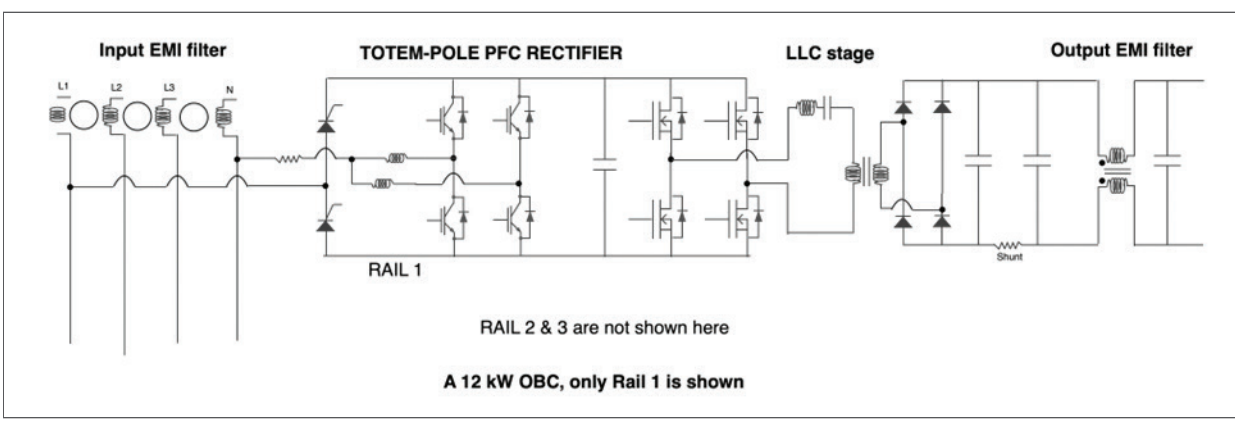

Figure 2: Schematics of a 12 kW on board charger (rails 2 and 3 are not shown in this diagram)

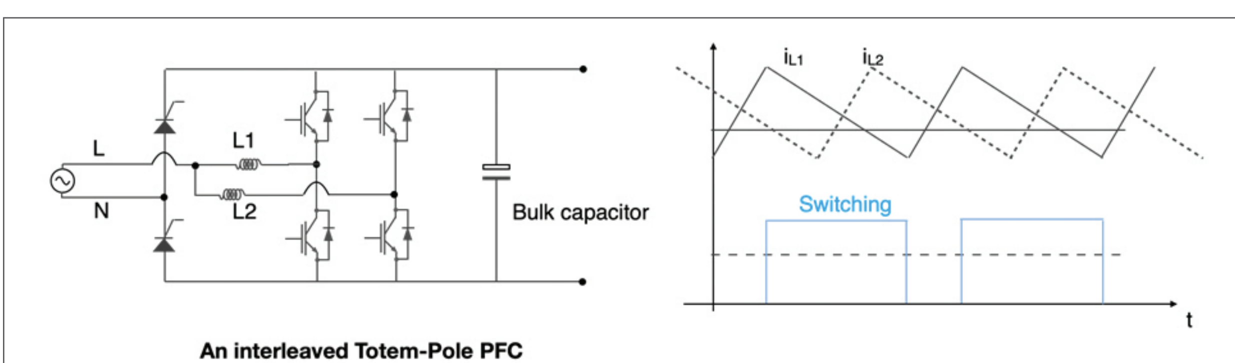

Figure 3: One of the benefits of using an interleaved totem-pole topology is ripple current cancellation

harmonics distortion (THD) during the charging state. Without the PFC, charging, especially fast charging, draws a high peak current at the voltage peak and almost no current over the remaining mains cycle. This results in excessive high current flow in the mains conductors, the power transmission lines, and the power transformers.

In the example shown in Figure 3, an interleaved boost totem-pole PFC is selected because the two interleaved rails topology achieves halved current rating per half bridge. This results in ripple current cancellation on both the input and output of the PFC stage. As a result, this reduces the size of the bulk capacitor and lowers the EMC impact of the PFC. But this approach increases the number of switching devices and the complexity of the control. (Reference 1 offers a detailed comparison study between different PFC topologies but does not focus on the EMC performance analysis.)

It is the design engineer's job to select the PFC topology based on the intended application. The decision needs to be based on the trade-offs between efficiency, ease of manufacturing, cost, weight, thermal considerations, and EMC. The topology also depends on the power rating of the applications. For instance, if it is a fast-charging device for a laptop or mobile phone, the PFC topology will be a simple boost PFC without interleaving. A number of trade-offs can also be seen when it comes to selecting the resonant converter stage. It should be noted that the zero-voltage switching (ZVS) has been widely used for resonant converters. When designed properly, ZVS provides significant circuit improvements in zero voltage switching and other areas, such as reducing common mode currents.

THE COMPONENT SELECTION STAGE

Reference 2 discusses the importance of selecting the right types of power electronics devices. For charging applications, choosing the right devices is essential to achieve a compact design and comply with EMC requirements. Among the devices of choice, wide bandgap devices such as gallium nitride (GaN) devices are widely seen in commercial applications such as fast chargers for laptops and phones, while silicon carbide (SiC) devices are dominant in the high voltage high power applications such as OBCs used in electric vehicles.

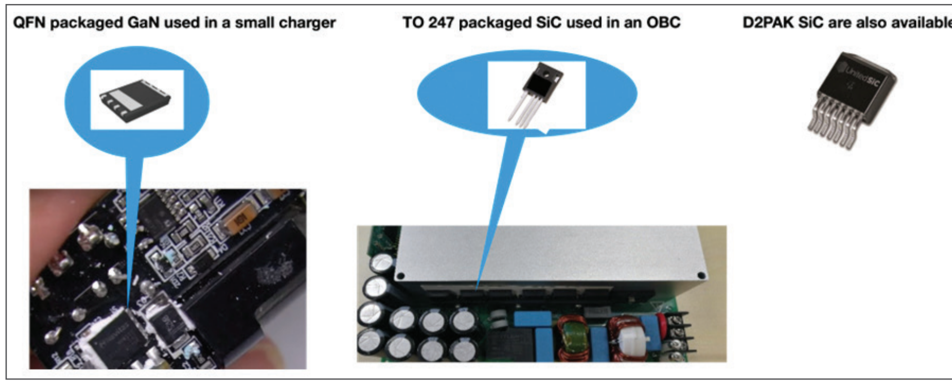

Figure 4: Wide band gap devices such as GaN and SiC FETs are widely seen in charging applications

As shown in Figure 4, most GaN devices are surface-mounted with integrated driver circuits, while most SiCs are through-hole discrete devices because of the high-power level. Though D2PAK SiC devices are available, they are not a design engineer's favorite choice, mainly because of the different thermal characteristics associated with the package.

Through-hole devices are robust, low cost, and enjoy better thermal characteristics, and are therefore widely used in high voltage, high power applications. But, for EMC, they are not as good as the surface-mounted devices because the extra-long leads of the package introduce larger inductance.[2] Being physically tall, they also radiate more efficiently compared with surface-mounted devices. The thermal design around these devices is crucial as heatsinks are often much larger than the devices themselves. If the heatsink is not grounded well, it can radiate much more at a lower frequency range (30-300MHz).[3]

Apart from switching devices, magnetics components such as the transformer used in the resonant converter stage also need to be designed with EMC considerations in mind. System efficiency is always the most important design factor. Therefore, a transformer's losses (including core losses, copper losses, skin effect, and proximity effect) are often given significant consideration during the design stage. The ZVS scheme also requires a saturable core of the transformer and prefers higher leakage inductance. This means that the EMC design of a transformer is often overlooked.

A simple electrostatic shield can often help reduce the common mode current when added to the transformer.[4] The shield needs to be connected to 0V on the primary side and should be kept as thin as possible to minimize eddy current loss due to the proximity effect. A second shield on the secondary side improves the EMC performance further, but at extra manufacturing cost.

Other techniques in the transformer design include common mode current cancellation or the so-called common mode current balance based on a unique winding structure design.[5] It should be noted that transformer design is also the key to optimizing the ZVS of the converter.

During the design review, pros and cons of each component selection should be assessed. Efficiency, size, and cost are often the key factors in selecting components. But the comparison should also account for EMC considerations as well. For example, engineers often select components so that the best form factor and minimum cost are achieved, only to find out that a heavy, bulky, and expensive filter needs to be added on at a later stage because the selected switches/transformer create too many EMI issues. If the issue had been highlighted early during the component selection stage, total time and cost could have been reduced.

THE SCHEMATIC AND LAYOUT REVIEW STAGE

During the schematic review, attention should be paid to the following areas:

1. The gate driver design should be reviewed, switching speed (rise time and fall time) of the switching devices should be analyzed based on the gate resistors, and risk analysis should be performed. The review should also extend to the bootstrap circuit for non-isolated gate drivers and snubber circuit design.
2. Input and output filters are key to the EMC performance of a charger. The insertion loss of each filter stage should be calculated/simulated. The filters should be most effective in the frequency range between a few kHz to 100s of MHz.

3. Decoupling capacitors are essential for all switched mode power supply designs. Design engineers should check if sufficient decoupling capacitors are placed in the key areas of interest. These key areas are power lines (primary and secondary sides), transformers (between primary and secondary), and connections to the chassis.

When it comes to the layout review, the devil is in the details. A layout review can easily cost a few days' time with design engineers from multiple disciplines involved. Decoupling capacitors, filter locations, connectors, traces, vias, and more all need scrutiny in the review stage.

One example is shown in Figure 5. In order to dissipate the heat generated by the GaN devices, a large copper area and thermal vias are often used. This is a design feature generally favored by both electronic

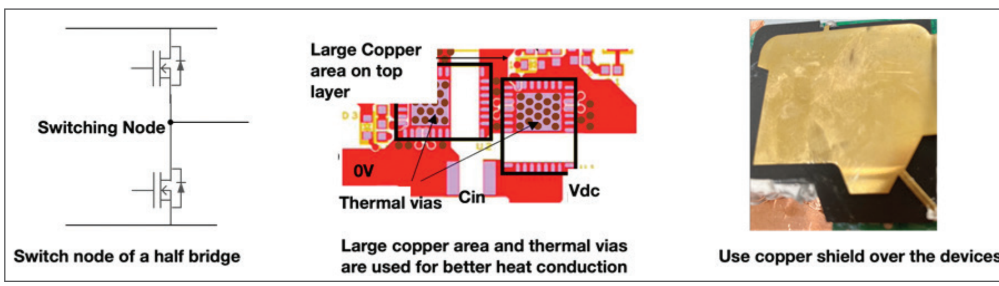

Figure 5: Using a large copper area under the switch node could lead to worse EMI, a shield over the devices is beneficial for both thermal and EMC

engineers and thermal engineers as large copper areas dissipate heat more efficiently, thereby achieving a higher efficiency conversion. The switching node of a half bridge connects the source node of one device and the drain node of the other. But having a large copper area effectively increases the size of the switching node, making the emission worse and hard to contain. This EMC-related risk should be highlighted in the layout design stage and a mitigation plan should be designed. In this case, a possible mitigation plan would be to use an aluminum/copper sheet over the devices. This sheet helps dissipate the heat while also providing shielding over the switching node. This contingency plan can then be implemented and tested in the packaging and mechanical stage.

TESTING AT AN EARLY STAGE

A preliminary test should be performed as soon as the first prototype PCB is ready. It is true that a product's EMC performance is dependent on the layout and packaging, and the noise profile of a final product will be different from that of a single PCB. However, an early-stage, near-field probing exercise can often indicate red flags and will reap benefits at the tail end of the design process.

On the PCB level, two simple benchtop tests can be performed. Near field probing, such as using a magnetic field loop over the PCB area, can locate the noise source (see Figure 6). The noise profile is generally a good indication of both conducted and radiated emissions.[6] As shown in Figure 7, measuring the common mode current on the cables using an RF current monitoring probe is another efficient way of predicting conducted and radiated emissions of the PCB under investigation.[7]

PACKAGING AND MECHANICAL ASSEMBLY STAGE

The packaging of the final product is often considered to be a mechanical job. At this stage, the final product is assembled, and the thermal design is applied. PCB assemblies could involve stacking up PCBs, stacking PCBs on stand-offs to chassis, wire-connecting PCBs, PCB connections to chassis connectors, etc. On the thermal design, for small power applications, this means applying thermal paste/glue, and thermal pads.

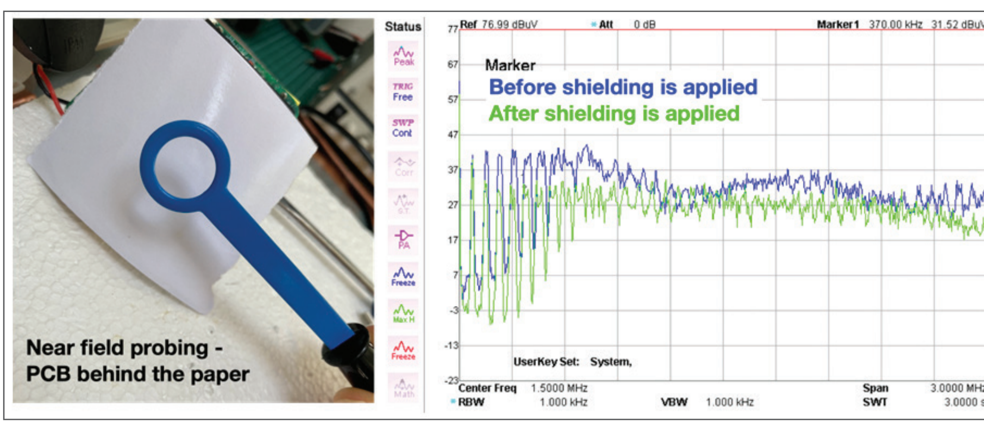

Figure 6: Using near field magnetic probe serves as a quick way of testing the EMC performance of the PCB

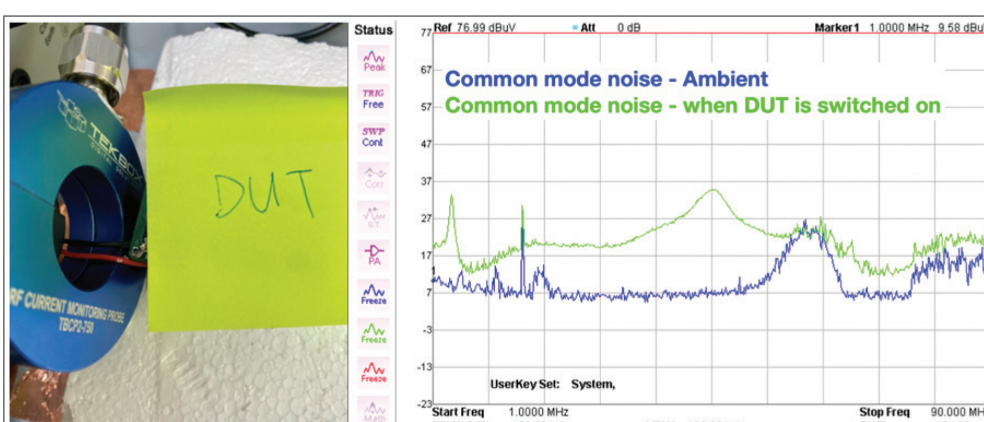

Figure 7: Using an RF current monitoring probe to measure the common mode current on the cables of the PCB

For large power applications, this means implementing heatsinks and liquid cooling pipes.

The key challenges at this stage are to minimize connection impedance. For instance, the height of the stand-offs determines the inductance between PCBs to chassis. Therefore, multiple shorter stand-offs are preferable from the EMC point of view, a preference typically endorsed by mechanical engineers as well[2]. However, with stacked-up PCBs, cavity resonances could occur, and ways of de-risking resonance structures can be found in References 8 and 9.

Heatsinks need to be bonded to either 0V or power rails to prevent them from radiating emissions. Shields such as the aluminum/copper shield introduced previously also need to be bonded to the 0V plane to make them work for EMC.[3] (For thermal design, they don't need to be bonded to any point.)

PRE-COMPLIANCE EMC TESTING

The two most important EMC tests for charging applications are for conducted and radiated emissions. It is always a good practice to test the products in a pre-compliance EMC test set-up before sending the unit for formal compliance testing. The good news is that both conducted and radiated emission pre-compliance tests can be performed on a benchtop at a relatively low cost.

CONDUCTED EMISSION

Depending on the power rating of the DUT, suitable power rated LISNs can be used for conducted emission testing. Because it is a high voltage application, high voltage safety should take priority when setting up a pre-compliance test set-up. Using an isolation transformer and grounding the test ground plane to safety earth are absolutely necessary to secure the safe operation of conducted emission test. Figure 8 shows a benchtop pre-compliance conducted emission set-up for a product in development using GaN switches.

RADIATED EMISSIONS

An open transverse electromagnetic (TEM) cell is often used to determine radiated patterns of a DUT. It should be noted that a TEM cell set-up will not deliver exactly the same quantitative results as a measurement using far-field antennas. Due to space constraints, longer wires are often wound within the TEM cell space, which also affects the radiated emission profile. Nonetheless, using a TEM cell has proved to be an effective way of predicting the radiated emissions of a DUT.

As shown in Figure 9, an OBC is placed inside the TEM cell. To draw a complete emission profile of the DUT, three main orthogonal orientations of the DUT need to be placed.[10] But this also illustrates the limitations of using a TEM cell for testing large power-rated products such as on OBC due to the spectrum height of a TEM cell (in this case, this TEM cell has 15 cm spectrum height). Therefore, in this case, only one orientation of the DUT is tested. However, for home appliance charging applications, a DUT is small enough to be tested with the three main orthogonal orientations.

Hopefully, at this stage, the pre-compliance results provide a high level of confidence that the device will pass the emission tests. However, if red flags are highlighted, engineers can walk back to the previous stage to work out a troubleshooting plan that will eventually address the highlighted issues.

SENDING THE PRODUCT FOR FORMAL EMC TESTING

There is always some degree of uncertainty when it comes to final EMC testing. But, by following the EMC management process described in this article, there should not be any big surprises. The process helps to ensure that all foreseeable EMC aspects have been considered and addressed during the design process. The meeting notes of each design review should be well-documented in an EMC risk assessment. The EMC risk assessment serves as convincing evidence that the company has at least attempted to address EMC issues.

Figure 8: A fast charger is being tested against conducted emission in a pre-compliance test set-up

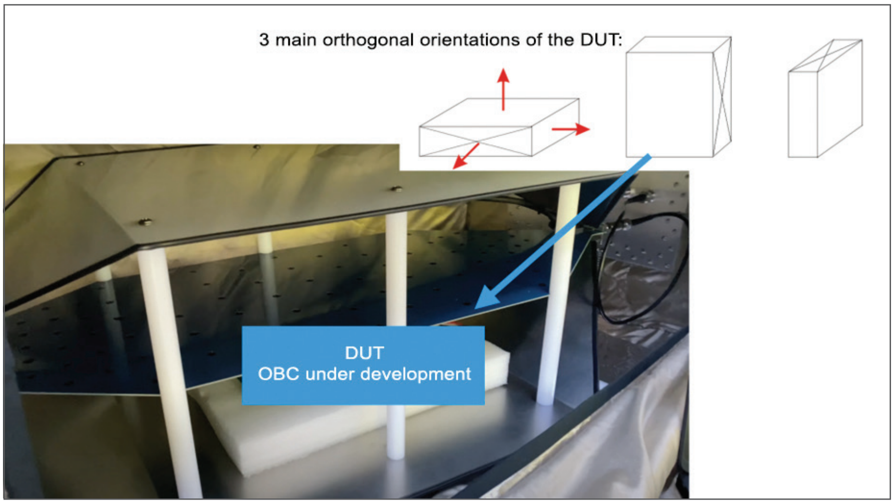

Figure 9: An OBC for automotive application is being tested against radiated emission in a TEM cell

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ESD COMPLIANCE IN A SERVER ROOM

How To Select ESD Flooring for a Space with No Set Industry Standards

Dave Long is the CEO and founder of Staticworx, Inc., a leading provider of flooring solutions for static-free environments. He has 30-plus years of industry experience and combines his comprehensive technical knowledge of electrostatics and concrete substrate testing with a practical understanding of how materials perform in real-world environments. Long can be reached at dave@staticworx.com.

By David Long

Static-control flooring provides protection against electrostatic discharge (ESD) in multiple industries servicing disparate applications that range from eliminating annoying shocks to protecting aircraft flight-tower operations from equipment malfunctions. Often referred to by the term ESD flooring, this category of flooring can protect static-sensitive electronic devices and equipment from harmful (but, due to its invisibility, seemingly inconsequential) levels of static discharge, far below the threshold of human sensitivity. In other instances, ESD flooring is installed to prevent static sparks from causing ignition of flammable chemicals, munitions, explosives, and energetic materials.

In their article "Are Data Centers Drying Up,"[1] authors Beaty and Quirk discuss alternatives to humidification, like ESD flooring, for preventing real-life ESD problems in data centers, such as:

- Self-correcting errors (such as a lost package in LAN traffic);
- An upset that may need user intervention; or
- Actual physical damage to IT equipment

Specified and used properly, ESD flooring prevents the generation of static electricity and provides a path to ground for charged objects, including people, materials, machines, and transport equipment. ESD flooring also grounds any object with intrinsic conductivity that makes contact with the floor. For data centers, multiple ASHRAE-funded studies strongly suggest the use of at least moderately conductive flooring systems in controlled areas to reduce the overall level of electrostatic charge accumulation, regardless of environmental moisture or the type of footwear used in the space.

STANDARDS VARY BY INDUSTRY

Depending on the industry and application, different static-control requirements and test methods take precedent. For example, static-control requirements for handling explosives usually fall under the jurisdiction of either the Department of Defense (DoD) contractor manual, DOD 4145.26, or Department of Energy (DoE) Standard, DOE 1212-2019. In contrast, organizations handling static-sensitive electronic devices follow the guidelines of ESD Association standard ANSI/ESD S20.20.

It's critical to match the right standard and static mitigation strategy to your specific application. When comparing the value, jurisdiction, and viability of any organization and standards, it's worth noting the possibility of legal complications should the wrong floor be installed. In a January 2012 article published by *In Compliance Magazine*, nationally recognized liability attorney Kenneth Ross says that in a lawsuit:

> *"…Industry standards and even certifications like UL are considered minimum…the standard establishes a reasonable alternative design, and the manufacturer has to justify why it didn't comply."*[2]

Although this advice applies specifically to safety risks, it presents a second problem on a much wider scale. What about product performance? Static discharge is a very real problem, but it is mostly an invisible problem. How does the end user know they actually installed a compliant solution? Does the end-user organization rely on supplier literature and specifications, or does the organization do its own testing? What are the metrics for establishing product compliance, and does their space resemble the conditions under which the product was designed to operate? ESD footwear, for example, greatly enhances the performance of ESD flooring but may be impractical for spaces such as call centers and server rooms.

Given that standards vary, how do you determine which standards and test methods should be referenced for which environment? To understand why this is important, consider the different requirements for resistance testing between UL 779, DoE/DoD, and the ANSI/ESD test requirements. DoE and DoD resistance testing of conductive flooring is usually performed with an ohm meter set at 500 volts. The ANSI/ESD and ASTM requirement for the same resistance test specifies applying either 10 volts or 100 volts, depending on the resistive properties of the material under test.

Flooring manufacturers do not typically provide product specifications based on 500-volt resistance testing, and most flooring specifiers don't ask for results obtained at different voltages. Why would using different voltages in a resistance test present a problem? In the case of the DoD, the government set a minimum flooring resistance of 40,000 ohms tested at 500 volts to assess "safety" from electrocution. According to Ohm's Law, increasing applied voltage lowers resistance. A floor that measures 40,000 ohms using test method ANSI/ESD STM 7.1 at 10 volts will measure well below the 40,000-ohm requirement when subject to 500 V applied voltage.

Figure 1: Deteriorating floor in cable company server room

ASTM and ANSI both evaluate the resistance of conductive floors at 10 and 100 volts. If a specifier chooses a conductive floor based on test results obtained using ASTM F150 or ANSI/ESD STM 7.1 test methods, the floor may not meet DoD (500 volts) requirements.

What happens if resistance testing isn't performed until after the floor has been installed? This occurred at a U.S. Air Force base earlier this year. The facility handles explosives, and the floor, tested post-installation, was not in compliance with government requirements. The supplier has spent over $100,000 in labor and materials to remove their ESD floor and install a new floor that complies with the government standard. Either floor would have eliminated static satisfactorily, but the Department of Defense doesn't provide waivers for non-compliant materials used in explosives applications.

A CASE HISTORY

A large cable television provider enlisted a local flooring contractor to provide costs for a complex project involving the removal of old flooring in a large operational data center/server room and replacement with a static-control solution—the project presented many challenges.

The bond between the old floor tiles and the concrete (see Figure 1) had deteriorated due to age and adhesive breakdown. Flooring directly under racks could not be removed because the facility operates 24/7. Removing the floor surrounding the racks was risky due to potential problems with dust containment. These obstacles and preexisting conditions steered the cable company towards solutions that could be installed directly over the existing floor.

Several different ESD flooring materials were evaluated. The primary objective was to find a material that could be installed without adhesives. This limited the options to interlocking tiles or a floating solution such as rubber, vinyl, or ESD carpet tile. The carpet option was dismissed due to the need to move heavy equipment without adding rolling resistance. This led directly to the decision to install a hard-surface interlocking floor.

The next question: did they want dissipative or conductive flooring? To ESD program managers in electronics manufacturing facilities, this may seem like a simple choice, but this application required grounding people who were handling and changing circuit boards in an operational environment. The client wanted to know how high the resistance could be before it was too high to effectively decay charges and what resistance might be considered too low or unnecessarily conductive, thus posing a potential safety risk. The floor also needed to inhibit charge generation on a person wearing regular footwear in an environment with varying humidity.

Per ANSI/ESD STM 7.1, conductive flooring is defined as any flooring with a resistance to a groundable point of less than one million ($< 1.0 \times 10^6$) ohms. A dissipative floor measures from one million ohms to less than one billion ohms ($< 1.0 \times 10^9$). This test's ANSI/ESD S20.20 qualification phase is typically performed in a lab at low relative humidity (RH). An ohm meter is used to measure the aggregate resistance of all the components required to install the floor. With glue-down floor tiles, this entails installing tiles to a test substrate with the proper adhesive and then measuring the resistance from the tile's surface to a ground connection buried into or under the adhesive. The measurements obtained from this simple lab test determine whether a floor is categorized as conductive or dissipative.

To attain a compliant resistance, floors with conductive surfaces are sometimes installed with dissipative adhesive. As long as the adhesive assures a path to ground above 1.0×10^6 and less than 1.0×10^9, this type of flooring system would be characterized as a static-dissipative flooring system. Lab testing cannot predict whether or not this may be problematic in the field because labs don't present variables found in the intended installation environment. For example, a dissipative flooring system that relies on dissipative adhesive to control its resistance to ground could be rendered conductive if installation conditions introduce concrete moisture vapor transmission or if grounded equipment placed on the flooring surface creates an unintended ground path.

Depending on the construction of the flooring system, certain types of floors could also measure differently in the field than in the qualification test. A composite floor such as carpet tile or a floating vinyl floor, for example, might be manufactured with a more conductive surface layer than the layers below the surface. Performing tests on a mock-up installation can catch such possible pitfalls ahead of time, preventing surprises after the floor has been installed.

FOLLOWING A STANDARD

In the case of data centers and server rooms, there are no official standards for choosing the right electrical resistance for ESD flooring. But we can look for static-control guidance from manufacturers who build this equipment. Most use some type of ESD flooring. Since their ESD-prevention programs are designed to meet ANSI/ESD S20.20, they install flooring with a resistance measurement below 1.0×10^9 ohms to ground and charge generation (per test method ANSI/ESD STM 97.2 lower than 100 volts on personnel wearing ESD footwear.

Given that S20.20, IEC 61340-5-1 (the international equivalent of S20.20), and FAA standards all set an upper limit of $< 1.0 \times 10^9$, the point at which the performance of static-control flooring is significantly diminished, it's logical that this would be a universally accepted upper threshold.

It's paramount to keep in mind that resistance measurements made with an ohm meter should never be relied upon to determine how much current will pass through a static-control floor.

HOW CONDUCTIVE IS TOO CONDUCTIVE?

For decades, NFPA publications set a minimum electrical resistance of 25,000 ohms for floors installed in operating rooms. This resistance value was determined using an ohm meter set at 500 volts. UL 779 requires an average minimum resistance of 25,000 ohms. DoD 4145.26 sets 40,000 ohms as the minimum in areas with 110-volt service and 75,000 ohms near 220-volt service. (For DoD, a ground fault interrupter meets the same requirement.) A post on an IBM data center website, updated in May 2022, says:

> *"For safety, the floor covering and flooring system should provide a resistance of no less than 150 kilohms when measured between any two points on the floor space 1 m (3 ft) apart."*[3]

FAA 019f, Motorola R56, and ATIS 0600321 all require ESD flooring to measure above 1.0 x 10^6. Like the company in the case study that needed to protect grounded personnel, people employed by facilities covered by these standards work near electrified equipment. These industries created their standards with the intention of protecting workers from the risk of electrocution. While we don't know of a case where someone was electrocuted by an ESD floor, it's a theoretical possibility that has been upheld in laboratory testing.

SPECIFYING HIGHER ELECTRICAL RESISTANCE IS NOT A SAFETY MEASURE

It's paramount to keep in mind that resistance measurements made with an ohm meter should never be relied upon to determine how much current will pass through a static-control floor. One study in particular, by Fowler Associates in Simpsonville, SC, demonstrated a significant variance in the actual measured electrical current on ESD flooring materials versus the predicted electrical current based on resistance measurements obtained using an ohm meter.[4] The only flooring products marketed to protect workers from electrical current are highly insulative and serve no static-control purpose. ESD flooring is not designed to prevent the flow of electricity. It is exactly the opposite. ESD flooring facilitates the flow of charges to ground.

This leaves us with requisite policies such as following national and local electrical codes, limiting electrical work to only qualified personnel and organizations along with developing, implementing, and enforcing an electrical safety program. This isn't to say that we shouldn't consider a minimum resistance. It just means that we shouldn't rely on electrical resistance as a safety measure. But whether resistance is a reliable predictor of leakage current or not, flooring manufacturers should take Ken Ross's advice into consideration, i.e., a standard (UL, NFPA, DOD, FAA) establishes a reasonable alternative design, and in the case of an accident, the "manufacturer would have to justify why it didn't comply."

REMEMBER FOOTWEAR

Server rooms differ from electronics manufacturing spaces, and the criteria for selection differ as well. One significant question when selecting an ESD floor for a server room as opposed to a manufacturing environment is whether or not the floor can mitigate static charges without ESD footwear. In electronics facilities, all personnel on the floor are required to wear some type of ESD footwear. The use of ESD footwear would be impractical in a server room. This limitation creates a strong need for installing a floor that generates minimal charges regardless of footwear or low relative humidity.

According to a major ASHRAE-funded study:

> *"While it may prove impossible to control with certainty the footwear worn by personnel who enter or work in data centers, facility owners and managers should be aware that footwear can lead to issues in the daily operation of the data center. Just about any conventional polymer-based sole material may lead to high charge levels, some more than others – regardless of humidity. A conductive floor will help mitigate electrostatic charging even on shoes with the highest potential for generating static."*[5]

The type of static-control flooring material also plays a part in charge generation. Among the most compelling documented statistics is the probability of generating a charge over 500 volts while walking on a static-control floor wearing ordinary shoes (see Table 1). The probability of 500 volts occurring on a static dissipative vinyl floor was calculated at 35%; for a conductive vinyl floor, the probability dropped to 8%. The probability of a conductive rubber floor allowing a charge over 500 volts was only .1%.

ESD FLOORING: A PRACTICAL, MONEY-SAVING CHOICE

Historically data centers have relied upon humidification to control static. The ESD Association removed humidification as a requirement in the 2007 version of ANSI/ESD 2020. We can and should draw from other standards to address the specific needs of these spaces.

ASHRAE research project RP-1499 shows that the installation of static control flooring in data centers and server rooms can control, reduce and prevent problematic levels of static generation and, as a result, enable a significant reduction of long-standing humidification and energy requirements in these spaces.

Combatting these problems with a one-and-done infrastructure solution like ESD flooring makes sense, particularly compared with wasting energy to cool a highly humidified space. In "The Effect of Humidity on Static Electricity Induced Reliability Issues of ICT Equipment in Data Centers" (Endnote #5), authors Wan, Swenson, Hillstrom, Pomerenke, and Stayer strongly suggest the use of:

> *"at least moderately conductive flooring systems in controlled areas to reduce the overall level of electrostatic charge accumulation, regardless of footwear or environmental moisture. Flooring has to be installed anyway, and the cost associated with a conductive rather than insulative floor is minor compared to continuing operational costs to sustain proper moisture levels (low humidity)."*

When evaluating an ESD floor, multiple performance factors should be investigated, including maximum and minimum electrical resistance, electrical codes and industry standards, charge generation at the lowest operational relative humidity, and performance with and without ESD footwear. Whether the data center is under construction or already in operation will impact and possibly limit ESD flooring options.

Table 1: Summary data in probability for voltages greater than a threshold value (based on fitted lines).

Type of Data Center	500 volt discharge probability		4,000 volt discharge probability		8,000 volt discharge probability	
	15% RH & 59° F	50% RH & 80° F	15% RH & 59° F	50% RH & 80° F	15% RH & 59° F	50% RH & 80° F
No Static Control	18%	0.2%	0.5%	3.7×10^{-6}%	0.1%	3.2×10^{-8}%
Dissipative Floors, Dissipative Footwear	16%	19%	0.016%	1.0×10^{-4}%	5.5×10^{-5}%	2.2×10^{-7}%
Dissipative Floors, Uncontrolled Footwear	34%	44%	0.9%	0.001%	0.09%	2.3×10^{-5}%
Conductive Floors, Dissipative Footwear	0.003%	1.6×10^{-7}%	1.8×10^{-7}%	1.8×10^{-11}%	7.4×10^{-9}%	8.9×10^{-13}%
Conductive Floors, Uncontrolled Footwear	8%	0.1%	0.004%	4.7×10^{-10}%	4.1×10^{-5}%	7.5×10^{-13}%
Conductive Rubber Floors, Dissipative Footwear	0.003%	1.6×10^{-7}%	1.8×10^{-7}%	1.8×10^{-11}%	7.4×10^{-9}%	8.9×10^{-13}%
Conductive Rubber Floors, Uncontrolled Footwear	0.1%	9.6×10^{-13}%	8.6×10^{-7}%	1.4×10^{-20}%	1.6×10^{-8}%	3.5×10^{-23}%

Source: Determination of the Effect of Humidity on the Probability of ESD Failure or Upset in Data Centers, Moradian et al, 2014

* Using ESD-mitigating flooring and footwear, the risk of ESD upset and damage can be reduced to an insignificant level, even if the humidity is allowed to drop to low values, such as 8%. Unfortunately, controlling the footwear in most data centers is very impractical.

Some organizations prefer that conductive flooring not make electrical contact with racks (see Figure 2) due to the potential impact on system analysis due to a ground path from the rack to the floor. Another consideration is whether contact with grounded racks might alter a floor's surface-to-ground resistance properties. Experimental installations can expose these possibilities prior to specifiers making a final selection.

Combined with static-control chairs and grounding straps, static-control flooring can provide a highly effective, single-expense solution for all types of ICT spaces.

Figure 2: Server room covered with interlocking conductive floor. Note the floor edges are trimmed to avoid contact with the racks

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Dear colleagues, friends, and ESD enthusiasts,

Souvick Mitra
General Chair

On behalf of EOS/ESD Association, Inc. and the 2022 Symposium Steering Committee, it is my honor to welcome you to the proceedings of the 44th Annual EOS/ESD Symposium and Exhibits at The Peppermill Resort & Casino in Reno, Nevada. The EOS/ESD Symposium represents the world's leading forum on Electrostatic Discharge and Overstress. Although COVID-19 is still impacting our business and operations significantly, the Steering Committee and the Technical Program Committee, with all our great volunteers, spared no effort to ensure that the 44th Symposium is a great experience for all attendees, on-site or livestream.

The 44th EOS/ESD Symposium program has six focus areas dedicated to advanced technologies and device testing, automotive, communications, mixed voltage applications, low-power, and EMC. Each focus area comprises sessions with technical papers, invited talks, tutorials, seminars, and workshops. In parallel, the "manufacturing track" offers 3.5 days of technical sessions, hands-on sessions, workshops, discussion groups, and technology showcases in the field of EOS/ESD in manufacturing – control materials, technologies, and techniques.

The Technical Program Committee has selected 23 technical papers for the Symposium covering almost all aspects of the ESD world. These papers are presented by experts from industry and academia, driving leading-edge research and development, and have been peer-reviewed by international experts. Additionally, the RCJ Best Paper authors have been invited to present their work at the EOS/ESD Symposium.

In addition to the submitted technical papers, the Steering Committee invited 17 world-leading experts to present a broad spectrum of EOS/ESD-related topics. In addition, "Topic in Review" presentations address recent developments in the areas of advanced technologies and device testing (Michael Stockinger, NXP Semiconductors), and communications (Michael Khazhinsky, Silicon Laboratories). Hands-on sessions and workshops in the Manufacturing Track focus on recent updates of the ESD control program standards ANSI/ESD S20.20, ESD TR53, and the new technical report ESD TR19.0-01-22 on high reliability ESD control programs.

The EOS/ESD Symposium is the premier international event for professionals in industry and academia working in the field of EOS and ESD to meet and learn about the latest technical findings and innovative designs.

I hope that you will find useful information and new ideas at this year's event!

Sincerely,

Souvick Mitra
2022 EOS/ESD Symposium General Chair

EOS/ESD Symposium Preview

Here are some of the tutorials, workshops, and sessions available during this year's event. Visit https://esda.events for the full schedule.

SUNDAY, SEPTEMBER 18, 2022
ESD Basics for the Program Manager
Operator Training
Safe Equipment Handling in Your EPA Explained
ESD Certified Professional Instructor Course
Basics of ESD and Latch-up Device Physics
ESD EDA Verification Tool
Fundamentals of ESD System Level
ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) - Day 1

MONDAY, SEPTEMBER 19, 2022
EMC
Advanced Technologies & Device Testing
Communication
Manufacturing
ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) - Day 2

TUESDAY, SEPTEMBER 20, 2022
Automotive
Advanced Technologies & Device Testing
Manufacturing

WEDNESDAY, SEPTEMBER 21, 2022
Automotive
Communication
Manufacturing

THURSDAY, SEPTEMBER 22, 2022
Advanced Technologies & Device Testing
EMC
Low Power
Manufacturing

FRIDAY, SEPTEMBER 23, 2022
ESD Professional Program Manager Certification Exam

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Wednesday . . . 9:00 AM - 1:30 PM

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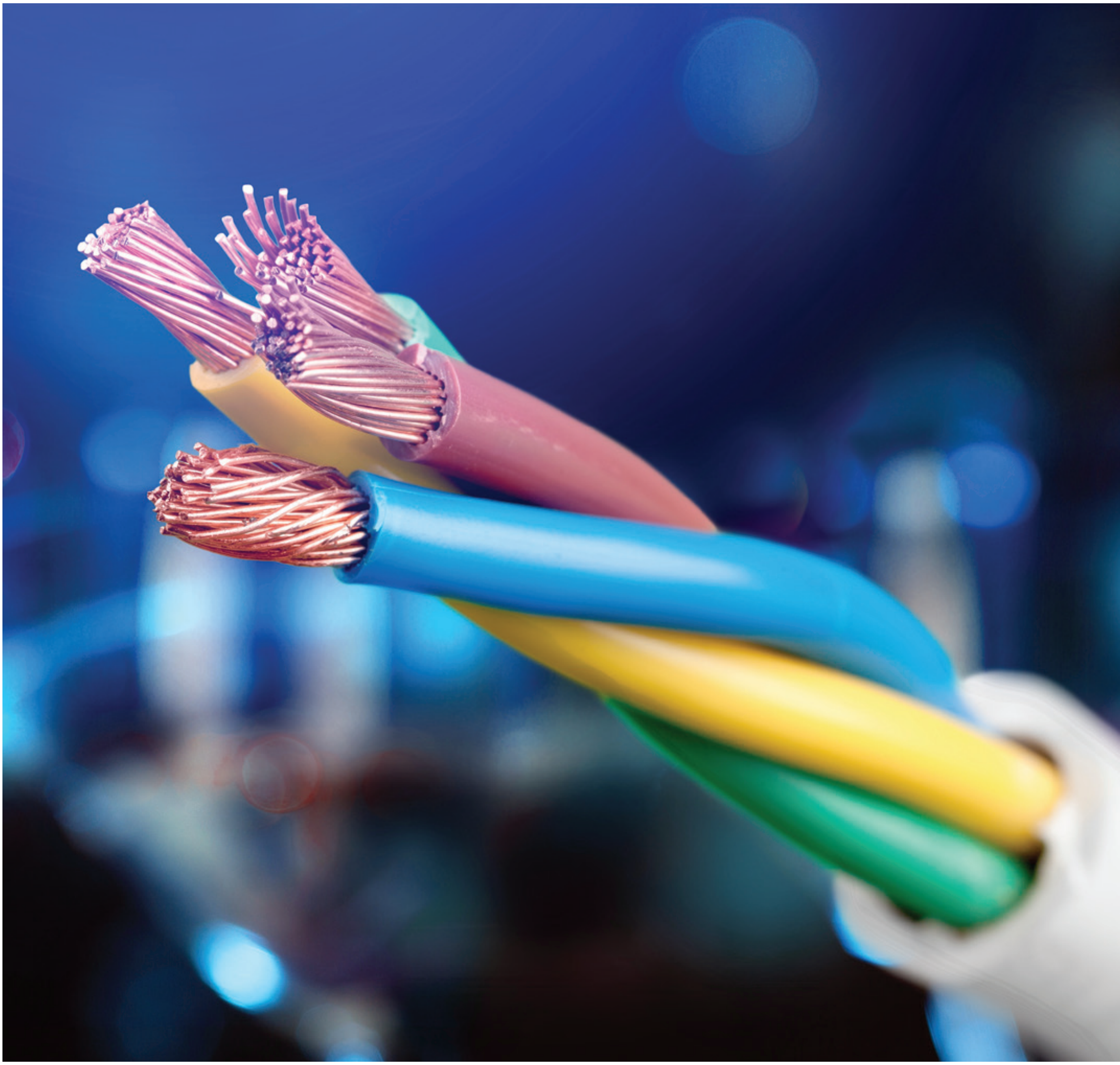
GETTING THE BEST EMC FROM SHIELDED CABLES UP TO 2.8 GHZ, PART 1

How to Terminate Multiple Shields in a Cable Bundle



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By Keith Armstrong

A couple of years ago, I needed to know the shielding effectiveness (SE) of screened[1] cables up to at least 18GHz, but – apart from coaxial cables intended for use in EMC[2] test laboratories – I could only find information up to 100MHz, such as Figure 1.

Accordingly, I set out to make my own measurements with the resources and time made available to me.

In these measurements, I used many different constructions of cable to try to answer the perennial debate about how best to terminate the individual shields of multiple-shielded cables, including single or double overall braids (overbraids), and individual shielded cables contained within an overbraid.

These measurements covered a great deal more than I have described in this brief article, but I am unable to report the other results for confidentiality and/or security reasons.

But before I can describe the cables and results I am permitted to share with you (see Part 2 of this article), I first need to establish the basic rules for terminating cable shields, so that you understand why I did what I did.

UNFORTUNATELY, PEOPLE OFTEN DEVIATE FROM GOOD SHIELDING PRACTICES

Except for conductors designed specifically for use as antennas, all conductors are often called accidental antennas [2]. For this reason, achieving a project's EMC requirements quickly and cost-effectively often requires shielded (sometimes called screened) cables.

For these cable's shields to provide the EMC benefits needed, they must be correctly terminated at their ends. Correct termination techniques for RF have been well-proven for decades (see References [1] and [3] through [14], which span the period 1976 to 2019).

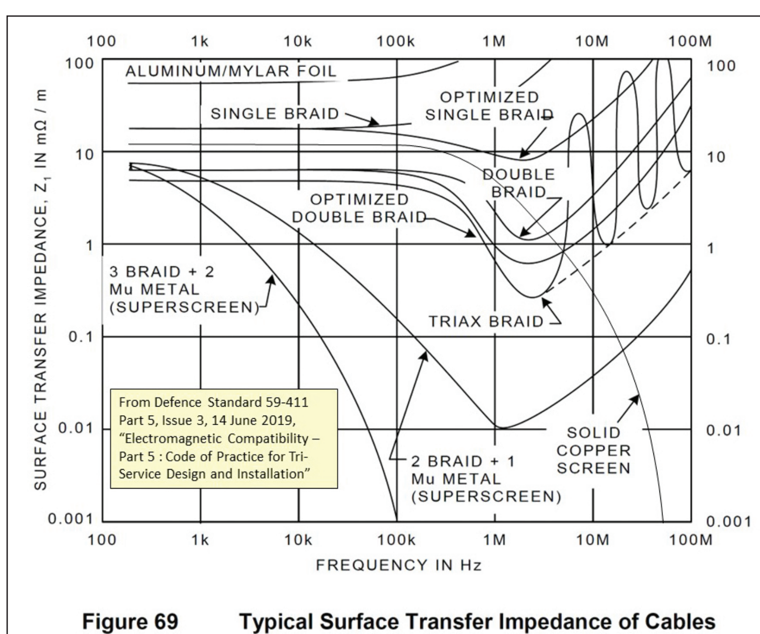


Figure 1: Effect of varying the length of a shield pigtail termination, from [1]

1. In the context of this article, the words: screened; screen, or screening may be replaced by shielded; shield, or shielding respectively, and vice-versa, without any changes in meanings.
2. EMC = Electromagnetic Compatibility, the engineering discipline of ensuring that: a) electromagnetic emissions are low enough for radio/telecommunications and other electronic equipment to function as intended without suffering from unacceptable electromagnetic interference (EMI); and that, b) the electromagnetic immunity of equipment is sufficient for it to function as intended in the electromagnetic environment expected to be present where it is used.

Unfortunately, despite all this publicly available knowledge on well-proven shield termination methods, they are still neither well-known nor widely used.

WELL-PROVEN GOOD EMC PRACTICE: ALWAYS TERMINATE SHIELDS 360°, AT BOTH ENDS

People are always quoting Henry Ott's excellent book [12] to me, claiming that it proves that low-frequency analog signals (such as those used in audio and certain kinds of sensors) must only ever terminate shields at one end. Similar guidelines for low-frequency signals and power also exist in [1], [3] through [11], [13] and [14].

These guidelines were usually acceptable in most ordinary consumer, commercial, and light industrial applications up until the 1990s because their electromagnetic environments were quite benign. But they were never sufficient for applications with very tough electromagnetic environments, as covered by [1] and [3] through [8].

However, when personal/portable computers and digital cellphones became widespread during the 1990s, their large electromagnetic emissions at frequencies up to almost 1GHz meant that IEC and similar EMC test standards for immunity started to test with at least 3 Volts/meter up to at least 1GHz, which is roughly equivalent to a cellphone operating at full power 2 meters away. Such standards were then adopted as part of claiming compliance to the European Union's EMC Directive.

Even electronic circuits that use low-frequency signals (say, below 20kHz) can be expected to demodulate and intermodulate RF noises (say, above 150kHz), as almost every designer of such products who took the trouble to perform these immunity tests discovered. [3] warned about this issue in the mid-1990s.

Now, in the 2020s, we can look back on thirty years of ever-worsening electromagnetic environments, and the EMC test standards for ordinary consumer, commercial, and light industrial applications now have to test immunity up to 6GHz or more. 28GHz will soon be necessary when 5G is extended into that frequency range as planned, see [15] and [16].

These days, the plain fact of the matter is that all analog and digital signals, and all power, are now heavily polluted with conducted RF noises up to at least 6GHz. These are common mode (CM) noises that are both picked up from the noisy electromagnetic environment, and created by the electronics themselves, even being emitted from analog inputs! (See [17].)

The result is that all guidelines for shielding low-frequency signals and power are now insufficient for EMC compliance, and techniques for shielding against high-frequency RF noises are always required, including instances when using RF filtering [18]. Reference [12] and all the other references in this article describe such techniques, and they all require terminating cable shields in 360˚, and at both ends.

Based on my own experience and that of the many EMC experts I know worldwide, the good news is that doing this not only results in good EMC, but also the quickest and most cost-effective project designs, and the quickest and most cost-effective installations (see [19]).

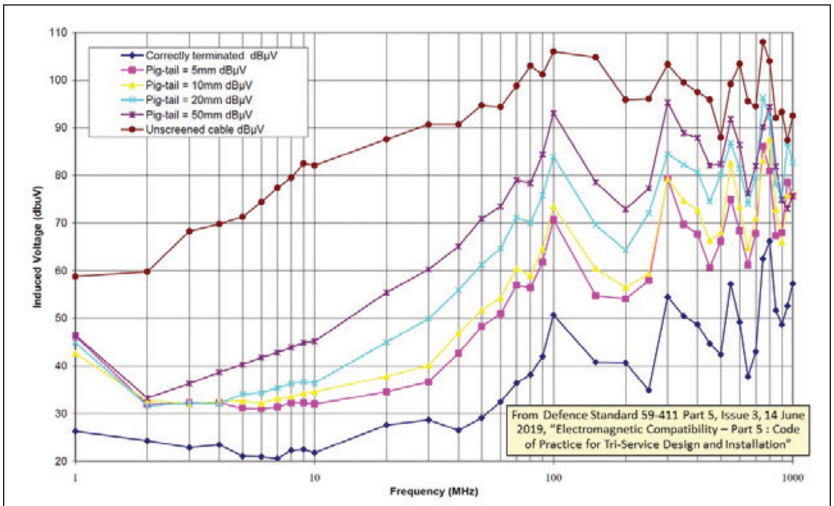


Figure 77 **Induced Voltage on a 0.6 m Cable from a 1 V/m Electric Field for Varying Lengths of Pigtail**

Figure 2: Effect of varying the length of a shield pigtail termination, from [1]

There is also some persuasive real-world evidence for improvements in functional performance where legacy equipment and its installations have been redesigned to use shielded cables terminated in 360˚ at both ends (see the two examples in [20]).

WHAT IS 360° SHIELD TERMINATION?

This is EMC-industry jargon, meaning: direct metal-to-metal connection all the way around.
It is sometimes also referred to as all-around, circumferential, or peripheral termination.

And shield termination is sometimes called shield bonding, shield grounding, or shield earthing. However, I strongly advise against using terms based on ground or earth for anything other than electrical safety purposes (see [21]).

As for worries about so-called ground loops, hum loops, earth loops, etc., when bonding cable shields at both ends, see my blog [22] and remember that bonding cable shields at both ends has been a requirement for military electronics since 1976 (see [3] through [11]).

We can always deal with such noisy loops by circuit design, which I learned how to do in the 1980s. Without such circuit design, the only generic alternative for poor EMC caused by badly shielded cables is to use shielded panel-mounted filters and/or better cable shielding. Of the two, better cable shielding is quicker and more cost-effective unless we are stuck with legacy cable systems that can't be replaced.

Note that fiber-optic converters and their cables may seem costly but can be more cost-effective overall, taking everything into account. I expect them to become more economically favorable year-on-year, going forward.

WHY *NOT* USE PIGTAILS?

All the references at the end of this article warn against using pigtails, sometimes simply called tails.

Figure 2 shows that even a 5mm pigtail makes shielding worse than 360˚ termination by between 10 and 20dB over the range 1MHz to 1GHz. Note that manual pigtailing is very difficult indeed if shorter than 20mm, which Figure 2 shows is up to 30dB worse.

However, the shielding degradation caused by using pigtails instead of 360° terminations depends very much on the test method used. For example, a 1991 study [23] found that using a pigtail in a subminiature 25-way D-type made shielding 20dB worse at 1kHz (only 1kHz!) and 75dB worse at 100MHz (see Figure 3).

I have seen test results showing that pigtails can cause shielded cables to emit more RF noise between 50MHz and 500MHz than an unshielded cable would have. So Figure 3's 75dB degradation at 100MHz could well mean that the cable shield was *amplifying* the RF coupling through its shield, instead of attenuating it as expected.

If, in ten years' time, you remember only two points about this article they should be:

1. Never use pigtails for terminating cable shields; and,
2. Always terminate shields at both ends (dealing with the inevitable ground loops, hum loops, etc., by circuit design, see [22]),

By remembering these two key points, you will almost certainly have saved yourself a great deal of work, cost, and project delays by reducing the number of design iterations required to pass EMC tests. (It is usually practical to design to quickly and cost-effectively design to pass EMC tests the first time, see [19] and [20].)

For a simple method for predicting a cable's SE from measurements of Z_T (surface transfer impedance, as used in Figure 3), see [24].

WHY TEST MULTIPLE SHIELD TERMINATIONS FROM 100MHZ TO 2.8GHZ?

A couple of years ago, I did some work for two suppliers of high-spec military equipment, involving projects that used a great deal of electronics that had to be interconnected with many bulky copper cables or cable bundles carrying analog and/or digital signals and/or power.

As their EMC specifications were required by their customers to be the toughest of all the UK's Defense Standards, these cables or cable bundles were all shielded with two layers of overbraid, directly in contact with each other along their lengths, as recommended by [1].

Many of the cables or cable bundles contained internal braid-shielded twisted-pair (TP) or multicore cables, with their individual braids insulated from the whole cables' or cable bundles' overbraids by their individual plastic jackets.

The customers for these equipment designs had made several of their own proprietary specifications for EMC design, assembly, and installation part of the contract for supply. Unfortunately, their own specifications did not always agree with each other, or with [1] when it came to issues of how to deal with the individual shields and overbraids of the cables or cable bundles.

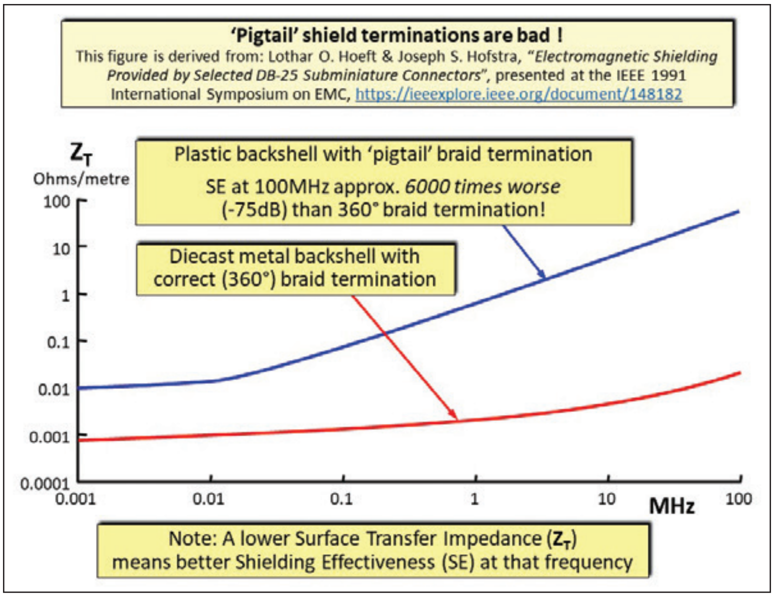


Figure 3: Effect of replacing a 360° shield termination with a pigtail, see [23]

Each designer of the suppliers' equipment cables or cable bundles seemed to have been differently confused by their customers' inconsistent shielding requirements, with the result that different cable assembly drawings often differed from each other in their use of shield termination methods. Some cable assembly drawings even contained an eclectic mix of shield-terminating methods because they had been worked on by different designers at different times.

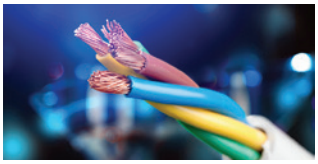
Enquiring as to why this was the case, I discovered that no designers at either supplier even knew about the existence of the official UK guidance on terminating shields in [1], despite compliance with [1] also being part of their contract requirements. This was even the situation with one supplier whose designers I had trained in good EMC design/assembly techniques three years beforehand. They relied almost entirely on subcontract designers, and in the intervening three years, these had all been replaced by new subcontractors who had not attended my course!

As well as the usual issues of which ends of the shields, or both, to terminate, whether pigtails could be used, and whether to connect internal cable shields to the overbraids or not, there was also the issue of whether to insert a thin insulating tube in between two overbraids.

Many of the cable bundles were 2 inches or more in diameter and, when assembled with two overbraids in direct contact with each other along their lengths, very stiff, making them difficult to install in military vehicles. Adding an insulating tube between their overbraids made them usefully more flexible, but I knew (from [3], [4], [1], and other reference materials) that this should reduce their shielding effectiveness (SE).

Some customers' specifications required thin insulating layers between double overbraids without commenting on the likely impact on EMC. This might have been because they wanted the mechanical flexibility and didn't realize that SE could be compromised. But it could also have been because they had seen some of the few references listed below (but not [1], [3], [4], [9], or [10]) that claim (incorrectly, in my view) that placing an insulating film between two overbraids along their length gives a 10 to 30dB improvement in SE, compared with two overbraids in direct contact along their length.

Other issues were that all the measurements I have seen published on cable shielding methods only covered up to 100MHz, and only for coaxial or triaxial cables. However, these projects had to pass the toughest EMC emissions and immunity tests up to 18GHz and were very far indeed from being



I wanted to discover for myself, and for the benefit of other designers on these projects, how best to design and assemble the shields in their cables or cable bundles.

simple coaxial or triaxial types. The guidance in [1], especially that shown in Figure 1, implies that, at and above 1GHz, few shielded cables could be expected to provide any useful shielding at all!

So, I wanted to discover for myself, and for the benefit of other designers on these projects, how best to design and assemble the shields in their cables or cable bundles, and above what frequency we might need to have to use filtering or galvanic isolation techniques (such as fiber-optics) because flexible metal shielding layers would be no use anymore.

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EYE DIAGRAM

PART 2: IMPACT OF DRIVER, HDMI CABLE, AND RECEIVER

By Bogdan Adamczyk, Krzysztof Russa, and Nicholas Hare

This is the second of two articles devoted to the Eye Diagram. Part 1 presented the fundamental definitions and concepts [1]. This article, Part 2, addresses the impact of driver, HDMI cable, and receiver on signal quality using data eye, based on the following criteria: data eye opening, data mask violation, and data jitter.

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Krzysztof Russa is a Principal Engineer at E3 Compliance LLC. He leads High-Speed design efforts related to Signal and Power Integrity challenges. Years of experience in the design industry with balanced use of simulation and measurement techniques have been recognized by awarding him three times the International Mentor PCB Technology Leadership Award. He can be reached at krzysztof.russa@e3compliance.com.

Nicholas Hare is pursuing his Bachelor of Science in Electrical Engineering at Grand Valley State University. He currently works full time as an Electromagnetic Compatibility and Signal Integrity Engineering co-op student at E3 Compliance, which specializes in EMC and high-speed design, pre-compliance, and diagnostics. He can be reached at nicholas.hare@e3compliance.com.

MEASUREMENT SETUP

The study included three different HDMI signal sources, four different HDMI cables, and two different receivers. The block diagram of the measurement setup appears in Figure 1.

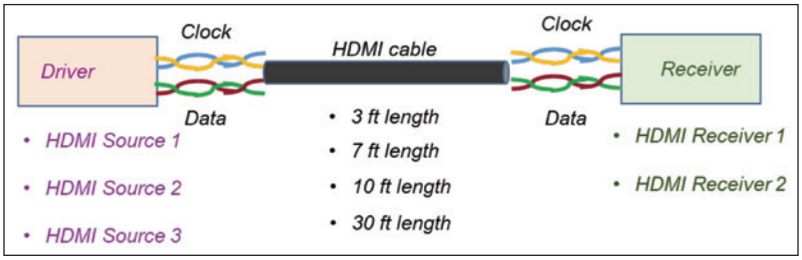

Figure 1: Block diagram of the measurement setup

The study focused on the evaluation of eye diagrams using the following criteria: eye opening, eye mask violations, and data jitter. The data jitter was presented in the form of a histogram.

IMPACT OF HDMI SOURCES

In this part of the study, we compared three different HDMI Sources, while the cable length was the same (3-ft), and the same HDMI Receiver was used (Receiver 1). HDMI Sources used in the study had significant implementation differences. Differences consisted of Driver IC and its configuration, differential trace routing, and HDMI connector style. Figure 2 shows the resulting eye diagrams.

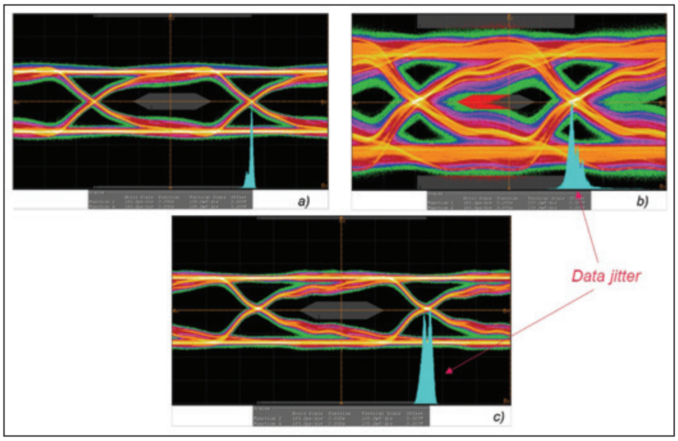

Figure 2: 3-ft cable, same receiver driven by: a) HDMI Source 1, b) HDMI Source 2 c) HDMI Source 3

Observations: HDMI Source 1 and HDMI Source 3 passed the eye diagram test with a significant margin, while the HDMI Source 2 failed (eye mask violation with large data jitter). Data jitter from HDMI Source 1 was smaller than that from HDMI Source 3.

Next, we evaluated the impact of cable length.

IMPACT OF HDMI CABLE LENGTH

In this part of the study, we evaluated the impact of the cable length with HDMI Source 1 or 2 while keeping the HDMI receiver unchanged. Figure 3 shows the eye diagram for HDMI Source 1 and four different cable lengths.

Observations: HDMI Source 1 passed the test for cable lengths: 3-ft, 7-ft, and 10-ft, but a failure was observed for the 30-ft cable. As the cable length increased, the eye opening became smaller, and the date jitter increased.

Figure 4 shows the eye diagram for HDMI Source 2 and four different cable lengths.

Observations: The HDMI Source 2 failed the test for all four cable lengths. Generally, as the cable length increased, the eye opening became smaller, and the data jitter became larger.

IMPACT OF HMDI RECEIVER

In the final stage of the study, we used the same driver, same cable, and two different receivers. Figure 5 shows the corresponding eye diagrams.

Observations: Both receivers passed the test with a similar amount of jitter. The eye opening of the Receiver 1 was slightly larger than that of the Receiver 2.

SUMMARY AND CONCLUSIONS

This article addressed the impact of driver, HDMI cable, and receiver on signal quality using data eye, based on the following criteria: data eye opening, data mask violation, and data jitter. The study has shown that all three system components affect the eye diagram. Measurement results have shown a correlation between data jitter and data eye mask opening; as the data jitter increases, the data eye opening gets smaller. The impact of the receiver in our study was less pronounced than the impact of the driver. The most obvious observation was the shorter the cable, the better the data quality.

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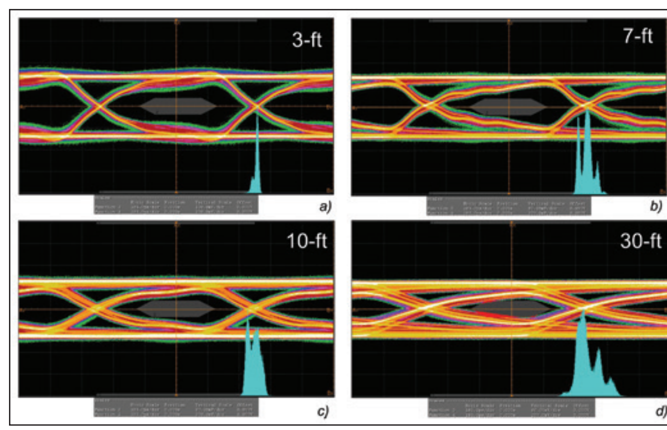

Figure 3: Impact of cable length driven by HDMI Source 1

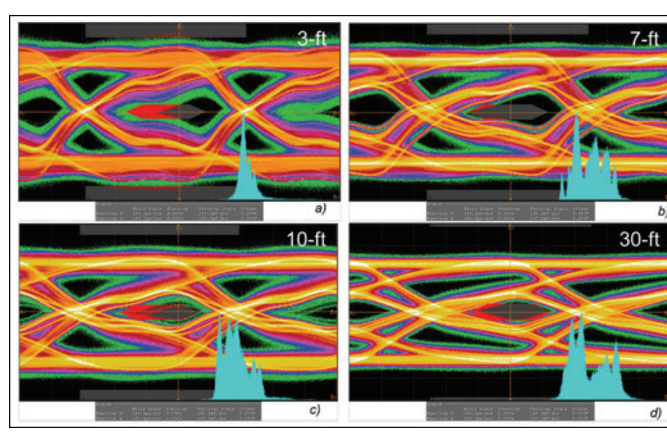

Figure 4: Impact of cable length driven by HDMI Source 2

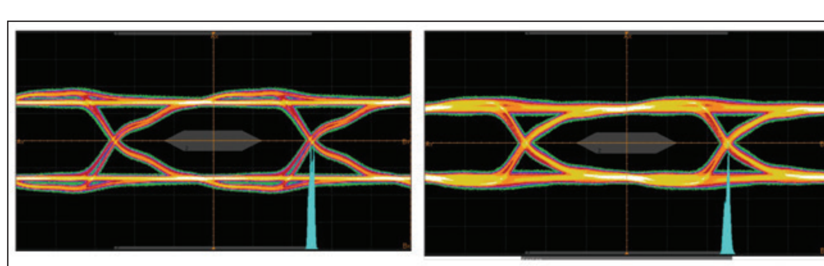

Figure 5: Eye diagram: a) HDMI Receiver 1, b) HDMI Receiver 2

INDUSTRY COUNCIL'S LATCH-UP SURVEY

By Theo Smedes for EOS/ESD Association, Inc.

Theo Smedes began work in ESD in 2000 and currently is Fellow for ESD, Latch-up and EOS within NXP Semiconductors. He published several papers on ESD and introduced an ESD design course within NXP. Theo is member of all ESDA device testing working groups and is chair of the TLP working group. He has been a member of the Industry Council on ESD Target Levels since it was founded in 2006.

Founded in 1982, EOS/ESD Association, Inc. is a not-for-profit, professional organization dedicated to education and furthering the technology of Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, and tutorials, and fosters the exchange of technical information among its members and others.

In July 2020, the Industry Council on ESD Target levels, in collaboration with the JEDEC JESD78 working group, launched a survey on latch-up testing. As described in an earlier article [1] in this magazine, the survey was conducted to better understand how the present latch-up standard (JESD78 revision E) is interpreted and used in the industry. The article also invited representatives from the industry to participate in order to collect data and opinions. The survey is closed, but a pdf version is still available at https://www.esdindustrycouncil.org/ic/docs/latchupsurvey2020.pdf.

This article provides a high-level overview of the Industry Council paper "Survey on Latch-up Testing Practices and Recommendations for Improvements," which describes the full analysis of the collected responses and lays a path for potential adaptations needed to accommodate its use in future technologies and applications. Based on the survey results, we summarize the key issues documented in the paper that include problems with the latch-up standard and its application. Based on that analysis, the compiled results suggest improvements for better understanding and future JESD78 related testing. This article serves explicitly as an invitation to read the published paper, which is freely available from the Industry Council website [2] and will also become available via the JEDEC website [3].

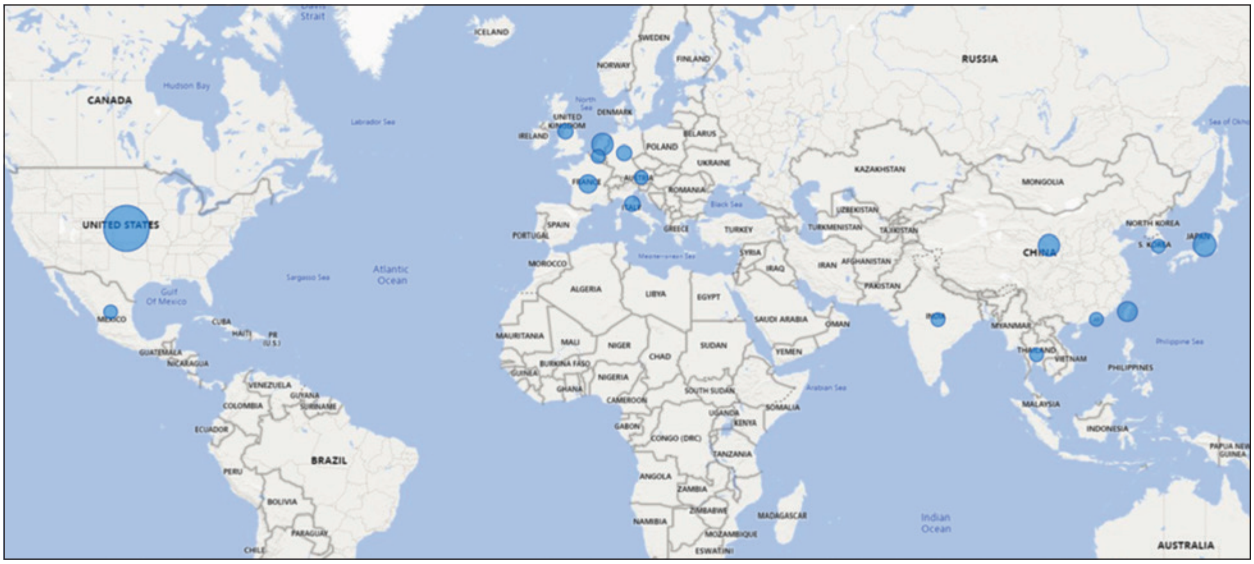

Figure 1: Global distribution of responses. The size of the dots is an indication for the number of responses from a country.

LATCH-UP SURVEY AND ANALYSIS PROCESS

The Industry Council received 70 individual responses from at least 35 companies from more than 16 countries. The distribution over the globe is illustrated in Figure 1. Multiple responses per company were encouraged because of the wide diversity of products, customers, and requirements. This makes it likely that different approaches to latch-up testing may be used even within one company.

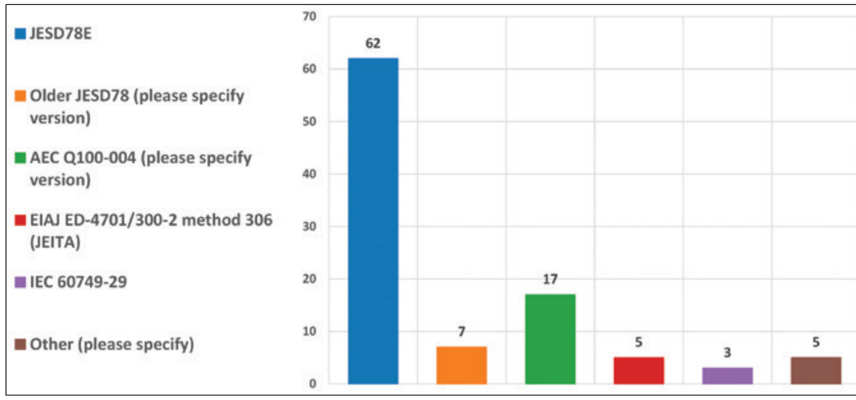

Figure 2: Pareto of Latch-up standards being used as reported by the respondents

Based on questions with respect to market space, business type, and applications, we can conclude that the respondents cover the industry well. Notable exceptions are OEMs using analog ICs. Although the survey was oriented at Revision E of the JESD78 standard, it is relevant to know which standards are actually used. Figure 2 shows that although other test standards and older JESD78 revisions are also used, the most prevalent standard in use is JESD78E. This gives good confidence in the relevance of the responses with respect to the survey's goals.

The survey was divided into nine sections, each addressing sub-topics like Field Returns, Test Execution, Failure Criteria, etc. More details on the structure of the survey are provided in Chapter 1 of the paper. The survey was set up to answer high-level questions such as:

- How is the test standard interpreted and executed across the industry?
- Which real-life events does JESD78 intend to simulate? Do these occur in present-day applications?
- The prescribed voltage compliance limits prevent any significant current injection for low voltage pins. Is that intended and/or desired?
- Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
- What changes should be made to the standard to better suit the reality of present-day and future technologies and products?

Chapter 2 of the paper describes the detailed analysis of the responses in relation to the questions mentioned above. An effort was made to address topics in the same sequence as the questions appeared in the survey. The analysis is meant to strictly report and summarize the respondents' information and find potential correlations between different topics. However, whenever the analysis team felt it was appropriate to offer a "possible interpretation," it was indicated using a special box format with the disclaimer that other interpretations would be possible.

CONCLUSIONS AND RECOMMENDATIONS

The conclusions and recommendations are provided in Chapter 3 of the paper. Some of the key results are summarized below. To fully understand the survey results, it is strongly recommended to read the full report.

One of the most relevant questions is if JESD78 latch-up testing ensures the robustness of products in the field. Related key findings are:

- JESD78 is considered useful and should not be removed.
- It is evident that passing JESD78 testing is insufficient to guarantee latch-up robustness in the field, as shown in Figure 3, and seems to be more related to the type of stress rather than the levels.
- Respondents see value in JESD78 testing for modeling real-world stress events beyond the specified test conditions.

Another major topic is the assessment of how large the latch-up problem is in practice. Examples of findings related to this are:

- Figure 4 shows the majority of latch-up fails are reported during the JESD78 qualification test, and many of these fails result in a re-spin, but this accounts for a very small fraction of the total number of re-spins as shown in Figure 5.
- More than 50% of all latch-up failures (field + JESD78 testing) do not require a re-spin, but the failure drives alternative mitigations such as board modifications or software changes

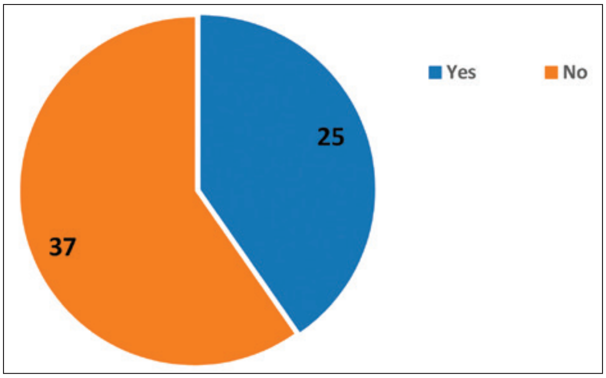

Figure 3: Pie Chart of [Q41], "Does passing JESD78 testing guarantee latch-up robustness in the field?"respondents

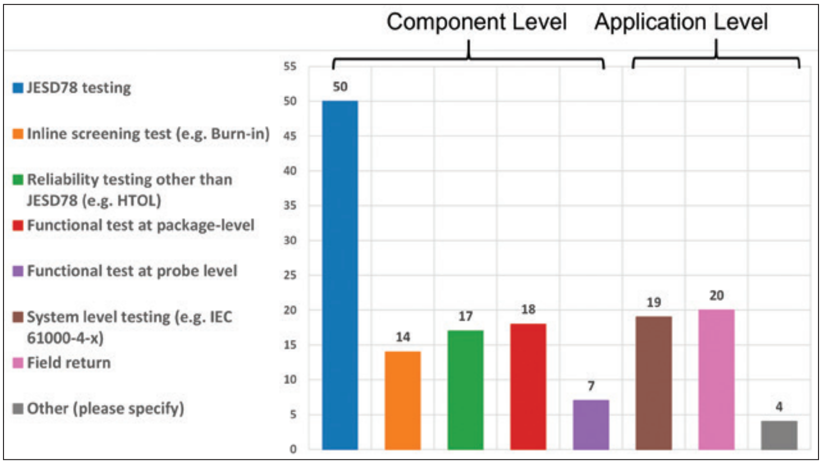

Figure 4: Feedback to [Q12], "Where have you experienced latch-up failures?" in the Case where [Q11], "Have you experienced latch-up failures?" Was Answered "Yes"

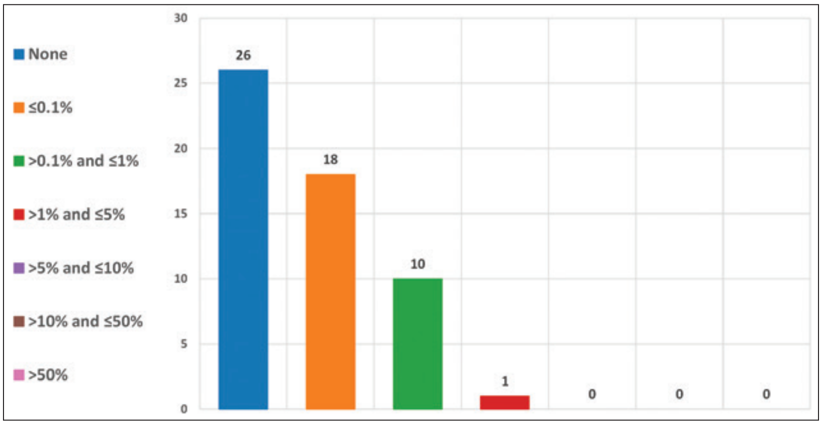

Figure 5: Pareto of [Q21], "What percentage of your company's product re-spins were due to latch-up failures in a system application?"

Figure 4 shows at what step latch-up was detected, Figure 6 shows the root causes, and Figure 5 shows how often such cases led to re-spins.

The last highlighted topic is the question if the standard is sufficiently clear. It appears that some concepts in the standard are not interpreted the same way by all users and sometimes are even used incorrectly. The most important example is:

- The concept of the "Maximum Stress Voltage" is well-known in the industry but very often misinterpreted or incorrectly applied to JESD78 testing
- Many respondents believe that the pin stress voltage should not exceed the product AMR, see Figure 7

Key recommendations for possible improvements and extensions of JESD78E are listed below. Some may reach beyond the JESD78 specification – they may appeal to other industry bodies, symposia, trainers, vendors, etc. Section 3.2 of the paper gives a more comprehensive list of recommendations.

- Create a JESD78 user guide with practical explanations, hints, and examples.
- Provide seminars and workshops aligned with the latest JESD78 revision F release, discussing the major changes from JESD78 revision E and its implications to LU testing.
- Consider ways to standardize LU testing at the application level (System Level ESD, Transient LU).

OUTLOOK

During the development of this survey and paper, the JEDEC JESD78 working group prepared and released a next revision of the JESD78 standard. Chapter 3, Section 3.3 concludes the paper with a summary of the major differences between JESD78 revision E and JESD78 revision F and relates this to the recommendations provided.

Overall, the survey results indicate a dire need to improve the definition and understanding of the latch-up test standard and cover a broader range of applications. The Industry Council releases this paper to help focus the work to accomplish that.

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3. Website JEDEC: https://www.jedec.org

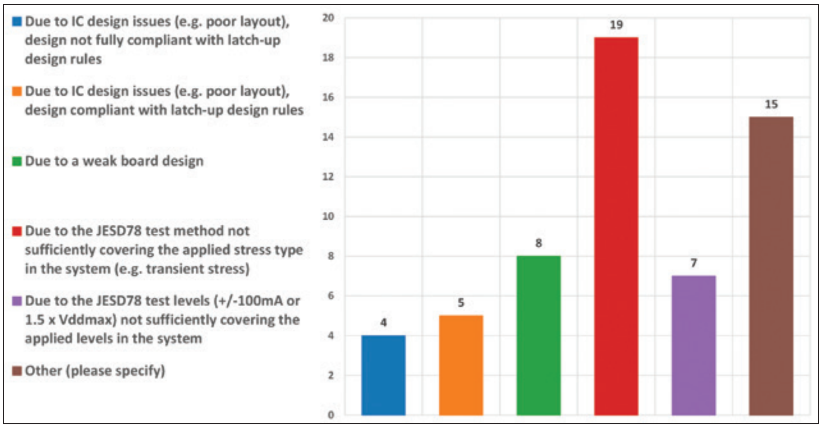


Figure 6: Distribution of Responses for [Q20], "For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?"

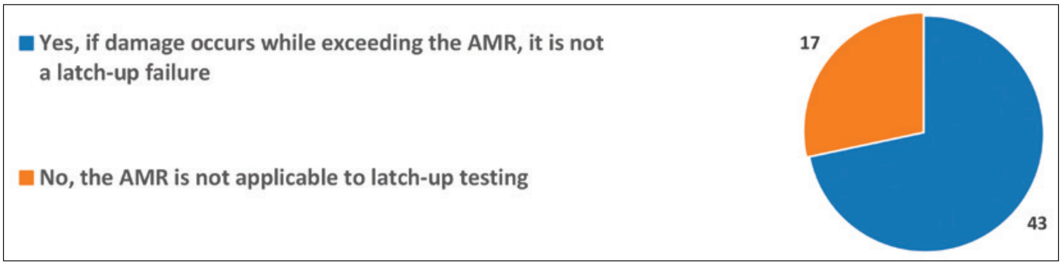


Figure 7: Pie Chart of Responses to [Q90], "Do you set the pin stress voltage limits so that they do not exceed the product AMR?"

Banana Skins

394 GHz radar pulses can interfere with motor cars

Because of their mobility, vehicles will be placed in many different kinds of Electromagnetic environment. From driving next to transformers and high voltage power lines operating at 50 or 60Hz to driving next to airports where the approaching and landing radars operate at 1.2 to 1.4GHz and 2.7 to 3.1GHz.

Manufacturers of vehicles found some isolated cases where vehicles in the proximity of airports and military bases were affected by the radiated fields from radar systems. The high fields from the radar interfered with the normal operation of critical systems in the vehicle. These systems included braking controls and airbag deployment. Given the importance of the problem the management of vehicle manufacturers applied pressure on the EMC departments to come up with a test plan to check components (what the auto industry often call electronic sub-assemblies, or ESAs – Editor) for electromagnetic immunity to these pulses.

Both Ford Motor Company and General Motors Worldwide introduced sections in their immunity standards for component testing to radar pulses. Generating 600V/m pulses at these frequencies requires the use of high power amplifiers and/or very high gain antennas. In the process of developing antennas optimised to meet these requirements, several issues with the test were discovered. While the test can be done it requires very expensive equipment that is not easily afforded by many small component manufacturers and test houses. As a result of some of the anomalies seen during the testing of the antenna prototypes Ford have made some changes to the tests described in their document.

(Taken from: "High Field Radar Frequency Pulse Test for Automotive Components", V Roderiguez et al, EMC Society of Australia Newsletter, Issue 35, December 2006.)

395 Telecomm globalisation and related interference issues

Some uniformity does exist in the requirements of the POTS (plain-old-telephone-system), at least in how the equipment works. Regulatory standards that the phone equipment must comply with vary from country to country, however. No one knows this fact better than the designers at Silicon Labs. Many years ago, they set out to design a modem that would comply with every standard in the world. Thus, they created the Isomodem line of chips.

The name of one system block of all modems, the DAA (direct-access arrangement), provides a clue to the challenges that designers face. The chips must ultimately interface with the real-world twisted-pair wiring, which can encounter lightning strikes and line-cross events. A line cross occurs when the electric power that is running on the same utility poles as the telephone lines breaks and falls across the phone line. In some regions of the United States those utility poles carry 440V-ac power, and peak voltage is more than 600V. European lines, on the other hand, directly distribute 240V (actually 230V rms, 240V only in the UK – Editor). Nevertheless, the standards for the line-cross event differ all over the world.

In the United States, FCC Part 68 specifies the design limits and testing and requires surge testing at 1500V. In Europe, European standard EN 55024 specifies the limits and does testing at 1000V. Real-world conditions are even more demanding: A line-cross event may generate only a few hundred volts on a phone line, but a lightning strike can far more voltage, and the rise time of that event will be short. Designers at Silicon Labs have seen field voltages of 4500V.

(Taken from "Globalisation and Analog", by Paul Rako, EDN Global Report 3, December 2006.)

396 Some power quality issues for products marketed worldwide

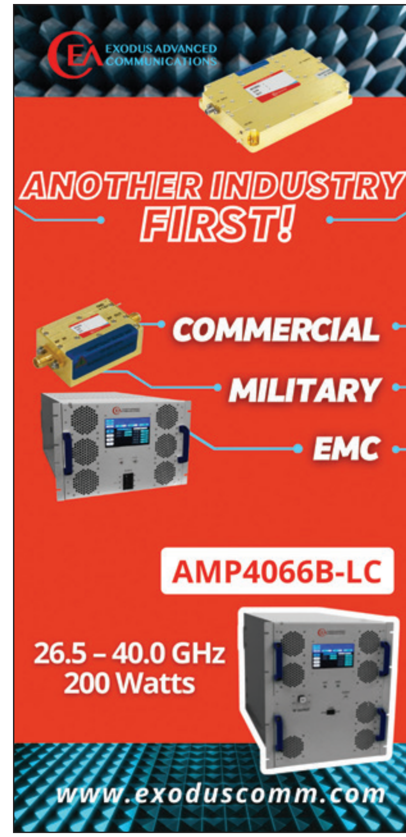
To compete in the global market, today's analog ICs must address a wide range of application and vo9ltage requirements," says Doug Bailey, vice-president of marketing for Power Integrations. "For example, we know that Japan's ac main can be as low as 90V power, whereas Europe uses 240V (actually 230V rms, 240V only in the UK – Editor). At first blush, this information seems like enough to design a power supply that will operate worldwide. The reality is more difficult. In India, the power grid is unreliable, forcing many big electricity consumers to use private generators during outages.

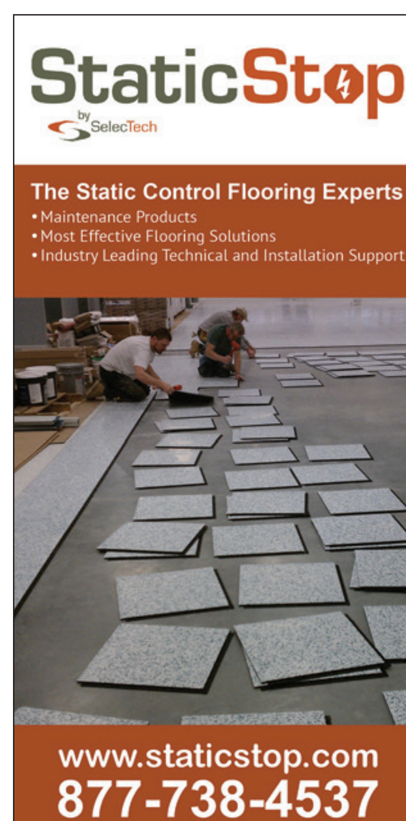
When the power goes down, and the generators switch in, numerous line spikes occur. When the power grid comes back up, everyone's using generators. The power grid is unloaded, so the voltage can overshoot and ring for several minutes. The resulting surges can go as high as 400V. Products have to be able to handle these extremes, so our application circuits must cover ultra-wide ranges of voltage and help ensure that our chips withstand the spikes.

(Taken from "Globalisation and Analog", by Paul Rako, EDN Global Report 3, December 2006.)

The regular "Banana Skins" column was published in the EMC Journal, starting in January 1998. Alan E. Hutley, a prominent member of the electronics community, distinguished publisher of the EMC Journal, founder of the EMCIA EMC Industry Association and the EMCUK Exhibition & Conference, has graciously given his permission for In Compliance to republish this reader-favorite column. The Banana Skin columns were compiled by Keith Armstrong, of Cherry Clough Consultants Ltd, from items he found in various publications, and anecdotes and links sent in by the many fans of the column. All of the EMC Journal columns are available at: https://www.emcstandards.co.uk/emi-stories, indexed both by application and type of EM disturbance, and new ones have recently begun being added. Keith has also given his permission for these stories to be shared through In Compliance as a service to the worldwide EMC community. We are proud to carry on the tradition of sharing Banana Skins for the purpose of promoting education for EMI/EMC engineers.

PRODUCT Showcase





Advertiser Index

Upcoming Events

Due to COVID-19 concerns, events may be postponed. Please check the event website for current information.

September 5-8
EMC Europe 2022

September 13-15
The Battery Show

September 13-15
Fundamentals of Random Vibration and Shock Testing Training

September 13-16
Lab Techniques, Robust Design, and Troubleshooting

September 18-23
44th Annual EOS/ESD Symposium

September 20
IEEE Rock River Valley EMC Seminar

September 20-22
ISPCE 2022

September 20-23
Applying Practical EMI Design & Troubleshooting Techniques

Advanced Printed Circuit Board Design for EMC+SI

Mechanical Design for EMC

September 29
2022 Minnesota EMC Event

October 6-7
Fundamental Principles of Electromagnetic Compatibility and Signal Integrity

October 9-14
AMTA 2022

October 17-20
Military Standard 810 (MIL-STD 810) Training

October 18
2022 San Diego Test Equipment Symposium