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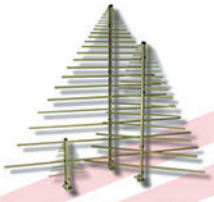

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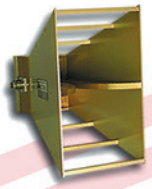

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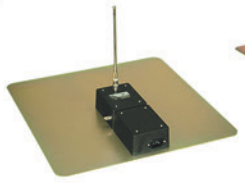

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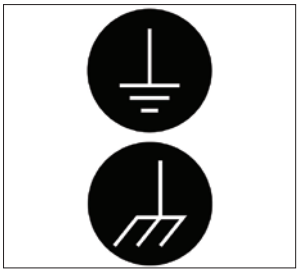

Boston, Raleigh to be Designated as FCC Innovation Zones

The U.S. Federal Communications Commission (FCC) has proposed adding Boston and Raleigh (NC) to its list of areas for advanced wireless communications and network innovation research.

According to a press release, Acting FCC Chairperson Jessica Rosenworcel proposed the additions to help expand the agency's efforts to help foster the development and integration of 5G network technologies and open radio access networks (RANs). If adopted by the Commission, Boston and Raleigh would join New York City and Salt Lake City under the agency's Innovations Zones initiative, which seeks to expand the geographic areas where those holding experimental program licenses can conduct research and testing of these technologies.

The Boston Innovation Zone would be centered at Northeastern University, while the Raleigh Innovation Zone would be based on collaborations with North Carolina State University.

Rosenworcel's proposed changes to the Innovation Zones initiative would also expand the New York City Innovation Zone to include three Columbia University and City College of New York campus areas.

FCC to Require Electronic Filing of International Applications, Reports

The U.S. Federal Communications Commission (FCC) has extended its requirements for the electronic filing of applications and reports submitted to the agency for review.

The Commission will require that all reports and applications administered by its International Bureau be filed electronically through its International Bureau Filing System (IBFS). The expanded requirements will apply to Section 325(c) Applications, Applications for International High Frequency Broadcast (IHF) Stations, and Dominant Carrier Section 63.10(c) Quarterly Reports.

The FCC's Order also removes duplicate paper filing requirements for satellite cost-recovery International Telecommunications Union (ITU) declarations.

The Commission says that the decision to expand its mandatory electronic filing requirements is part of its overall efforts to streamline the filing process, reduce the costs for applicants, carriers, and Commission staff, and increase the transparency of this information.

Report Addresses Fires Attributable to Lithium Batteries

As part of an effort to reduce the risk of fires caused by lithium batteries in waste electrical and electronic equipment (WEEE), a consortium of industry groups has just issued a report that compiles a number of "good practices" applicable to all phases of the product development process.

The report, "Recommendations for Tackling Fires Caused by Lithium Batteries in WEEE," compiles the findings of an industry survey conducted in 2019 by a consortium of EU-level associations of WEEE manufacturers and recyclers.

Part 2 of the report provides a compilation of the findings of that survey, listing nearly 30 different recommendations and good practices for reducing the risk of fires associated with WEEE batteries and addressing issues related to design, collection, and logistics, as well as policy matters.

The report makes clear that there is no "magic formula that will reduce to zero the risk of fires caused by WEEE containing batteries."

EU Commission Updates Harmonized Standards for In Vitro Devices

The Commission of the European Union (EU) has updated its list of harmonized standards applicable to in vitro medical devices to reflect the latest available technical and scientific information.

According to Commission Implementing Decision (EU) 2021/1195, two new standards can now be used to demonstrate compliance with applicable requirements of the EU's In Vitro Diagnostic Device Regulation, (EU) 2017/745. These are:

- EN ISO 11737-2:2020, "Sterilization of health care products – Microbiological methods – Part 2: Tests of sterility performed in the definition, validation and maintenance of a sterilization process (ISO 11737-2:2019)"
- EN ISO 25424:2019, "Sterilization of health care products – Low temperature steam and formaldehyde – Requirements for development, validation and routine control of a sterilization process for medical devices (ISO 25424:2018)"

In addition, the Commission's Implementing Decision designated amendments to current harmonized standards, as follows:

- EN ISO 11135:2014/A1:2019, amendment to "Sterilization of health care products – Ethylene oxide – Requirements for the development, validation and routine control of a sterilization process for medical devices (ISO 11135:2014)"
- EN ISO 11137-1:2015/A2:2019, amendment to "Sterilization of healthcare products – Radiation – Part 1: Requirements for development, validation and routine control of a sterilization process for medical devices (ISO 11137-1: 2006, including Amd 1: 2013)"

Under Commission rules, compliance with an EU harmonized standard confers a presumption of conformity with the corresponding essential requirements in EU harmonization legislation once the standard has been published in the *Official Journal of the European Union*.

TOWARD STANDARDIZATION OF LOW IMPEDANCE CONTACT CDM

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By Nathan Jack, Brett Carn, and Josh Morris

Editor's Note: *The paper on which this article is based was originally presented at the 41st Annual EOS/ESD Symposium, where it was awarded the Symposium Outstanding Paper in 2020. It is reprinted here with the gracious permission of the EOS/ESD Association, Inc.*

INTRODUCTION

The field-induced Charged Device Model (CDM) test method standardized in ANSI/ESDA/JEDEC JS-002 [1] is widely used for CDM qualification of integrated circuits. Because it relies on an air spark to initiate the stress, the pulse amplitude varies from zap to zap [2]. This discharge variation is increasingly significant as pre-charge voltage V_{pre} decreases [3].

Relay-based alternatives have been proposed to eliminate the variable air spark [2], [4]. Such "contact CDM" (CCDM) systems rely on transmission line pulsing and utilize 50 Ω coaxial cables and relays. It has been shown that 50 Ω systems generate pulses much wider than those of JS-002, but a better match can be obtained using lower system impedances. In [3], CCDM systems of 50 Ω, 25 Ω, and 11 Ω impedances were demonstrated. It was theorized that a 16.6 Ω CCDM system would provide the closest match to JS-002 in terms of waveform shape and the failure current (I_{fail}) thresholds generated.

In this work, a 16.6 Ω "Low Impedance" Contact CDM system (LICCDM) is demonstrated. This system complies with the newly published CCDM Standard Practice 5.3.3 [5]. The waveform shape and I_{fail} threshold generated during stress of a 32 nm test chip are compared against those of JS-002. It is shown that JS-002 produces non-monotonic peak currents (I_{peak}) at low V_{pre}. LICCDM is monotonic and enables low voltage testing with higher accuracy. LICCDM and JS-002 are shown to exhibit the same I_{peak} dependency on the effective device capacitance C_{eff}. Recommendations for merging JS-002 and LICCDM in a future standard are proposed.

LICCDM

A simplified hardware schematic of LICCDM is shown in Figure 1. The charge cable is charged and then quickly discharged through a relay. A transmission line pulse is delivered through a rise time filter to the device under test (DUT) by way of a coaxial cable connected to the pogo pin. A second coaxial cable is connected in parallel to the first and delivers the transmitted pulse to an oscilloscope. A 50 Ω resistor is also connected between the pogo pin and ground. The effective impedance of the system as seen by the DUT is hence 50 Ω || 50 Ω || 50 Ω = 16.6 Ω. Displacement current

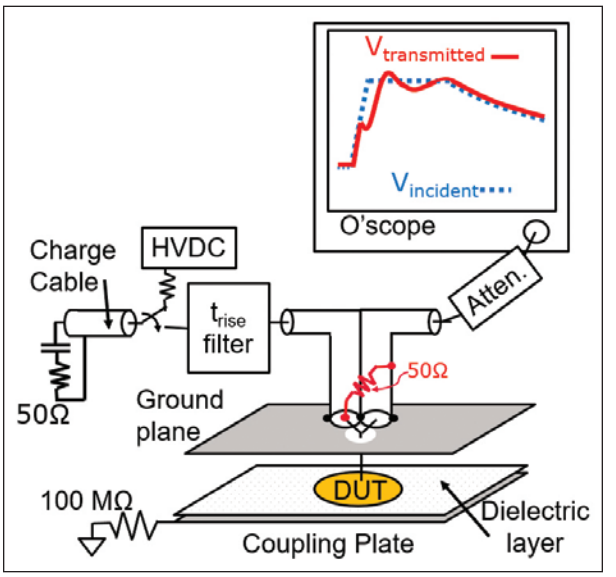


Figure 1: Simplified hardware schematic of Low Impedance Contact CDM (LICCDM). Two coaxial cables – one for pulse delivery and the other for measurement – connect to the pogo pin along with a 50 Ω shunt resistor. The effective impedance of the system is thus 16.6 Ω.

stresses the DUT during the pulse rising edge. The RC termination results in a slow decay of the falling edge of the incident pulse, thereby preventing dual-polarity stress to the DUT. By subtracting the transmitted voltage waveform from the incident waveform and dividing by the system impedance, the current through the DUT can be determined [3]. The pogo pin is in contact with the DUT both before and after the stress; hence, the only spark that occurs is within the relay.

The LICCDM test head is used on a Thermo Fisher Orion2 tester. The waveforms generated when stressing the large and small verification modules (coins) on both JS-002 and LICCDM are shown in Figure 2. Because the effective RLC models of the two testers are similar, the waveforms generated share close resemblance [3]. The LICCDM V_{pre} required to obtain a given I_{peak} is approximately three times larger than that of JS-002. This is because the LICCDM V_{pre} is applied to the charge cable rather than directly to a field plate (JS-002). This charge cable V_{pre} is then divided as it travels through the transmission line network such that the actual voltage at the test head is approximately equal to the V_{pre} applied to the JS-002 field plate.

TEST CHIP MEASUREMENTS

LICCDM and JS-002 were used to stress a test chip fabricated in a 32 nm CMOS process. A 37mm x 37mm LGA package was used. Some pins of this chip were known to fail below 250 V, so characterization at low voltages was conducted to determine an appropriate step size and starting voltage.

Zap-to-zap variability

When characterizing a device to determine the CDM failure threshold, it is desirable to use a step

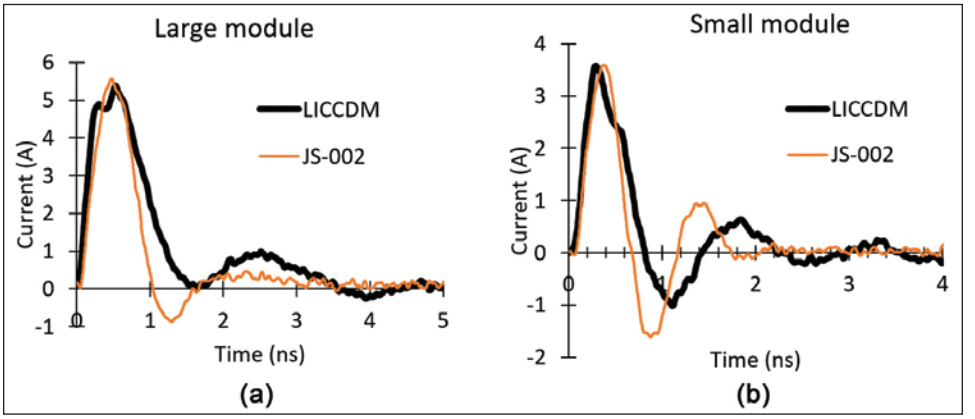


Figure 2: Discharge waveforms from the large and small verification modules. The JS-002 is taken at 250 V, while the LICCDM voltage is scaled to match the peak current.

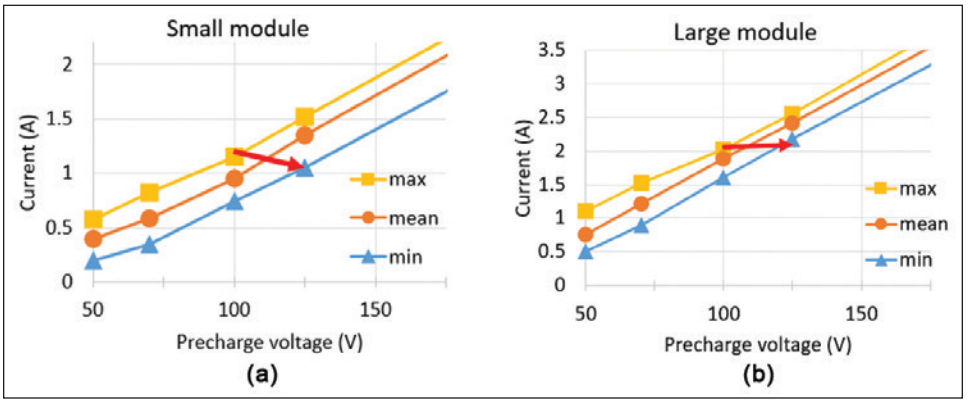


Figure 3: The max, min, and average I_{peak} measured during 50 zaps to the verification modules using JS-002. The red arrows indicate the non-monotonic behavior in I_{peak} that is possible when incrementing V_{pre} by 25 V.

When characterizing a device to determine the CDM failure threshold, it is desirable to use a step size that is a small percentage of the threshold being resolved.

size that is a small percentage of the threshold being resolved. For example, while a 50 V step size in V_{pre} may be adequate for resolving a failure occurring near 500 V, that same step size is relatively large when resolving a 125 V failure. However, it is well documented that air discharge CDM testing suffers from zap-to-zap variability arising from the variable nature of the spark [2], [3]. The step size must not be so small that the zap-to-zap variability in I_{peak} is larger than the expected increment in I_{peak}. Figure 3 shows the variation when stressing the small and large verification modules at various V_{pre}. A 25 V step increase in V_{pre} could result in no increase or even a decrease in I_{peak}, as shown by the red arrow in Figure 3. Based on these data, testing with less than a 50 V step size would not be meaningful because I_{peak} would be non-monotonic with V_{pre}.

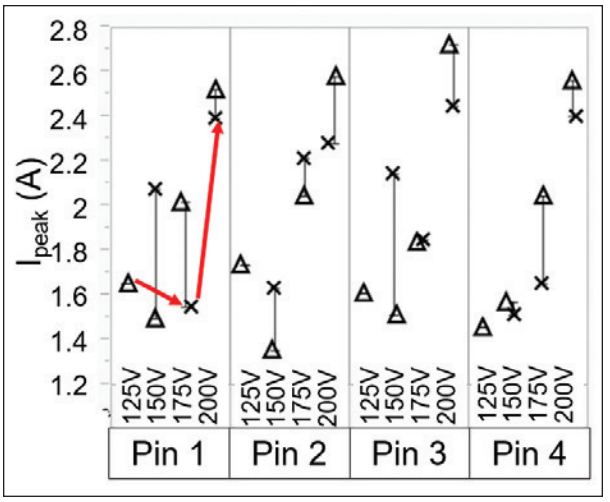


Figure 4: Measured I_{peak} from stress to the test chip at a given V_{pre} using JS-002. Data from single zaps to two units are displayed, both represented by a different symbol. A non-monotonic relationship with V_{pre} is exhibited (red arrow).

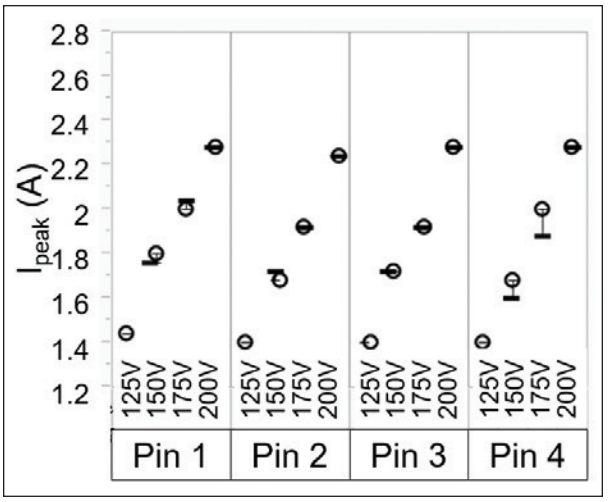


Figure 5: Measured I_{peak} from stress to the test chip at a given V_{pre} using LICCDM. Data from single zaps to two units are displayed, both represented by a different symbol.

The variation measured on verification modules is a best case scenario: the modules have a large, uniform surface on which to discharge. When testing a package pin, I_{peak} will also vary with pin shape and pogo pin alignment [6]. Figure 4 shows the I_{peak} obtained from two units when measuring four pins of the test chip using JS-002. A single stress to each pin was used at a given V_{pre}. In between each voltage step the unit was removed for parametric testing and then re-aligned before incrementing V_{pre}. The re-alignment procedure introduces another variable in the I_{peak} distribution. Despite 25 V increments to V_{pre} from 125 V to 175 V, I_{peak} actually decreases in some cases (red arrows in Figure 4). Increasing V_{pre} from 175 V to 200 V causes more than a 60% I_{peak} increase. These data indicate that even a 50 V step size is too small to avoid non-monotonic behavior; this makes it difficult to determine the true I_{fail} of the pin.

The same experiment is repeated using LICCDM to stress the test chip. Figure 5 shows a very repeatable, linear relationship between I_{peak} and V_{pre}. Because contact is made with the pin before the stress is applied, there is no air spark. Furthermore, minor differences in pogo pin alignment have no impact on I_{peak}. With zap-to-zap variation eliminated, a very fine step size in V_{pre} can be used. This enables the true I_{fail} to be extracted, even at low discharge currents and voltages.

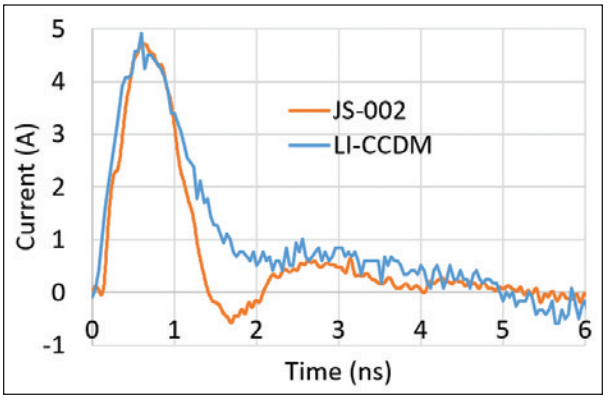


Figure 6: Test chip waveforms from a center package pin

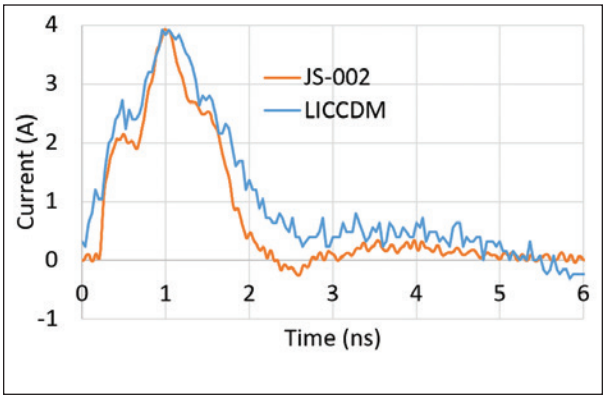


Figure 7: Test chip waveforms from a pin near the package edge

Pin location dependent variability

Sample waveforms from the test chip measurements are shown in Figures 6 and 7. Waveforms from the center of a package tend to be narrow, while those at the edge are wider and often have multiple peaks [7]. These variations are due to the parasitic elements of the discharge path *within* the DUT; charge from across the package takes longer to reach an edge pin than a center pin. LICCDM captures this natural source of variation which increases the likelihood of I_{fail} correlation with JS-002.

Failure threshold comparison

The I_{fail} of several different I/O circuits on the test chip were compared for both LICCDM and JS-002. Figures 8 and 9 show the I_{fail} of various output driver pins. In all cases the output driver itself was the anticipated location of failure. The I_{fail} levels generated by both testers are comparable in Figure 8. In Figure 9 some unit to unit variation is observed for both JS-002 and LICCDM. This makes it more difficult to compare I_{fail} levels. However, the thermally induced voltage alteration (TIVA) analysis in Figure 10 on page 14 indicates that failures occurred in the driver transistors when stressed by both JS-002 and LICCDM.

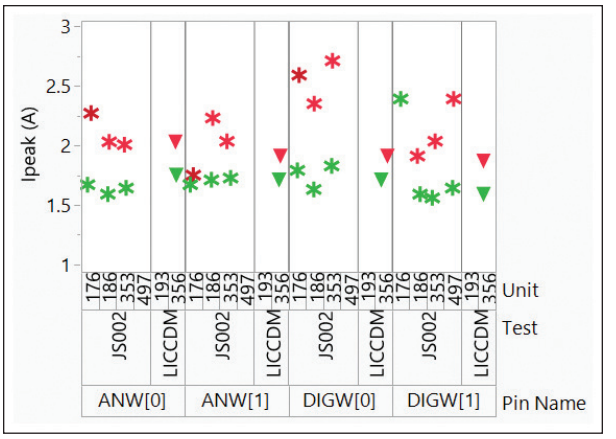


Figure 8: I_{peak} measured on four pins from multiple units. Green indicates no failure, while red indicates damage.

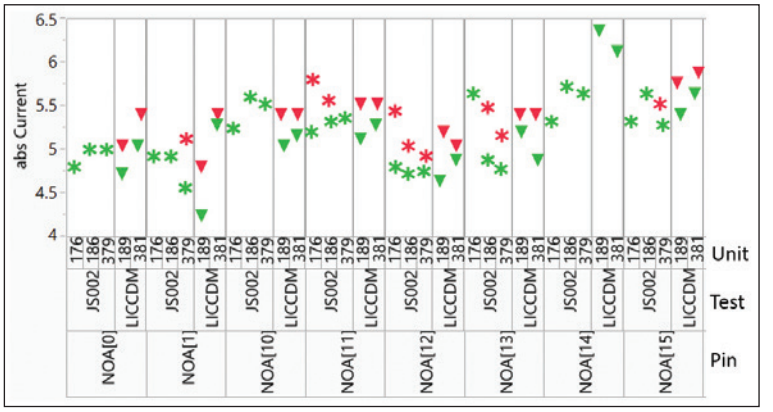


Figure 9: I_{peak} measured on eight pins from multiple units. Green indicates no failure, while red indicates damage. Unit to unit I_{fail} variation was more prevalent for this pin type, but the general trend aligns between both testers.

The test results from differential input pins with impedance matching termination resistors are shown in Figure 11 (all pins) and Figure 12 (CLKIN pins). The TIVA analysis in Figure 13 indicates failure in the termination resistor. Again, good correlation is observed between test types. The other pins in Figure 12 are general purpose input/output pins. No failures occurred on either test up to approximately 6 A.

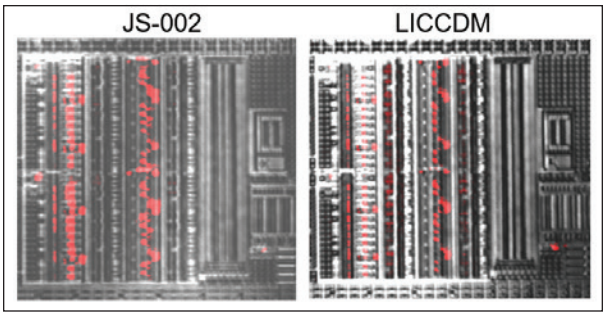


Figure 10: TIVA image of a pin from Figure 9 showing the same damaged regions of the driver after JS-002 and LICCDM stress

I_{peak} DEPENDENCE ON V_{pre}, C_{eff}

It was shown in [3] that CDM I_{peak} can be captured as a single, continuous function $I_{peak} = f(V_{pre}, C_{eff})$. In that work, the older "C101" air discharge test method [8] was used. This function is here applied to JS-002 (Figure 14) and LICCDM (Figure 15) using data taken on seven differently sized verification module coins. The area of these coins ranges from 4 mm² to 1500 mm². A good fit across V_{pre} and C_{eff} is achieved. Note that the plots represent the maximum I_{peak} observed out of 50 zaps to each coin. While runt pulses are increasingly common and reduce the mean I_{peak} at low V_{pre} during air discharge testing [3], the maximum I_{peak} is very predictable down to single-digit V_{pre}.

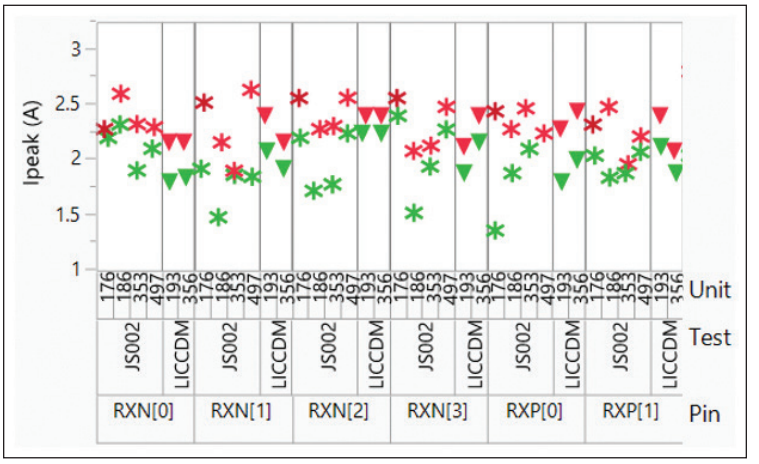


Figure 11: I_{peak} measured on six pins from multiple units. Green indicates no failure, while red indicates damage.

The models from Figures 14-15 are overlaid in Figure 16. The JS-002 standard has an I_{peak} tolerance specified for two coin sizes at discrete "Test Conditions" (TCs) of 125 V and upward. These are indicated on the plot by solid black lines. The 1000 V, 250 V, and 125 V model curves from Figure 14 are thickened and shaded in Figure 16. The thickness represents the allowed JS-002 tolerance if it were extended across the entire C_{eff} range. While LICCDM (solid thin lines) is slightly less dependent on C_{eff} than JS-002, it can generate I_{peak} within the allowed JS-002 I_{peak} tolerance using a set V_{pre}.

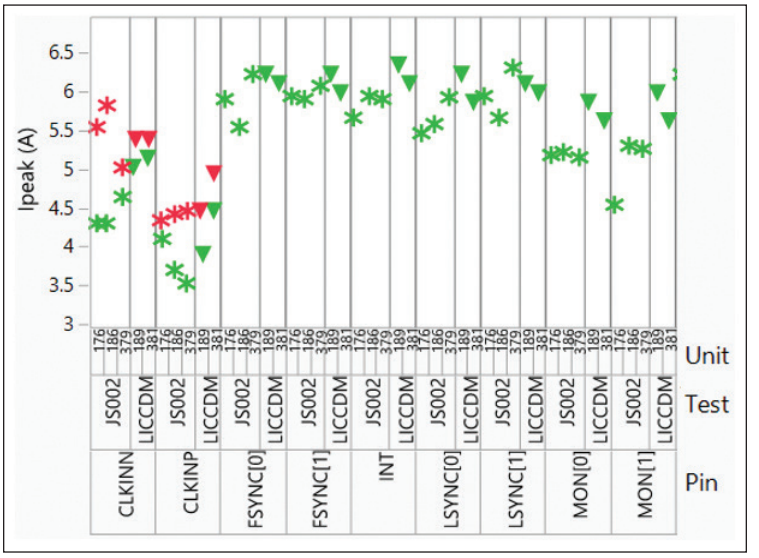


Figure 12: I_{peak} measured on nine pins from multiple units. Green indicates no failure, while red indicates damage.

STANDARDIZATION

While the LICCDM Standard Practice is a powerful CDM characterization tool, it cannot be used in lieu of JS-002 until it achieves Standard designation. This

section describes the importance of investigating LICCDM for inclusion in a future Standard and what the next steps and considerations should be.

The need for LICCDM in a standard

This paper has highlighted several undesirable characteristics of air discharge CDM testing: zap-to-zap variation; sensitivity to pogo pin alignment; and non-monotonicity at low V_{pre}. These drawbacks will be increasingly impactful as design targets reduce below 250 V. Air discharge testing has other problems not addressed in this work. Packages with tight pin pitch are difficult to test with certainty because the spark from the pogo pin may strike any of the neighboring pins [9], [10]. Furthermore, the pogo pin may be larger than the pin being tested [9], [10]. Sharpening the tip can alter the onset of the spark generation and the corresponding waveform due to the corona effect [9].

LICCDM overcomes all of the above-mentioned problems because the pogo pin contacts the device pin prior to discharge. In addition to eliminating zap-to-zap variation, any uncertainty regarding which pin was stressed on a tight pin pitch package is also eliminated. A sharper, thinner pogo pin can also be used for testing small pins. This could conceivably be done at dimensions as small as the bare die level. The ability to test tight pitch, small dimension package pins will become increasingly important as package dimensions shrink to accommodate smaller form factors and faster signaling rates.

The need for more data

Given the decades-long history much of the industry has with air discharge CDM testing, it is highly desirable that any new test method replicate the stress and failure mechanisms of air discharge (i.e., JS-002

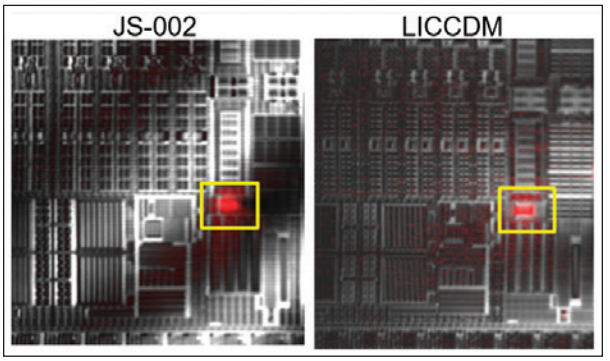


Figure 13: TIVA image of an input pin from Figure 11 showing damage in the termination resistor after JS-002 and LICCDM stress

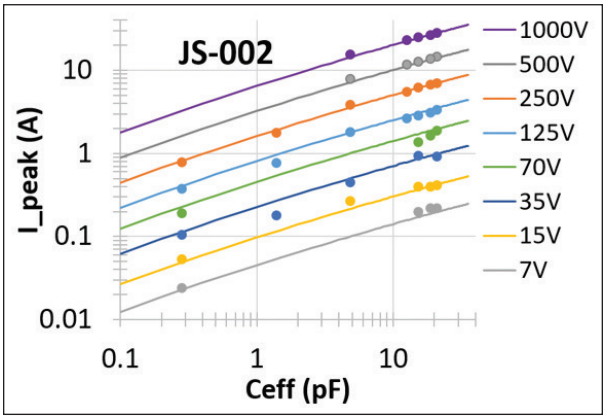


Figure 14: JS-002 I_{peak} data (dots) from seven differently sized verification coins and the continuous function fit to the data (solid curves). The maximum I_{peak} of 50 zaps is used to capture the worst scenario.

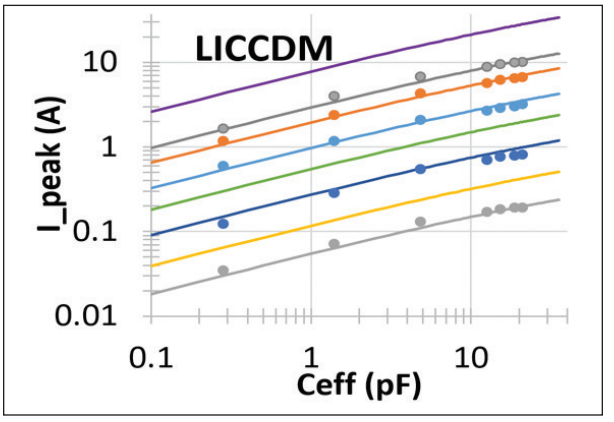


Figure 15: LICCDM I_{peak} data (dots) from the same seven differently sized verification coins and the continuous function fit to the data (solid curves)

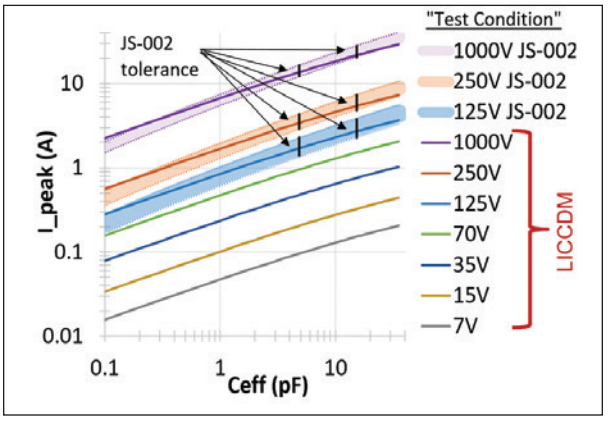


Figure 16: JS-002 model with I_{peak} tolerance (shaded thick, from Figure 14) compared to LICCDM model (solid thin, from Figure 15)

The industry must decide what degree of correlation is required between LICCDM and JS-002 before LICCDM can be adopted.

today). While this work and [3] have shown strong correlation between the two methods, a larger body of data is needed before LICCDM standardization.

An important first step is an industry-wide round robin to examine the I_{peak} vs. C_{eff} relationship of the two testers as was done in Figure 16. This can initially be done with verification module coins of varied sizes as was done in this work. JS-002 compliant testers from many manufacturers should be used along with multiple LICCDM tools.

Next, device level testing on a range of product applications and technologies should be conducted at multiple companies using both test methods. Failure mechanisms, locations, and I_{peak} should be compared. While many CDM-induced device failures are driven by I_{peak}, others are driven by pulse rise time. Recent works have highlighted this as a potential source of miscorrelation when using relay-based alternative CDM test methods. In [11] it was postulated that a very fast-rising event occurs during air discharge testing as the capacitance between the pogo pin and the ground plane charges. This rapid event is not accurately measured by the disk resistor but was shown to be the likely cause of failure on a sensitive product. Relay-based methods were only able to replicate this failure by generating sub-100 ps rise times. The same was true in [12]; a miscorrelation between air discharge and relay-based Capacitively Coupled TLP (CC-TLP) was only resolved with sub-100 ps rise times. LICCDM and CC-TLP can generate these fast rise times, but it complicates the hardware setup. Given that the sub-100 ps rise time is not accurately measured on JS-002 today, relay-based testers like LICCDM and CC-TLP actually offer a more accurate alternative. A broader product study can help the industry decide how crucial it is to replicate these rapid rise time events and what the correct waveform would look like.

Finally, the industry must decide what degree of correlation is required between LICCDM and JS-002 before LICCDM can be adopted. Given the drawbacks of JS-002 and the future direction of shrinking packaging technology and reduced CDM target levels, the benefits of LICCDM will likely outweigh infrequent miscorrelation.

Framework for a future CDM test standard

An inclusive CDM standard was proposed in [3] that would allow a wide range of test methods to be used interchangeably. Such an approach required a unique V_{pre} adjustment for every DUT using a C_{eff}-dependent look-up table. The results in Figure 16 suggest that a simpler approach can be taken: LICCDM can achieve the existing JS-002 tolerance specifications without a DUT-by-DUT V_{pre} adjustment. If supported by round robin results, both air discharge and LICCDM (and possibly other methods) could be used interchangeably following nearly the same test procedure outlined in JS-002:

1. Keep the existing JS-002 small / large verification module I_{peak} + tolerance limits as-is. Add a third very small verification module (with corresponding limits) to be verified before testing very small devices.
2. Verify the tester by essentially following the JS-002 procedure. As is typical today with JS-002, the actual V_{pre} will not match the TC voltage. The software would apply a single scale factor to adjust V_{pre} such that the I_{peak} requirements are satisfied for all three modules. For LICCDM, this scale factor would be larger (approximately 3x) because V_{pre} is applied to the charge cable.
3. Specify the pertinent details of the waveform shape. It may be necessary to specify the rise time and pulse widths at multiple points (e.g., specify pulse width at 20%, 50%, and 80%). Product level correlation studies will inform these decisions.
4. Specify a TC above which either LICCDM or air discharge methods can be used. Below this TC, only LICCDM (or a similar relay-based tester

compliant to #1 - #3 above) should be used to avoid significant variability.

5. Report the results in terms of the legacy Test Condition voltage. The $I_{peak} = f(V_{pre}, C_{eff})$ continuous function could optionally be published to inform users of the expected I_{peak} at any TC for a given C_{eff}.

CONCLUSIONS

LICCDM shows strong correlation with JS-002 across a wide range of V_{pre} and C_{eff}. The I_{fail} generated using either JS-002 or LICCDM were equivalent on a 32 nm test chip. LICCDM eliminates a number of problems inherent with JS-002 air discharge testing, namely: zap-to-zap variation, non-monotonicity at low V_{pre}, and inaccurate testing of products with tight pin pitch or small pin dimensions. A simplified approach to a standard inclusive of air discharge and LICCDM is proposed, allowing either tester to be used interchangeably. Further data collection is needed at multiple sites and on a variety of products to determine the limits to apply to waveform parameters (e.g. rise time).

ACKNOWLEDGEMENTS

The authors thank the ESDA/JEDEC CDM Joint Working Group for valuable discussion that shaped the direction of this work. The authors thank Thermo Fisher for manufacturing and loaning the LICCDM test head used in this work.

REFERENCES

1. "Charged Device Model (CDM) – Device Level", ANSI/ESDA/JEDEC, JS-002, 2018.
2. R. Given, M. Hernandez, and T. Meuse, "CDM2 – A New CDM Test Method for Improved Test Repeatability and Reproducibility," *Proc. EOS/ESD Symp.,* 2010, pp. 359-367.
3. N. Jack and T. Maloney, "Low Impedance Contact CDM," *Proc. EOS/ESD Symp.,* 2015.
4. H. Wolf, H. Gieser, W. Stadler, and W. Wilkening, "Capacitively coupled transmission line pulsing CC-TLP—A traceable and reproducible stress method in the CDM-domain," *Proc. EOS/ESD Symp.,* 2003.
5. "Low Impedance Contact CDM as an Alternative CDM Characterization Method," ANSI/ESD, SP5.3.3-2018.
6. T. Brodbeck, K. Esmark, and W. Stadler, "CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts," *Proc. EOS/ESD Symp.,* 2007, 1A.1.
7. J. Di Sarro, B. Reynolds, and R. Gauthier, "Influence of package parasitic elements on CDM stress," *Proc. EOS/ESD Symp.,* 2013, 9A.3.
8. "Field-induced charge-device model test method for electrostatic discharge withstand thresholds of microelectronic component," JEDEC, JESD22-C101F, 2013.
9. Industry Council on ESD Target Levels, May 2016, "White Paper 2: A case for lowering component level CDM ESD specifications and requirements."
10. R. Ashton, M. Johnson, S. Ward, "CDM Testing of Small Integrated Circuits," *In Compliance Magazine*, June 2010.
11. D. Johnsson, K. Domanski, and H. Gossner, "Device Failure from the Initial Current Step of a CDM Discharge," *Proc. EOS/ESD Symp.,* 2018.
12. J. Weber et al., "Comparison of CDM and CC-TLP Robustness for an Ultra-High Speed Interface IC," *Proc. EOS/ESD Symp.,* 2018.

Dear colleagues, friends, and ESD enthusiasts,

Wolfgang Stadler
General Chair

On behalf of EOS/ESD Association, Inc. and the 2021 Symposium Steering Committee, it is my honor to welcome you to the proceedings of the 43rd Annual EOS/ESD Symposium and Exhibits at The Westin La Paloma Resort & Spa in Tucson, Arizona. The EOS/ESD Symposium represents the world's leading forum on Electrostatic Discharge and Overstress. Although COVID-19 is still impacting our business and operations significantly, the Steering Committee and the Technical Program Committee, with all our great volunteers, spared no effort to ensure that the 43rd Symposium is a great experience for all attendees, on-site or virtually online.

In the 43rd EOS/ESD Symposium, the Steering Committee and the Symposium Strategy Team have structured the program in five focus areas, each with a program of 1-1.5 days. The focus areas are Advanced Technologies and Device Testing, Automotive, Communications, Mixed Voltage Applications, and, as in the last years, EMC. Each focus area comprises one or several sessions with technical papers, invited talks, tutorials, seminars, and workshops. For the first time, the Symposium started on Monday and was, therefore, one day longer than in the past, allowing more time for program and discussion. In parallel, for the fifth time, the "Manufacturing Track" offers full 3.5 days of technical sessions, hands-on sessions, workshops, discussion groups, and technology showcases in the field of EOS/ESD in manufacturing – control materials, technologies, and techniques.

The Technical Program Committee has selected 26 technical papers for the Symposium covering almost all aspects of the ESD world, including five technical papers for the Manufacturing Track. These papers were presented by experts from industry and academia, drive leading-edge research and development, and have been peer-reviewed by international experts. Additionally, the RCJ Best Paper authors have been invited to present their work at the EOS/ESD Symposium.

In addition to the submitted technical papers, the Steering Committee invited world-leading experts to present their thoughts on the focus areas. Eleven invited talks and six seminars cover a broad spectrum of EOS/ESD-related topics. In addition, "Topic in Review" presentations address recent developments in the areas of analog and high-voltage technologies (Lorenzo Cerati, ST Microelectronics), CDM test methods (Nathan Jack, Intel), and high-speed communications (Kathleen Muhonen, Qorvo). Hands-on sessions and workshops in the Manufacturing Track focus on recent updates of the ESD control program standards ANSI/ESD S20.20, ESD TR53, and the new standard practice ANSI/ESD SP17.1 on ESD process assessment.

The EOS/ESD Symposium is the premier international event for professionals in industry and academia working in the field of EOS and ESD to meet and learn about the latest technical findings and innovative designs.

I hope that you will find useful information and new ideas in these proceedings!

Sincerely,
Wolfgang Stadler
2021 EOS/ESD Symposium General Chair

Here are some of the tutorials, workshops, and sessions available during this year's event.
Visit https://www.esda.org/events/43rd-annual-eosesd-symposium-and-exhibits for the full schedule.

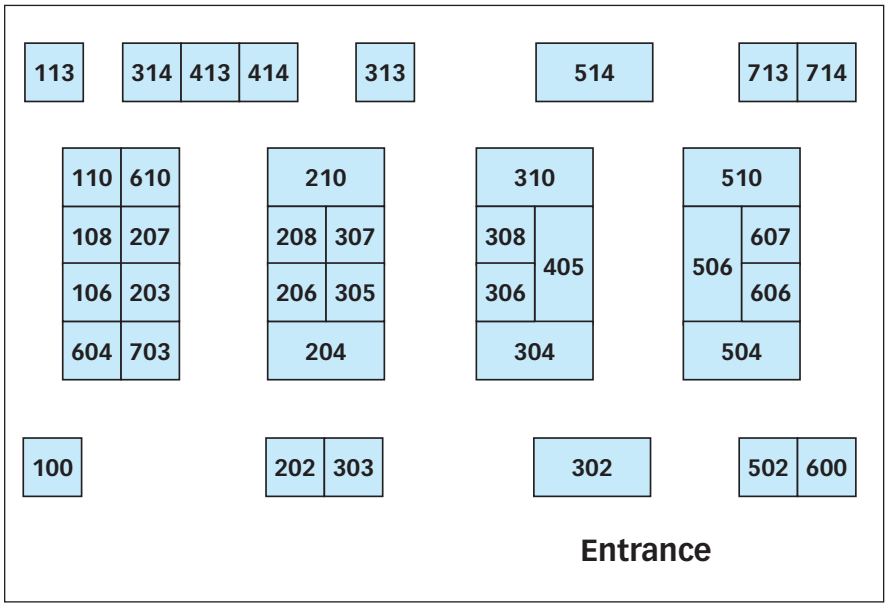
SUNDAY, SEPTEMBER 26, 2021
ESD Protection and I/O Design
System Level ESD/EMI (Principles, Design Troubleshooting, & Demonstrations
ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar)
Design for EOS Reliability
Practical Applications of Ionization

MONDAY, SEPTEMBER 27, 2021
Mixed Voltage Applications
Advanced Design and Technologies
Manufacturing
ESD/EOS in Automotive Applications
5G Communication

TUESDAY, SEPTEMBER 28
Analog and High Voltage Technologies
CDM Test Methods
Manufacturing

WEDNESDAY, SEPTEMBER 29
ESD/EOS in Automotive Applications
EMC
Manufacturing
High Speed Communication

THURSDAY, SEPTEMBER 30
Automotive
EMC
Future Testing Methodologies
Manufacturing



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Industry Council Survey on Latch-up: A Brief Status Update

By Theo Smedes (NXP Semiconductors) for the Industry Council on ESD Target Levels

In July 2020, the Industry Council on ESD Target levels, in collaboration with the JEDEC JESD78 working group, launched a survey on Latch-up testing. An earlier article[1] in this magazine described the reasons for launching the survey and invited representatives from the industry to participate in order to collect data and opinions. The survey is now closed, but a full pdf version of the survey[2] is still available online. This article will give a short update on the results of the response analysis that is ongoing.

The Industry Council received 70 individual responses, from at least 35 companies from more than 16 countries. Multiple responses per company were encouraged because of the wide diversity of products, customers, and requirements. Although the survey was oriented at Revision E of the JESD78 standard, it is, of course, relevant to know which standards are actually used. The responses show that although other test standards and older JESD78 revisions are also used, the most prevalent standard in use is JESD78E. This gives good confidence in the relevance of the responses with respect to the survey's goals.

A high-level analysis of the responses shows interesting observations and allows preliminary conclusions:

- The responses give insight into the occurrence of Latch-up failures at different stages in the IC qualification process, application qualification process, and in the field. For example, answers to [Q06]3 show that the complaint rate for Latch-up based fails is low for most customers.
- A topic of debate in the Latch-up community is the definition of Latch-up. Historically, Latch-up is associated with the presence of a parasitic thyristor. From responses to [Q47], it can be concluded that the majority considers that the definition should be much broader. A significant group of respondents agrees with the generic definition 'anything that causes sustained current increase'.
- Most respondents consider the Latch-up test method relevant, even with significance beyond the boundaries of the applied waveforms. Still, significant reservations to the usefulness are listed [Q09], and roughly 50% of the responses indicate that JESD78 alone is insufficient [Q49], [Q50].
- There is considerable disagreement on what should and should not be considered a Latch-up failure, but only 5% of the responses stated that the current (JESD78E) criteria were sufficient.
- The responses on questions related to Maximum Stress Voltage (MSV) and Absolute Maximum Rating (AMR), clearly suggest that in practice these are often equated. Since that is not the intent of the method, this feedback indicates that a better explanation is needed, possibly accompanied by additional education using webinars or tutorials.

All in all the survey results indicate that there is a need to improve the definition and understanding of the Latch-up test standard, as well as a need to cover broader ranges of applications. The full analysis of all responses is in progress and will be incorporated into a report that has recently been started. A more detailed analysis and summary will be presented at the 2021 EOS/ESD Symposium in September. This will be followed by the full report published by the Industry Council and JEDEC.

More information on the Industry Council on ESD Target Levels can be found here: http://www.esdindustrycouncil.org/ic/en. ■

Theo Smedes began work in ESD in 2000 and currently is Fellow for ESD, Latch-up, and EOS within NXP Semiconductors. He published several papers on ESD and introduced an ESD design course within NXP. Theo is a member of all ESDA device testing working groups and is chair of the TLP working group. He has been a member of the Industry Council on ESD Target Levels since it was founded in 2006.

1. "Industry Council Launches Survey on Latch-Up," *In Compliance Magazine*, July 2020, pp. 20-21
2. Full link to the survey: https://www.esdindustrycouncil.org/ic/docs/latchupsurvey2020.pdf
3. [Qxy] indicates question xy in the survey document that can be found via the link mentioned in the text

STATIC CONTROL FLOORING IN HIGH RELIABILITY ENVIRONMENTS

Special Considerations for Static Control Flooring for Added Risk Reduction

Tom Ricciardelli is the President and Founder of SelecTech, Inc., which makes a complete line of static control flooring systems sold through its StaticStop division. He has been involved in static control for more than 20 years and is an active member of the EOS/ESD Association, where he serves as Chairman of the Flooring and Healthcare committees. Ricciardelli can be reached at tricca@selectech.com.

By Tom Ricciardelli

Static control flooring is widely used throughout the electronics industry to provide a means to ground personnel and mobile equipment to control static charge generation and build-up. While I'd argue that it is always important to control static in an electronics manufacturing environment, there are some organizations where the risk of a device failure could have more serious consequences. This raises the bar in terms of managing the risk of failure and there are some things you should keep in mind when choosing static protective flooring to help with that.

WHAT IS HIGH RELIABILITY?

A group of researchers at the University of California, Berkeley, in their research to understand causes of major failures, identified certain organizations that were better at handling and avoiding these failures. [1,2] In their work, they defined a high reliability organization (HRO) as "an organization that has succeeded in avoiding catastrophes in an environment where normal accidents can be expected due to risk factors and complexity." They further defined the five principles that HROs have in common:

- Preoccupation with failure
- Reluctance to simplify
- Sensitivity to operations
- Commitment to resilience
- Deference to expertise

These principles have been adopted across many complex industries, including aerospace, defense, nuclear power, air traffic control, automotive controls, and healthcare, in which the major failures can have catastrophic and/or life-threatening consequences. Karl Weich and Kathleen Sutcliffe have studied several of these industries and how they adopt principles of high reliability. [3,4,5,6]

HOW DOES THIS APPLY TO ELECTRONICS MANUFACTURING?

With the ubiquitous use of electronics to perform demanding and critical functions within the above-mentioned industries, high reliability is an ongoing concern. Moreover, with the growing complexity of systems used throughout our environment, coupled with the increased complexity and miniaturization of devices, the concept of high reliability is becoming more and more commonplace in the electronics manufacturing industry, in general. In fact, the IPC standard for electronics assemblies, IPC-A-610, includes the following three classes for assemblies, with the most stringent being defined as High-Reliability Electronics Products: [7]

- Class 1 Electronics: General Electronics Products
- Class 2 Electronics: Dedicated Service Electronics Products
- Class 3 Electronics: High-Reliability Electronics Products

HOW DOES THIS APPLY TO STATIC CONTROL OF THE MANUFACTURING ENVIRONMENT?

In general, ANSI/ESDA S20.20 provides a framework for establishing a static control program for operations:

> *"…that manufacture, process, assemble, install, package, label, service, test, inspect, transport, or otherwise handle electrical or electronic parts, assemblies, and equipment susceptible to damage by electrostatic discharges greater than or equal to 100 volts HBM, 200 volts CDM, and 35 volts on isolated conductors."* [8]

Within the ANSI/ESD S20.20 framework, flooring is primarily used as a means to ground personnel and mobile equipment. For personnel, it is intended to keep

the voltage on personnel to below 100 volts and thereby ensure that any potential discharge from a person to a sensitive device falls below the limit of 100 volts HBM. To meet this objective, ANSI/ESD S20.20 set standards for flooring as follows:

- The complete system must have a resistance (point-to-point and point to ground) of less than 1.0 x 10^9 ohms as tested per ANSI/ESD STM7.1; [9]
- The complete system of person-flooring-footwear must have a resistance to ground of less than 1.0 x 10^9 ohms as tested per ANSI/ESD STM97.1; [10] and
- The complete system of person-flooring-footwear must generate less than 100 volts as tested per ANSI/ESD STM97.2. [11]

So, ANSI/ESD S20.20 is designed to control to 100 volts HBM. But what if the devices handled are more sensitive, that is, have a lower withstand threshold? For those situations, the standard simply states:

> *"Activities that handle items that are susceptible to lower withstand voltages may require additional control elements or adjusted limits."*

Or, what if there is a desire to limit HBM to below 100 volts simply to increase the margin of error for preventing a failure? Or, what if there is a desire to increase the reliability of a static control program beyond what an ANSI/ESD S20.20 program would provide?

ANSI/ESD S20.20 is viewed as providing a minimum set of standards that meet a vast majority of the needs in factory-level ESD controls. End users, trained in ESD controls, can expand upon the ANSI/ESD S20.20 controls to create more stringent requirements for their particular applications and many HROs do just that.

HOW DOES THE ESDA VIEW HIGH RELIABILITY?

The issue of high reliability has become so prevalent within the ESD community that the Electrostatic Discharge Association (ESDA) has formed Working Group (WG) 19 – High Reliability to develop a guidance document to help users that may need or want to implement more stringent controls than those prescribed in ANSI/ESD S20.20. This work will include recommendations for nearly every aspect of ANSI/ESD S20.20.

Members of this working group are involved with some of the most stringent ESD control programs in the world and bring to this project their vast knowledge of ESD controls. While the work is not yet published, the working group meetings are open to guests. If you are interested in learning more about this work, go to http://www.esda.org/events for a schedule of upcoming working group meetings.

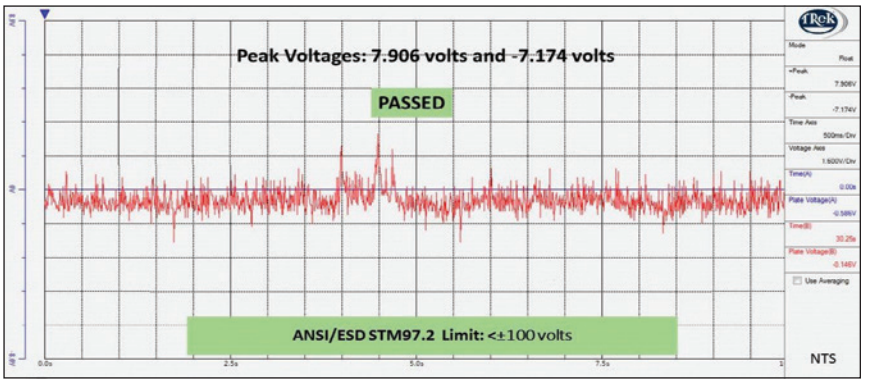


Figure 1: Walking voltage generated on a conductive floor

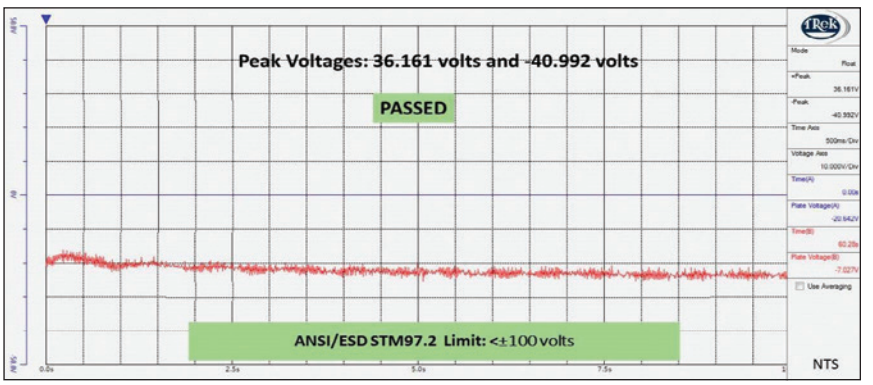


Figure 2: Walking voltage generated on a dissipative floor

CONDUCTIVE VS DISSIPATIVE FLOORING – MOST HROS CHOOSE CONDUCTIVE

With regard to static control flooring, the industry has historically used two "grades" of flooring, conductive and dissipative. These terms are defined in ANSI/ESD STM7.1 as:

- Conductive flooring system – has a resistance to ground of less than 1.0×10^6 ohms
- Dissipative flooring system – has a resistance to ground of greater than or equal to 1.0×10^6 ohms to less than 1.0×10^9 ohms

But the electronics industry is moving away from classifying flooring by grade. As noted above, ANSI/ESD S20.20 simply requires that flooring have a resistance of $<1.0 \times 10^9$ ohms, so either of these "grades" will meet the requirement as long as they also meet the requirement for the walking voltage test when tested in combination with the footwear to be worn in the area.

While the flooring/footwear combination is extremely important in determining the body voltage generation, all else being equal, the lower the resistance of the flooring, the lower the body voltage.

Figures 1 and 2 show the test results of body voltage generated for two flooring systems. In these tests, the flooring systems were nearly identical, with the first being formulated to have a resistance in the conductive range and the second having a resistance in the dissipative range. The footwear and the person conducting the test were the same in both cases.

As you can see, while both systems passed the requirement of ANSI/ESD S20.20, the conductive floor generated significantly lower body voltage, which

could be important in a very sensitive environment and would certainly reduce the risk of a potential failure due to an ESD event.

Also, as a floor gets dirty or ages, resistance levels may increase, potentially rendering the flooring-footwear system ineffective at achieving the desired level of protection. For these reasons, most of our HRO customers choose flooring that has a resistance of less than 1.0×10^6 ohms. This provides an added measure of security that the floor will still perform when dirty and that body voltages will be kept as low as possible in the area.

FOOTWEAR

As previously noted, the ultimate test of protection and the resulting risk reduction is the amount of voltage that a person generates when walking on the floor and that this is affected by the combination of both the footwear and the flooring. There are a number of types of footwear available in the market, including:

- Heel grounders
- Sole grounders
- Conductive shoes
- Conductive booties

As mentioned, you must test the footwear that you intend to use with the floor you intend to use to ensure that you get the body voltage results that you require. The combination matters. I've personally seen a situation with a floor that tested consistently with a resistance in the 1.0×10^5 ohms range, but the walking voltage test performed with the shoes actually used in that facility resulted in body voltage spikes greater than 100 volts. Fortunately, this was discovered in the planning stages and different flooring was chosen that worked extremely well with the footwear used.

One other thing to consider with regard to footwear is the contact that it has with the floor. Heel grounds offer the least, while conductive shoes and conductive booties have the most. The better the contact with the floor, the less likely someone will become electrically disconnected from the floor as they move across it.

UNDERSTAND THAT STATIC CONTROL FLOORING IS A SYSTEM

For any flooring system used in an ESD control program, it is important to understand the nature of the flooring system, the components it uses, and how they interact. So, for example, a conductive vinyl flooring system that is glued down includes the conductive vinyl tile, the glue, the substrate it is adhered to, and the grounding mechanism. Many of the epoxy/resinous coating systems used include a primer layer, a highly conductive ground layer, and a more decorative finish coat.

There have been many situations where one component in the system develops a resistance higher than desired, thereby causing the whole system to be out of compliance. In a high reliability environment, when choosing a flooring system, it would be prudent to understand all of these components and the risks associated with a potential failure in order to reduce the likelihood of a future non-compliance situation.

REDUNDANCY WITH FLOORING

In any quality system, adding redundancy reduces the probability of failure. In many high reliability applications, users will control static using wrist straps, ionization, equipment grounding, and packaging, to the point where flooring may not really be necessary. The floor provides a secondary means of grounding and protection in these environments and helps to ensure charges are kept to a minimum. Moreover, many HROs will increase the areas of coverage to include more ancillary areas to help ensure that any movements of devices are within an area with static protective flooring.

COMPLIANCE VERIFICATION OF FLOORING

ESD TR53 [12] provides compliance verification procedures for ongoing verification of control items used in an ANSI/ESD S20.20 control program. For flooring, some things to take into consideration for ongoing compliance verification include:

- **The periodicity of testing:** This is not prescribed in either ANSI/ESD S20.20 or TR53.The periodicity of testing should be regular enough to head off non-compliance, as determined by:
  - *Use and maintenance:* If the floor is subjected to a lot of traffic and dirt, it may need to be checked

more regularly. Likewise, the regularity and extent of floor cleaning will impact how often the floor should be checked.

- *Life of electrical properties:* Some flooring systems have lifetime electrical properties, while others, such as applied finishes, only last a few months.
- *Any changes:* The floor should be checked if there are any changes in use or maintenance practices and materials. Any of these could impact the performance of the floor.
- *Past results:* By monitoring results over time, you can get a sense of if or how the floor is changing over time and adjustments can be made to periodicity as appropriate.

- **Incorporating regular walking body voltage tests:** The procedure in ESD TR53 for verifying flooring is a simple check of resistance to ground. As noted previously, the body voltage generation is a critical measurement of the effectiveness of a flooring-footwear system. As such, walking body voltage measurements should be taken periodically following the procedure of ANSI/ESD STM97.2. Doing so will help ensure that that flooring system and the flooring-footwear combination is still providing the desired static control.

CONCLUSION

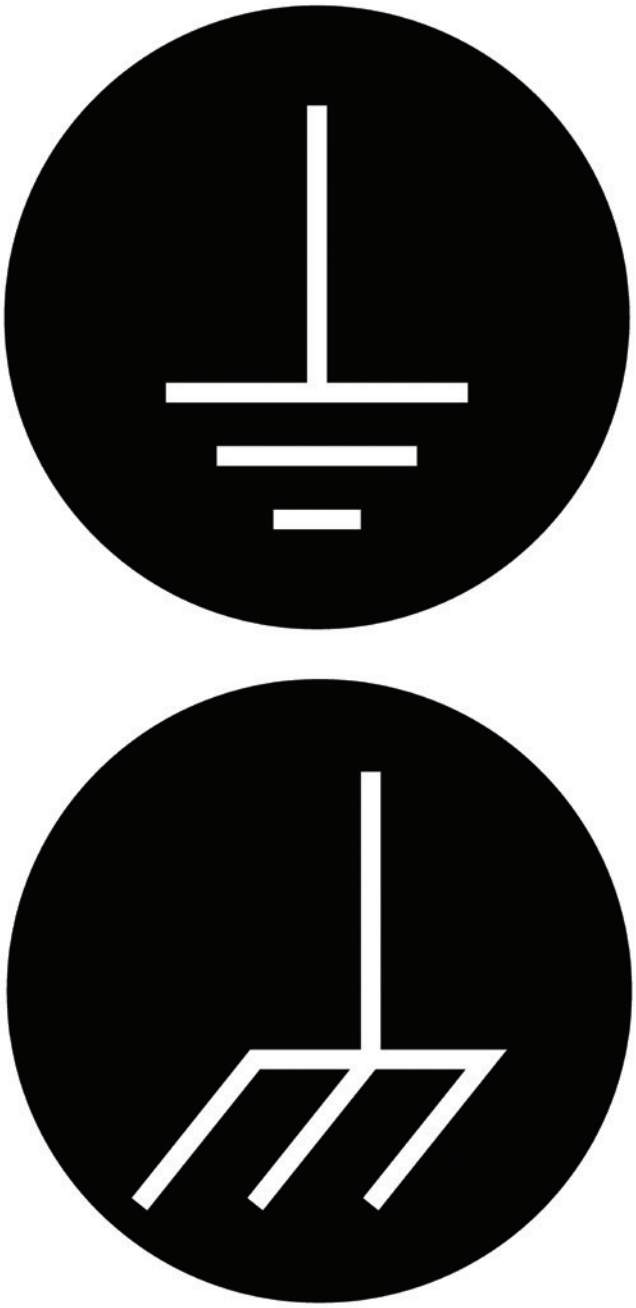
While ANSI/ESD S20.20 provides a very strong framework for establishing an ESD control program, it does recognize that some organizations may need to enhance their program to meet their particular needs. HROs fall into this latter category and often will take added steps in their ESD control programs to reduce any potential risk of an ESD event leading to a failure. There are several things that an HRO can consider with regards to their static protective flooring system, including the resistance of the system, the footwear used in conjunction with that system, the extent of area covered, and the ongoing verification of the system.

ENDNOTES

1. Rochlin, Gene I., (1996-06-01), "Reliable Organizations: Present Research and Future Directions," *Journal of Contingencies and Crisis Management*, 4 (2): 55–59. doi:10.1111/j.1468-5973.1996.tb00077.x. ISSN 1468-5973.
2. Roberts, K.H., (1989), "New Challenges in Organizational Research: High Reliability Organizations," *Organization & Environment*, 3 (2): 111–125. doi:10.1177/108602668900300202.
3. Weick, K. E., Sutcliffe, K. M., and Obstfeld, D., (1999), "Organizing for High Reliability: Processes of Collective Mindfulness," In B. M. Staw & L. L. Cummings (Eds.), *Research in Organizational Behavior* (Vol. 21, pp. 81-123). Greenwich, CT: JAI Press, Inc.
4. Weick, K. E., and Sutcliffe, K. M., (2001), *Managing the Unexpected: Assuring High Performance in an Age of Complexity*, First Edition, San Francisco: Jossey-Bass.
5. Weick, K. E., and Sutcliffe, K. M., (2007), *Managing the Unexpected: Resilient Performance in and Age of Uncertainty*, Second Edition, San Francisco, CA: Jossey-Bass.
6. Weick, Karl E., Kathleen M. Sutcliffe, 2001, *Managing the Unexpected - Assuring High Performance in an Age of Complexity*, San Francisco, CA, USA: Jossey-Bass. pp. 10–17. ISBN 978-0-7879-5627-1.
7. IPC International, "IPC-A-610H: Acceptability of Electronics Assemblies," 3000 Lakeside Drive, 105N, Bannockburn, IL 60015.
8. Electrostatic Discharge Association, "For the Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)," 7900 Turin Road, Bldg. 3, Rome, NY 13440.
9. ANSI/ESD STM7.1, EOS/ESD Association, Inc. "Flooring Systems Resistive Characterization."
10. ANSI/ESD STM97.1, "Floor Materials and Footwear-Resistance Measurement in Combination with a Person STM97.1."
11. ANSI/ESD STM97.2, EOS/ESD Association, Inc. "Floor Materials and Footwear – Voltage Measurement in Combination with a Person."
12. ESD TR53, EOS/ESD Association, Inc., "Compliance Verification of ESD Protective Equipment and Materials."

SYSTEM-LEVEL GROUNDING

Is Your System Well Grounded? Consider These Points in Effective Grounding



Grounding is the most fundamental property of all types of electrical equipment. There are plenty of quality articles on specific subjects in *In Compliance Magazine* and in other publications, largely on grounding on a printed circuit board (PCB) level. This article focuses on a path less traveled, grounding on a system level, that is grounding of the equipment in actual use at the factories.

There are several key aspects of grounding, including safety, ESD, EMI, and signal integrity. While this and other magazines have published detailed articles on one or more of these subjects, this article combines them all to assist equipment users and tool makers in understanding what is important and how to achieve optimal ground performance. This article does not cover PCB grounding (there are plenty of excellent articles on this subject) and portable tools with double insulation that do not have grounding.

SAFETY

Safety is always first. Too many specialists in electrostatic discharge (ESD) and electromagnetic interference (EMI) are not professionally trained in electrical safety. This article is far from a comprehensive safety guide, and it doesn't cover every important safety point. The whole purpose of this section is to bring electrical safety

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By Vladimir Kraz

to the attention of ESD and EMI specialists at factories and tool designers who otherwise may not be aware that grounding is a safety item. I strongly recommend that those who deal with such subjects take an electrical safety course, make friends with factory's licensed electricians, or join a factory safety committee. In this article, we will just scratch the surface and touch on the basics.

So why is grounding a safety element? As an example, let us consider a typical piece of industrial equipment, such as an integrated circuit (IC) handler, or surface mounted technology (SMT) pick-and-place machine (or any other tool that you are familiar with). Each of these tools takes its power from AC mains, meaning that typically anywhere from 100VAC to 440VAC enters the equipment. If a live wire inside such a machine or tool gets loose for whatever reason, it can touch and energize (that is, supply voltage to) a metal part to which an operator has access. Now this metal part, such as the enclosure, is under high voltage. The operator can easily be electrocuted simply by touching such a part.

Here is where grounding comes to the rescue. If all operator-accessible metal parts are properly grounded, an energized loose wire that touches such a part effectively short-circuits any live voltages to ground, and the resulting excessive current triggers the circuit breaker to cut power to the tool. For all this to work, these conditions must be met:

- All operator-accessible conductors must be grounded;[1] and
- The ground path must have a low enough impedance to allow a high current sufficient to trigger the circuit breaker.

1. Due to its construction, some equipment may have electrically floating metal parts, i.e., not electrically connected to anything. These parts are generally small. Special care must be exercised to assure that such floating pieces of metal physically cannot have electrical contact with live voltage.

How conductive should a ground path be in order to trigger the circuit breaker? There are several varying standards and guidelines on this subject, but the essential answer is that the ground path should be at least as conductive as either the live or neutral paths. If your power cable utilizes AWG12 (or 2mm diameter) power wires, you cannot have ground wires that are thinner than that. A ubiquitous AWG18 green wire just won't do.

Must all grounding wires inside the tool be as thick as the power wires that enter it? Not necessarily. In places where grounding is done for purposes other than safety (for example, ESD/EMI) and where there are no voltage-carrying conductors, grounding wires can be selected based on other criteria (see further on in this article).

Ground and Neutral Reversal

More often than desired, ground and neutral wires are reversed in either facility wiring or in the internal wiring of the equipment itself. This leads to return current flowing through ground rather than through the neutral wire, resulting in a multitude of functional problems in addition to being a safety issue. A ubiquitous three-LED outlet checker cannot detect that. The easiest way to check for it is to measure AC current on the ground wire entering the equipment using a simple AC current clamp (make sure to properly identify ground wire). If the equipment ground current exceeds 0.1 A during operation, an investigation is in order. This does not account for excessive leakage current in equipment even if the wiring is correct.

ESD

After safety, the second most common use of grounding in equipment is to address ESD considerations, more specifically, to provide a discharge path to ground for conductors and static-dissipative

materials. If accumulated static charges on electrically "floating" conductors and dissipative materials are not discharged to ground potential, they may carry unwanted voltage and cause problems for ESD-sensitive devices.

How do we effectively ground such objects? Standards such as ANSI/ESD S6.1[1] and an "omnibus" standard ANSI/ESD S20.20 [2] provide good recommendations. Here we will add some helpful narrative.

It is curious to me that engineers and technicians dealing with grounding issues don't ask the most important and logical question about ground, that is, what is the voltage on ground? Not the resistance since resistance is just the means of reducing the voltage on grounded parts. The whole purpose of grounding for ESD purposes is to create an equipotential environment.

There are currently no coherent standards, standard practices, or technical reports issued by either the ESD Association or the IEC that touch this subject with any specifics on validation. Yet, this is the most important question for the safety of the devices in the process. The only document addressing it is SEMI Standard SEMI E.176 [3] which I'll cover later in this article.

How do we assure that what needs to be grounded actually is? There are implicit and explicit ways of providing grounding connections. Implicit ways include mechanical fastening of conductive parts of the tool to the grounded frame so that there are no obvious grounding wires, but the electrical connection via mechanical fastening is still present and is adequate. The problem with such implicit connections is that they are uncontrolled. Depending on the construction of the tool, any component in the electrical connection chain can be altered in the next revision of the tool or during repair or service and modified to the degree where the electrical connection is no longer assured. During any revision, maintenance, or repair, a metal washer can be replaced by a nylon one, or an originally bare metal part may become anodized, and so on.

There are two ways to prevent such problems. One way is to add requirements for adequate ground connection to the tool's specification and to the maintenance

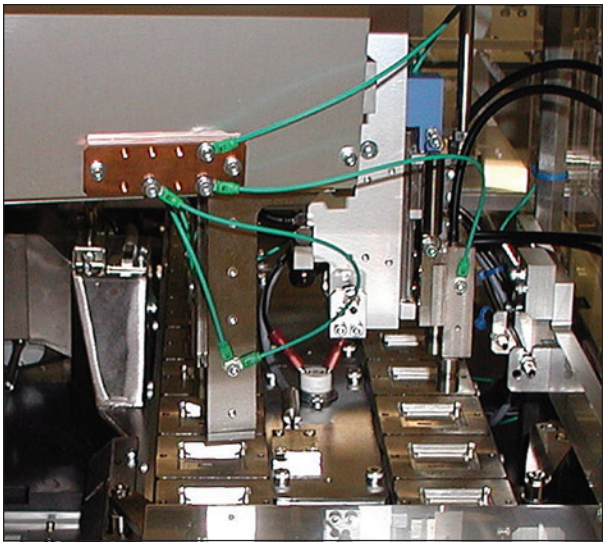

Figure 1: "Explicit" grounding in the IC handler

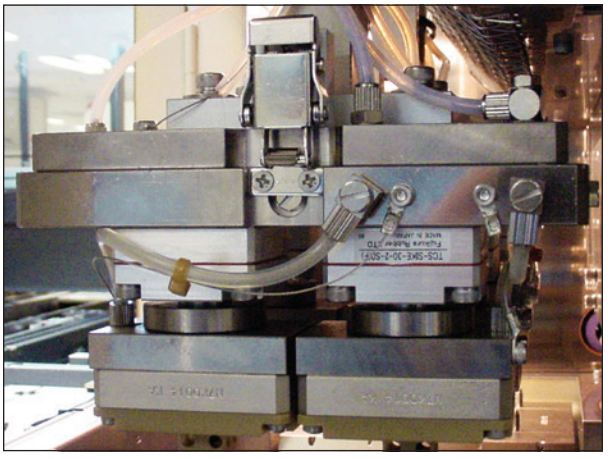

Figure 2: Grounding of moving parts using flexible steel cable

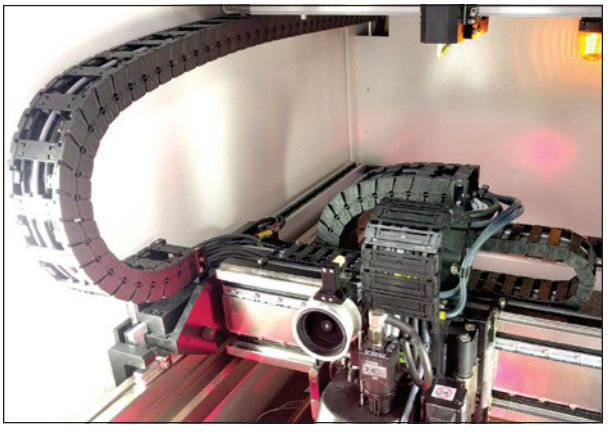

Figure 3: Flex cables on a robotic arm

procedure and verification documentation (and to meticulously follow it). Another way is to use an explicit, separate grounding method. Either of these methods is viable, and the choice is up to the user of the equipment since its manufacturer may not appreciate the importance of proper grounding for ESD.

An example of explicit grounding is shown in Figure 1. I'll come back to this figure later in this article.

ESD GROUND: HOW GOOD IS "GOOD"?

Various ESD-related standards such as ANSI 6.1, ANSI/ESD S20.20, ESD S10.1 [4], IEC 61340 [5], and some other documents, plus proprietary factory-wide documents, provide guidance on grounding. This section simply attempts to provide clarification on some of the details.

Metal Ground

For "explicit" grounding and for the grounding of floating metal parts, these documents specify (or recommend) a resistance path to ground of less than 1 Ohm. While this goal is reasonably easy to achieve with stationary equipment, it can be quite elusive and not feasible for some of the moving parts.

If the part moves just a little (even just a few centimeters, as is common in many tools) grounding is often done using flexible steel cable (quite similar to a bicycle brake cable, see Figure 2). Careful selection of material, flex radius, and the number of bend cycles of such cables is required to avoid breakage of the cable in use. Obviously, steel is not as good a conductor as copper, but it is much more durable. And, with very short cable runs, resistivity isn't really an issue.

Longer movements require much longer runs of ultra-flexible cables protected by flex conduits, as shown in Figure 3. The internal construction of such flex cables does not support a sufficiently thick gauge of wire. Therefore, many ultra-flexible cables include an additional layer of Teflon or similar material around each wire that facilitates a low friction coefficient, allowing wires to slide against each other while bending.

This would be the case with any ultra-flex cables, with or without an external harness, as shown in Figure 2. The result is higher resistivity of such wires, making

a 1 Ohm requirement of the entire connection almost unachievable, considering all the interconnects along the chain. Requirements to the total resistance of flex ground connections typically vary between 2 and 10 Ohms, depending on the factory, although I've seen 20 Ohms requirements as well. Would such an increase over 1 Ohm noticeably alter the ESD environment in the process? Actually, that's very unlikely, but what would cause the problem is a loss of ground connection.

The problem with the reliability of explicit grounding using dedicated conductors is that the failure of a ground connection may not be obvious right away. After all, such grounding or the absence of it does not alter the basic functionality of the tool and can go unnoticed for some time. I've witnessed an unfortunately large number of situations where "explicit" ground wires were disconnected for tool's maintenance but, instead of being reconnected, the wires were either completely removed or their ends were left "hanging," making the tool look a bit like a hedgehog. And these issues typically emerge when there's a need to resolve a "sudden" ESD or EMI problem.

One of the solutions to a lost ground problem is ground monitoring, and there are plenty of ground monitors on the market. Such monitors independently connect to the grounded point and to the reference ground and sound an alarm whenever a ground connection fails.

The 1 MOhm Question

Wriststraps and/or wriststrap cords contain a 1 MOhm resistor in line with ground for a simple reason, that is, to prevent electrocution of personnel. Should an operator wearing a wriststrap accidentally touch a grounded conductor, the current through the operator should not exceed 0.5mA (ANSI/ESD S1.1 ANNEX B [7]), a limit that is consistent with several broader safety standards. At 250V RMS, which is the highest RMS AC voltage among common electrical outlets, the minimum resistance should be no less than 500 kOhms (not accounting for the electrical resistance of the operator's body). A 1M resistor would satisfy this requirement, including dual wriststraps that would have two resistors, electrically parallel to each other, between the operator's body and ground. Try to avoid low-cost wrist straps and cords unless their resistance is verified.

Should the same 1 MOhm resistor be used to ground other items, such as metal objects or dissipative materials? The often-stated reason for use of a 1 MOhm resistor in such applications is "to slow down the discharge." Would it truly "slow down" the discharge?

Let us consider an electrically floating metal object that needs to be grounded. This object would have an electrical capacitance dependent on its size (among other things). Assuming that this object is at ground potential, would it make a big difference in discharge properties whether the object is grounded via sub-Ohm resistance, via 1 M resistance, or left electrically floating?

Figure 4 shows a highly simplified equivalent electrical schematic of such a connection (parasitic inductances and capacitances have been omitted for clarity). A device (IC) has a certain capacitance, C1, and is charged, to voltage V1, likely as a result of being lifted from the tray. An IC handler's arm is about to place this device onto a shuttle (a metal tray for moving ICs in the handler). When the IC comes in contact with the shuttle, the voltage is almost instantly equalized.

For exercise purposes, we will assume that the shuttle is implicitly grounded via resistor Rg and not by mechanical means. In the end, whatever charges were left on the shuttle will dissipate to ground via Rg. But the issue we are trying to resolve is the role that the Rg plays in the properties of the discharge itself.

Resistance Rc of contact between the IC and the shuttle is negligible, perhaps just a few milliohms. If we set Rg to 1 MOhm, most of the action will happen between the IC and the shuttle, since Rg is too large to participate in voltage equalization during a short nanosecond-long discharge. If we bring this

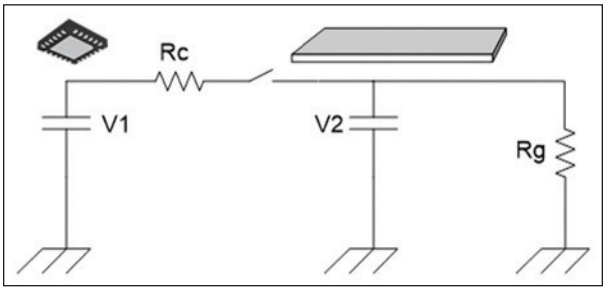

Figure 4: Discharge equivalent schematic

situation to an extreme, assuming that Rg has infinite resistance, would this "slow down" the discharge? Of course not, since the waveform of the discharge is defined only by the capacitances of metal parts and contact resistance Rc. ESD practitioners know well that touching a floating plate of CPM easily produces discharge, just like touching a completely insulated metal doorknob would produce the same. The only function of Rg is to eventually dissipate whatever little charge the IC shared with the shuttle to ground and to bring shuttle voltage to ground potential.

The same holds true for static-dissipative mats. Inserting a 1 MOhm resistor into the ground connection will not change the rise time or amplitude of the discharge. Instead, it will only slow down the dissipation of charge to ground which, in the case of static-dissipative materials, may leave these materials under voltage in fast-paced processes. While existing practices allow a 1 MOhm resistor to be used in a ground circuit with dissipative materials, it is counterproductive in reality.

EMI

We are finally coming to the most interesting part of grounding, that is, high-frequency voltages on ground, or EMI. The term in this context may not satisfy a purist but, since it is widely used in the industry, this is what we will be using as well.

Every electrical equipment generates some sort of parasitic, for example, unplanned or unwanted signals. Automated equipment contains plenty of sources of high-frequency voltage and current signals [8], with the strongest generated by pulse-driven motors (servo, steppers, and VFD – variable frequency drives) [9], and switched-mode power supplies, including those in LED lighting as well. These high-frequency signals "leak" to ground via parasitic capacitance, resulting in highly undesirable voltages between different grounded parts of equipment. This is never good news, but it's especially bad news for sensitive devices and for testing and measurement.

Why are we focusing on high-frequency voltages and not any other voltages? Simply, conventional grounding methods deal with DC and low-frequency AC voltages reasonably well. They sink to ground any leakage AC and static DC voltages that happen to be on metal and static dissipative parts of equipment, given their low ground path resistance (see the previous discussion). That leaves only high-frequency voltage signals, due to the parasitic inductance and capacitance of conductors and the mutual influence between them. While resistance path to ground can be very low for DC and for low frequencies, this is not the case for high-frequency signals, which we'll analyze it in detail.

A Wire is an Inductor

Simple, straight wire that would be great for ESD and safety grounding is, in fact, an inductor. Although calculating this inductance may be a bit involved, there are plenty of useful Java-based inductance calculators on the internet that are far more practical [10] than doing the calculation by hand.

As a point of reference, a 1mm diameter wire (AWG18) of 1 m length has an inductance of 1.5μH. At 1MHz this would present an impedance of 9.42 Ohms. This is for the straight wire only, and the typical service loops of ground wire only add to impedance. There are calculators for that too [11]. As an example, five turns of the same wire coiled in a 6" (15cm) diameter coil produces 6.1μH inductance with an impedance of 38 Ohms at 1MHz. The same wire would have a resistance of only 0.06 Ohms at DC.

Only Outer Layer of Wire is a Conductor at High Frequency

At high frequencies, the current is "pushed out" by the magnetic field resulting from the passing current, the so-called skin effect. The higher the frequency, the thinner the conductive layer. At 1 MHz, the outside conductive layer is only 66μm thick. Skin effect doesn't add as much resistance as pure inductance (1m of AWG18 wire constitutes 0.09 Ohms vs. 0.021 Ohms Ohms if there were no skin effect), but it all adds up. Multi-stranded wires help, since the bigger the wire surface the lower the resistance. But the wires typically found in manufacturing environments have too few strands to be effective.

Capacitive Coupling

Two wires running in the same conduit influence each other via capacitive and inductive coupling. In Figure 2, there are drive signals among the wires in the flex channel to servo motors on the robotic arm, along with a wire to ground the arm itself, all of which

are in immediate proximity to each other. A typical robotic arm of automated equipment has three servo motors, one for each degree of freedom. This amounts to nine wires carrying pulsed voltage with typically 200V peak voltage (not counting ringing and other artifacts). The rise and fall times of such drive pulses are under 50 nS, creating signals with the spectrum extending up to 20 MHz.

In the example of Figure 2, the length of wires in the flexible harness is 3m. The capacitance between two adjacent wires would be approximately 63pF [12] which at 20MHz constitutes 125 Ohms impedance. The rough equivalent schematic would look like the one in Figure 5a.

Due to the properties of capacitive coupling, the higher the frequency, the higher the induced voltage. Correspondingly, the sharper the edges of the pulses, the higher the induced voltage.

Inductive Coupling

The long wires running in parallel form a distributed transformer. Without the core and the turns of windings, it works only at higher frequencies, and this is where the problem lies. Figure 5b shows how the current in one wire imposes corresponding currents on a nearby wire. Due to the properties of this parasitic transformer, only high-frequency signals are being passed from one wire to another, creating waveforms similar to those shown in Figure 5a.

Field Data

One can get easily absorbed in simulations and calculations of induced voltages and currents. In our case, however, is not likely to produce realistic results due to the number of variables not accounted for in the equivalent schematic, and the variability of parameters between the tools. But measurements serve a much more practical purpose. Measurement methodology and techniques are described in detail in this article [13], previously published in *In Compliance*.

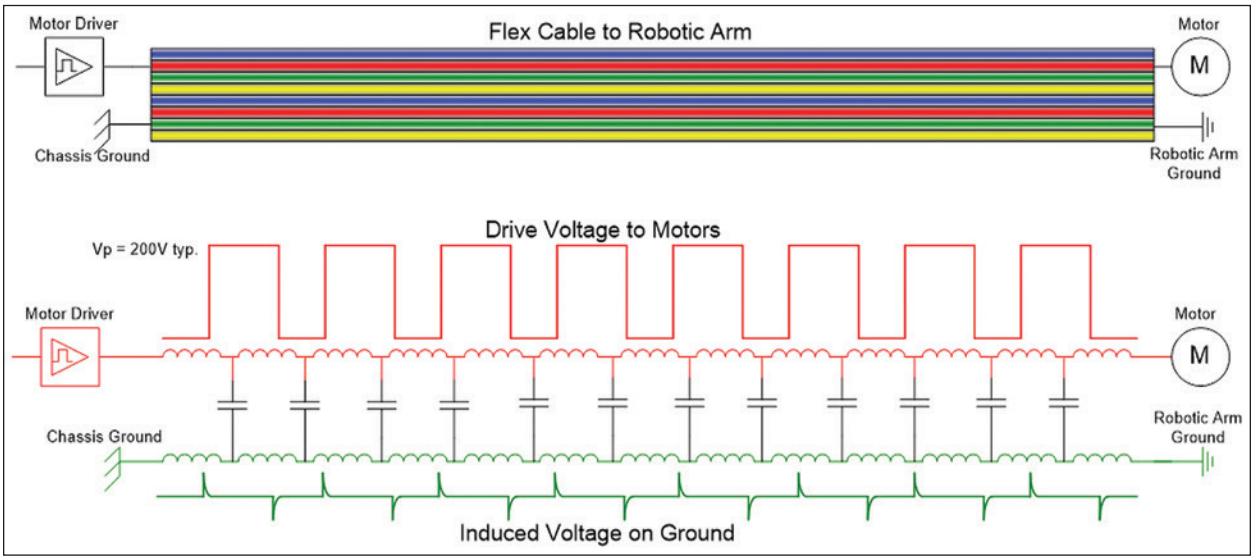

Figure 5a: Induction of high-frequency voltages into group wire in a flex conduit of Figure 2

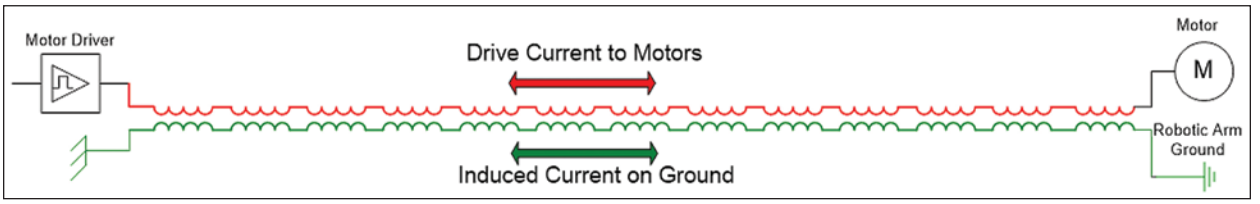

Figure 5b: Induced current on ground

Figure 6 shows typical voltage between the nozzle of the robotic arm in the IC handler and the chassis. The spikes correspond to the rise and fall edges of the interfering signal.

Figure 7 depicts the current between the robotic arm and the chassis in a different tool. The current was measured using Tektronix's CT1 probe with 5mV/mA ratio, and the peak current is 76.8mA. Ringing is simply an artifact of imbalanced impedance match, and manufacturing equipment is a far cry from fully matched RF instruments.

What Harm Can Little Ground Voltage Do?

What could be wrong with a little voltage between different grounded parts? In many tools and processes, it's not a problem. If your devices are not sensitive to electrical overstress (EOS), and if you are not concerned with data integrity and measurement accuracy, there is not much to worry about. However, since you are reading this article, you must have some interest in keeping voltages and currents on ground as low as possible.

Electrical Overstress (EOS)/Electrically Induced Physical Damage (EIPD)

Grounded surfaces are supposed to provide a "safe space" for sensitive components without the possibility of any overvoltage exposure. But if we actually conduct measurements, the situation can be quite different and often "unsafe."

Consider, for example, the common handling of ICs in an IC handler or SMT pick-and-place machine (Figure 8). An actuator/nozzle at the end of the robotic arm has plenty of high-frequency voltage vs. the chassis that we described above. A silicon die of the IC is capacitively coupled to the nozzle in its immediate proximity. At high frequencies, this capacitive coupling presents a very low impedance. When this IC is placed on either a test socket or on a shuttle (a metal holder for moving ICs in the horizontal plane), excessive current may flow through the device, weakening its structure and causing failures in the field, or even resulting in an outright failure.

This is just one example. Any metal contact with the device, such as soldering [14], wire bonding [15], or others can expose the devices to unwanted voltages and currents.

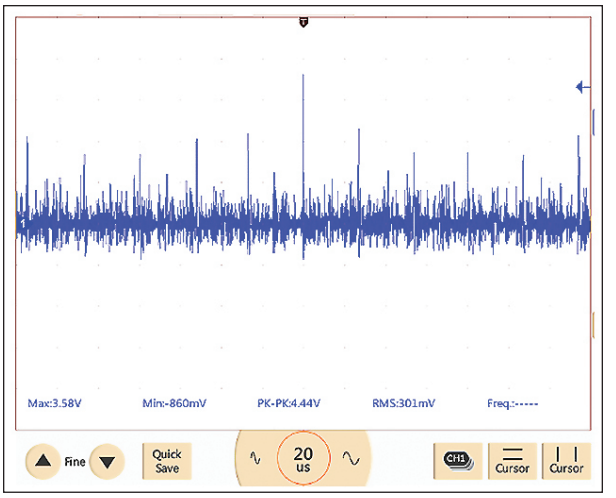

Figure 6: Voltage between the nozzle of the robotic arm in IC handler and the chassis

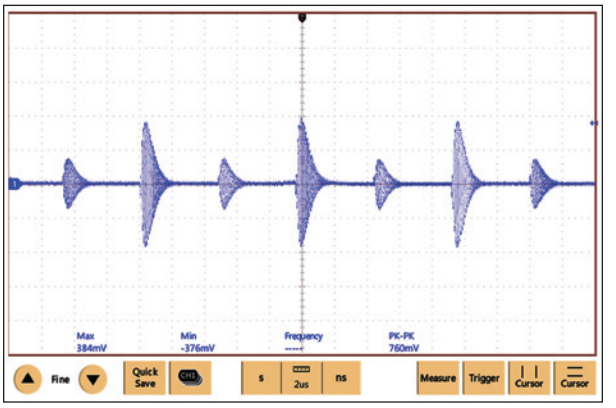

Figure 7: Current between the robotic arm and the chassis

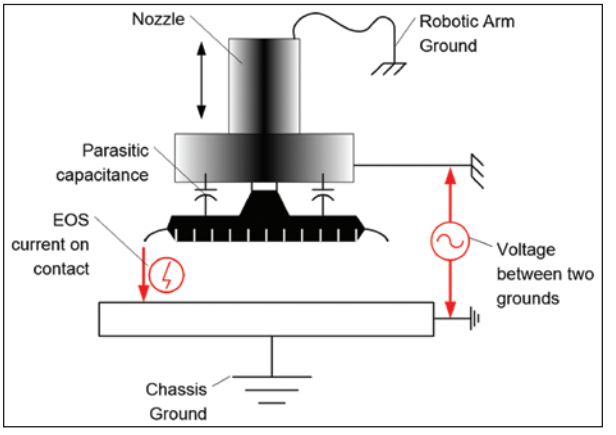

Figure 8: Mechanism of EOS in automated handling of ICs

How Much Ground Voltage and Current Are Too Much?

There are plenty of documents about controlling the resistance/impedance of ground connections. But SEMI Standard E.176 "Guide to Assess and Minimize Electromagnetic Interference (EMI) in a Semiconductor Manufacturing Environment" is the only relevant industry document that actually specifies the maximum allowed EMI voltages and currents on ground based on the properties of devices used in the process.

While written largely for semiconductor manufacturing, SEMI E.176 has a direct bearing on all applications of semiconductors, which includes most of today's equipment. After all, the sensitivity of semiconductor devices doesn't change once it has been shipped to a PCB assembly plant. I've written several articles published in previous issues of *In Compliance* [16] [17] that discuss SEMI E.176 in detail.

As one point of reference, today's common IC with 10nm geometry in its unpowered state (i.e., in IC manufacturing and handling, such as PCB and product assembly) should typically not be subject to voltages higher than 0.1V across it, and the peak ground currents for this geometry should not exceed 10mA (Level 3 in SEMI E.176).

Unless you can measure and quantify ground voltages and current, you cannot control it. Another of my articles previously published in *In Compliance* [13] provides detailed guidance on the methodology, instrumentation, and techniques for such measurements, and I encourage you to read it before performing any measurements.

EMI: EFFECT ON DATA

High-frequency signals can interfere with data and measurements in several ways. Induced EMI voltage can present itself as a valid signal since it can be close in amplitude and in waveform to the real signal. This leads to data corruption [18] and measurement errors [19],[6]

Ground Bounce on a System Level

Electrical engineers are familiar with "ground bounce" effect in semiconductors (see, for example, [20]). Ground bounce is mostly thought of as happening on the IC level, but the physics of ground bounce work on a system level as well. Figures 9 and 10 show an example of how it happens.

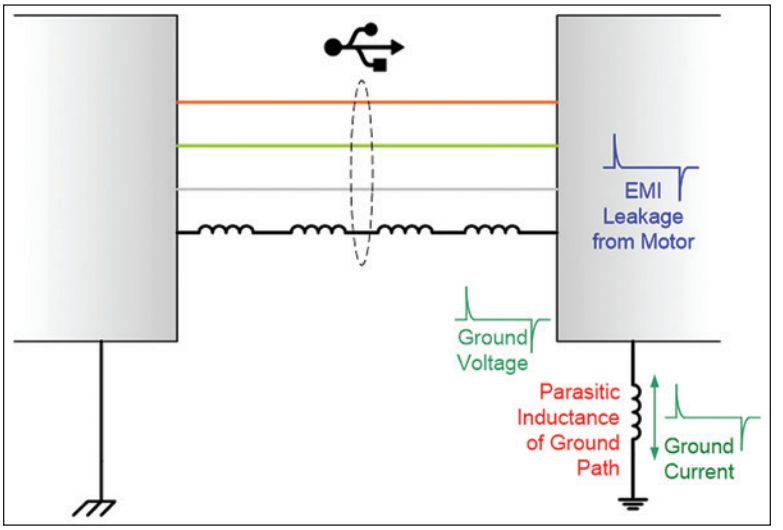

Figure 9: Ground bounce on a system level

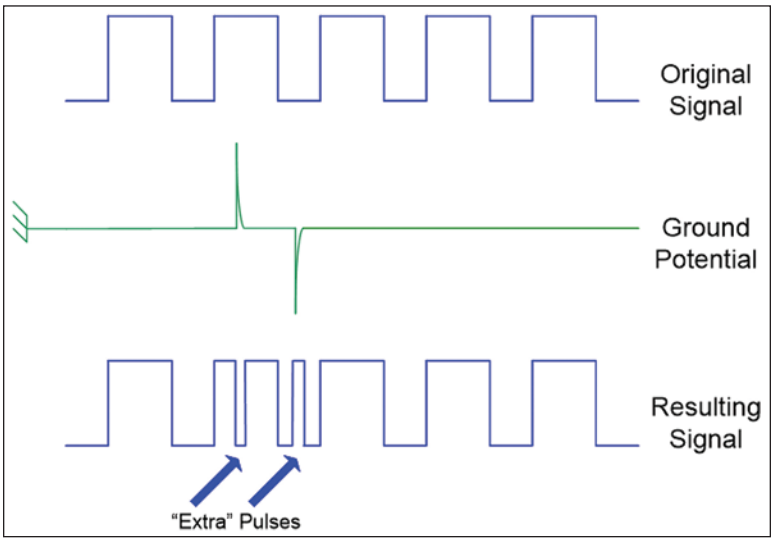

Figure 10: Ground bounce causes "extra pulse"

Figure 9 shows how current spikes from sources such as motor operation travel to the facility ground and thus create a voltage drop on the tool's ground wiring. The resulting voltage on the tool's ground is no longer the same as the facility ground, and not the same as the ground of another tool with which the tool is trying to communicate (in this example, the USB). In such conditions, logic levels are no longer valid as shown in Figure 10, and the very next logic gate can easily mistake "1" for "0" and vice versa, depending on the timing and the amplitude of such interference. The worst part of it is that there is no record in the system of such occurrence, and reproducing it is often impossible.

I HAVE EMI ON GROUND - NOW WHAT?

Simply understanding the problem is only the first step in resolving it. There are several methodologies to mitigate EMI issues on ground. All revolve around the same three basic principles:

- Reduce EMI at the source;
- Block propagation of EMI; and
- Reduce susceptibility of your circuit/devices to EMI

Depending on whether you are an equipment designer or an equipment user, your options may vary.

Reducing EMI at the Source

The two biggest sources of EMI in equipment are pulse width modulation (PWM) motors (e.g., servo, stepper, and VFD), and switched-mode power supplies. If we manage to decrease dV/dt of the edges of their pulses (in other words, "slow down" the signal transitions), there will be less EMI to induce on ground. Designers of PWM drives and SMPS are trying to make these edges as sharp as possible so that the output transistor drivers do not heat up as much and the circuit is simpler. Typical rise/fall times of drive pulses in a servo motor are around 50nS, which translates into the spectrum of up to 20MHz.

It is now our job to make these drives and SMPS work for us in the way we want them to. The only practical way to increase the rise and fall times of pulse edges is filtering. For SMPS, the more filtering that is applied to their DC output the better. PWM drives require a more careful approach since trying to filter pulsed drive signals may easily make the motors perform poorly or not work at all.

Figure 11 shows the original rise edge of a servo motor drive pulse, and the modified edge after applying a servo motor filter. Figures 12a and 12b show the result of such edge modification, with a ground current drop of around 50 times.

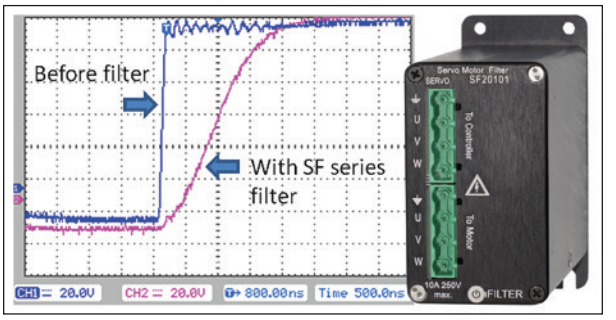

Figure 11: Modified rise time with SF20101 motor filter

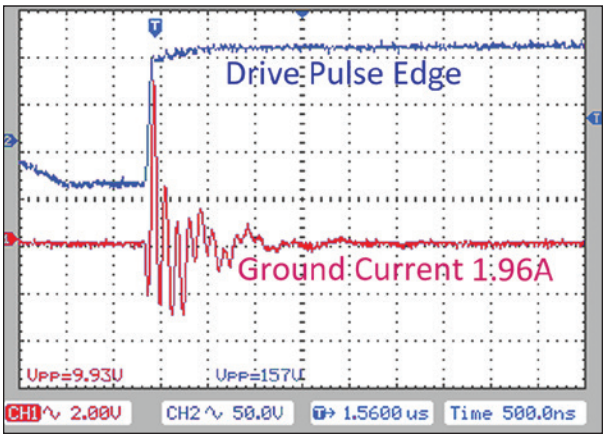

Figure 12a: Ground current without filter

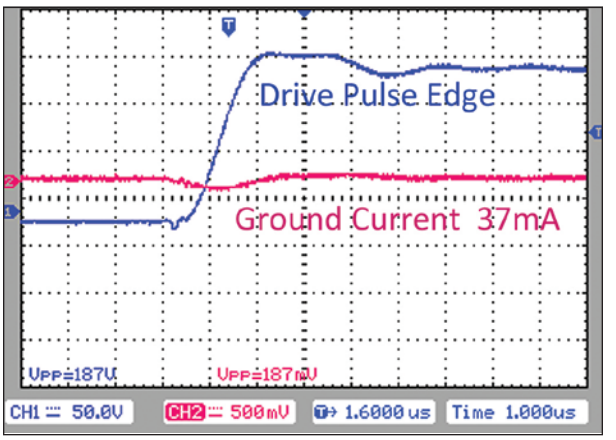

Figure 12b: Ground current with the filter

For reducing EMI from switched-mode power supplies, DC filters such as the one shown in Figure 13 are often used since they remove high-frequency content from DC supply.

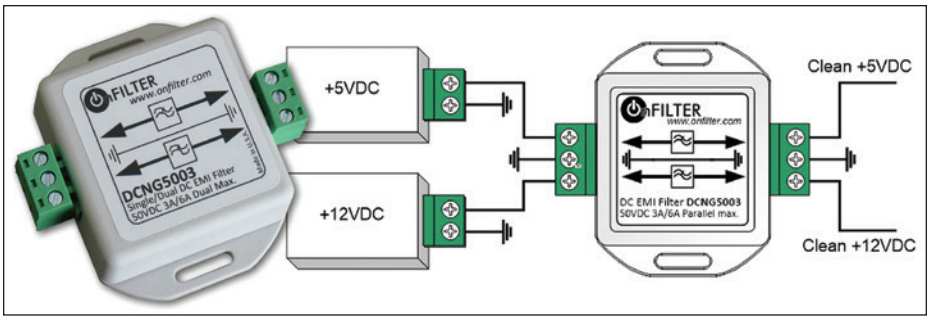

Figure 13: DC filter [23]

Blocking Propagation of EMI

Filtering of EMI is just like filtering polluted water in which you block contaminants and let clean water pass through. Our readers are likely already familiar with the concept of filtering EMI on wires and cables, even if they never considered a filter. The ubiquitous ferrite clamp (typically a black lump on a computer cable) is, in fact, an EMI filter for cables. From a technical perspective, a ferrite clamp is a current transformer with a shorted secondary that converts high-frequency signals in cables into heat (no, you won't be able to check it by touch – the energy is too low to be noticed this way). And ferrite clamps are inexpensive and easy to implement.

Figure 14: Ground EMI filter for equipment [25]

The problem is their limited performance. Most ferrite clamps become effective only at the higher end of the spectrum, above 50MHz or so (a lot of energy of EMI in manufacturing is below 1 MHz), and the attenuation they offer at these frequencies is largely limited to 10dB. A ferrite clamp is often the first way to bring EMI propagation in check. But using a ferrite clamp is not unlike using a band-aid. It will stop minor bleeding and cover a small scratch, but it just won't be sufficient in cases involving more serious injuries.

Ground EMI filters, such as the one shown in Figure 14, offer much better performance by providing substantial attenuation of broadband signals while also providing low impedance for the mains' frequencies (let's not forget that ground is a safety element). One of the applications of a ground filter is shown in Figure 15. It addresses the issue of EMI-caused EOS exposure, as shown in Figure 8. The modification is straightforward and involves an insulative plate made of mechanically hard material, such as FR4, Bakelite,

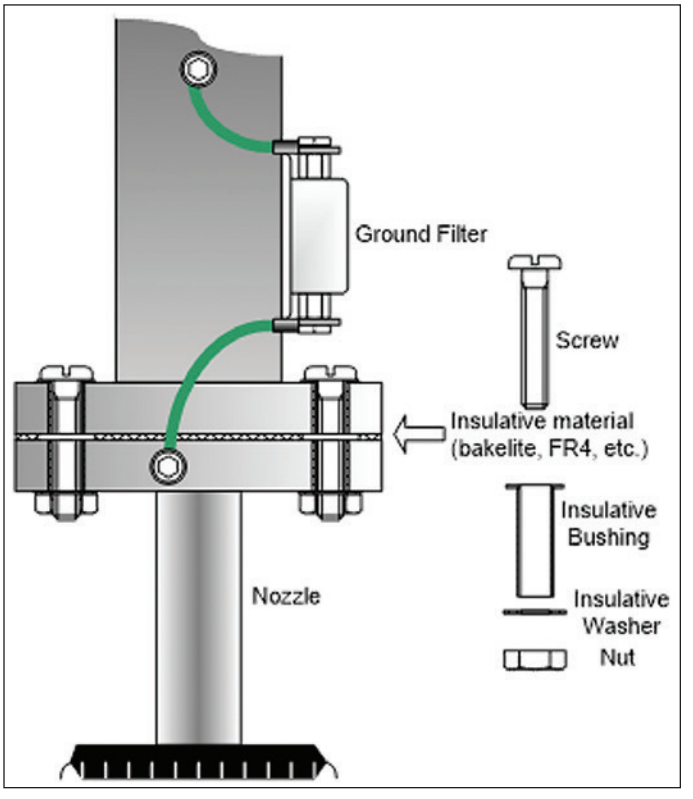

Figure 15: Ground filter on robotic arm blocks EMI on the nozzle

or equivalent, sandwiched between the parts of the robotic arm and the end piece is grounded via the filter of Figure 14. (See [24] for a detailed description of the implementation of such filtering in an IC handler in production).

Figures 16a and 16b show ground current between the robotic arm and the corresponding chassis without and with the filter. Such a ground filter inserted in wires for ESD grounding inside equipment will block the propagation of EMI throughout the tool while complying with all relevant ESD and safety standards. A similar approach with similar results can also be taken at a facility ground level, especially in facilities that employ separate grounding. In such cases, inserting a ground filter every few meters prevents EMI from propagating from noisy tools to the tools that require a low-noise environment.

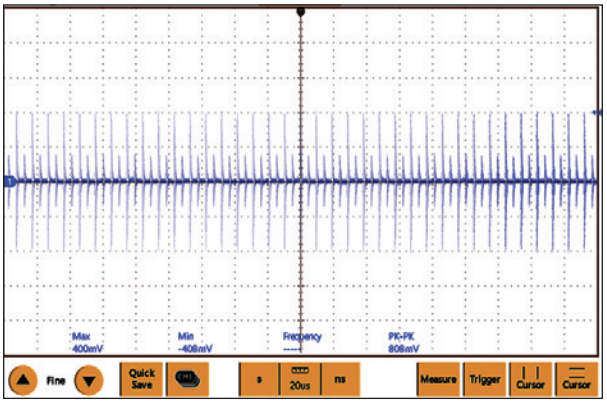

Figure 16a: Ground current without filter

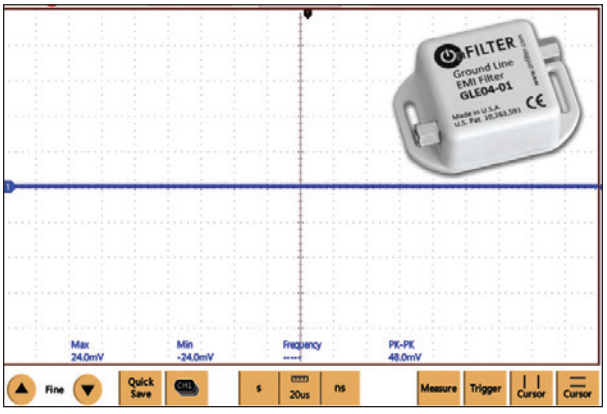

Figure 16b: Ground current with GLE04-01 installed

The key takeaway about ground filters is remembering that grounding is a safety element and that use of ground filters should not influence compliance with relevant ESD standards and practices.

CONCLUSION

Proper grounding extends beyond just running a green wire. A good grounding can help ensure the uninterrupted operation of your equipment and the integrity of your data, while a bad ground can do just the opposite. Whether you are an electrician, an ESD practitioner, or an EMC engineer, you should consider and address not just the aspect of grounding that aligns with your specialty but all grounding considerations, including safety, ESD, EMI, and data integrity. In most cases, a single standard cannot sufficiently account for all needs in the process. Pay special attention to EMI on ground as it connects all equipment and is a conduit for EMI spread. Comprehensive, quality ground is a solid foundation to help ensure the smooth and efficient running of your processes and equipment.

REFERENCES

1. *ANSI/ESD 6.1-2019 Standard Practice for the Protection of Electrostatic Discharge Susceptible Items – Grounding*, EOS/ESD Association.
2. *ANSI/ESD S20.20-2014 Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)*, EOS/ESD Association.
3. *SEMI E.176 Guide to Assess and Minimize Electromagnetic Interference (EMI) in a Semiconductor Manufacturing Environment*, SEMI.
4. *ESD SP10.1-2016 Standard Practice for the Protection of Electrostatic Discharge Susceptible Items – Automated Handling Equipment (AHE)*, EOS/ESD Association.
5. *IEC 61340 Protection of Electronic Devices from Electrostatic Phenomena - General Requirements*, IEC, 2016.
6. "Improved IC Production Yield by Taking Into Account the Electromagnetic Interference Level During Testing," Cheng-Nan Hu et. al., IEEE Transactions on Electromagnetic Compatibility, 7/2011.

7. *ANSI/ESD S1.1-2013 Standard for the Protection of Electrostatic Discharge Susceptible Items – Wrist Straps*, EOS/ESD Association.
8. "Don't Be the Victim of Electrical Noise and EMI," J. Moulton, *Control Engineering*, October 2015.
9. "Mitigating EMI Issues in Servo Motors and Variable Frequency," V. Kraz, *Interference Technology, Test and Design Guide*, 2016.
10. https://www.allaboutcircuits.com/tools/wire-self-inductance-calculator
11. https://www.daycounter.com/Calculators/Air-Core-Inductor-Calculator.phtml
12. https://www.emisoftware.com/calculator/wire-pair-capacitance
13. "Measurements of Conducted Emission in the Manufacturing Environment," V. Kraz, *In Compliance Magazine*, Annual Guide 2021
14. "Reducing EOS Current in Hot Bar Process in Manufacturing of Fiber Optics Components," J. Salisbury et.al., EOS/ESD Symposium Proceedings, 2016.
15. "EMI-Generated EOS in a Wire Bonder," T. Iben, EOS/ESD Symposium Proceedings, 2017.
16. "Dealing With EMI in Semiconductor Manufacturing, Part II: SEMI E176-1017 Standard," V. Kraz, *In Compliance Magazine*, May 2018
17. "The Implementation of SEMI E176: Guide to Assessing and Minimizing Electromagnetic Interference in a Semiconductor Manufacturing Environment," V. Kraz et. al., *In Compliance Magazine*, September 2019
18. "How Ground Bounce Can Ruin Your Day," S. Krishnan et. al., *Signal Integrity Journal*, February 2020.
19. "Managing Electromagnetic Interference in Large Instrumentation Systems," M. Gruchalla et.al., Proceedings of IBIC2014, Monterey, CA, USA."
20. About Ground Bounce and How to Measure It," Teledyne LeCroy, 2018.
21. EMI dV/dt Filters for Servo Motors and VFD, OnFILTER, 2017.
22. Dual DC EMI Filter 3/6A 50V, OnFILTER, 2021.
23. Ground Line EMI Filter for Grounding Inside Equipment, OnFILTER, 2014.
24. "Practical Aspects of Managing EMI-Caused EOS in IC Handlers and Similar Equipment," J.J. Montalban, et. al., EOS/ESD Symposium Proceedings, 2021.

PRODUCT Showcase

CASTER CONTACT: THE ACHILLES HEEL OF ESD FLOORS

Standard ESD Resistance Tests Do Not Fully Evaluate a Floor's Suitability for Grounding Carts, Chairs, and Mobile Workstations

What's the purpose of installing an ESD floor? The most common answer to this question is "we need ESD flooring to prevent static charges on mobile personnel when they handle static sensitive parts and systems." In other words, we need the effectiveness of a wrist strap, but we don't want to deal with the restrictions of wires and cords.

While this answer highlights a key attribute of a properly functioning ESD floor, it sets the bar very low. It also short sells the many advantages an ESD floor actually offers. Like every other static mitigation component, ESD flooring is only one piece of a larger comprehensive system that keeps all parts, machines, tools, packaging, work surfaces, and personnel at the same potential.

When floors are evaluated, specifiers focus on two main performance parameters: 1) the flooring system's electrical resistance; and 2) how much charge a person can develop when walking on the floor wearing specific footwear. But what about the parts themselves? How

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By David Long

do we protect them? When we move parts from one operation to another, we don't cradle them in the palm of our hands. We move parts and systems in zip lock bags, on wheeled carts with trays, and possibly with automatically guided vehicles. In agile manufacturing operations, the ESD floor might even be used as the primary ground for workbenches on wheels.

FLOORING BASICS

ESD floors are designed to prevent static discharge from harming electronic parts and assemblies in an ESD-protected area (EPA.) They are installed for multiple reasons. The ideal floor prevents static on:

- people
- parts and equipment
- shelves, mobile workstations, and ESD chairs

Some ESD floors satisfy all three tasks. Other inhibit static from developing on people but do little or nothing to protect equipment or ground mobile workstations, carts, and ESD chairs.

WHY DOES THIS MATTER?

To produce quality products, pass ISO certification, and satisfy customers, electronics facilities must meet ANSI/ESD S20.20. In an effort to meet ESD flooring requirements in ANSI 20.20, buyers and specifiers often focus all their attention on the electrical resistance of the flooring/adhesive system. But resistance is only one performance parameter.

Finding floors that meet S20.20 point-to-point (RTT) and point-to-ground (RTG) resistance requirements is an easy task. Adherence to all aspects of ANSI/ESD S20.20 requires the floor to perform multiple functions, and not just meet an electrical resistance parameter. It's equally important to determine the maximum voltage the floor will generate on a person in combination with specific footwear. Furniture, mobile workstations, and equipment must also be properly grounded through the floor, with resistance between the castors and ESD floor ground within the S20.20 acceptable range (< 1.0 x10^9).

Below are some tests every end-user should perform when evaluating floors:

- STM 7.1 Acceptable system resistance < 1.0 X 10^9 (Tool used: Ohm meter and NFPA probes)
- STM 97.1 Acceptable person + footwear + flooring system resistance < 1.0 x 10^9 (Equipment used: Ohm meter and NFPA probes)
- STM97.2 Maximum voltage measured on a person wearing ESD footwear while walking on an ESD floor: less than 100 volts (Equipment used: Charge plate monitor/field meter)
- STM4.1 Verification (page 18, Section 12.3 TR53-01-18) Maximum resistance between mobile ESD workstation surface and ground while resting on a grounded ESD floor < 1.0 X 10^9 (Equipment used: Ohm meter and NFPA probes)

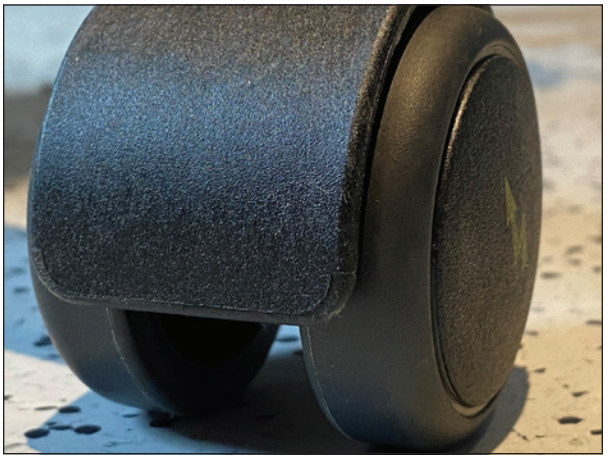

Figure 1: Conductive chair caster on an ESD Floor

A CASE HISTORY

As part of an ESD tile evaluation by the facilities department at a medical instruments manufacturer, test floors were installed. Various properties were evaluated, including flatness, slip characteristics, flooring system resistance, body voltage generation, ease of rolling heavy equipment, maintenance, and difficulty of installation and repairs.

One of the flooring options met all criteria including the ability to install without adhesive using internal labor. However, prior to ordering the flooring, a manufacturing engineer placed several mobile carts on the test floor and measured resistance to ground from the cart surface through the conductive casters to the floor's groundable point.

Despite the fact that the floor by itself had measured in the conductive range ($< 1.0 \times 10^6$) per ANSI/ESD S7.1 tests, the flooring failed the mobile workstation test, with the resistance to ground measurements from the cart surface ranging from 1.0×10^6 to 1.0×10^{12}. Per ANSI/ESD S20.20, any measurement $\geq 1.0 \times 10^9$ constitutes a failure. Seven measurements out of the initial 40 test points exceeded the ANSI maximum (see Table 1).

This sampling was followed up with over 1000 measurements. The reject rate was approximately 16%. Was the cart the problem? When placed on a metal plate, the cart resistance to ground measured well below 1.0×10^7. To eliminate contamination as a variable, the flooring and casters were thoroughly cleaned and retested. This had little impact and measurements remained unacceptable. The resistance between the cart and the floor changed by four to six orders of magnitude simply by moving the cart as little as one inch. Given that the flooring resistance and the cart caster resistance exhibited consistency, the only remaining variable was the random placement of casters (caster and floor interface) on the floor tiles.

ANALYZING THE DATA

Figures 2 and 3 are photos of a tray cart commonly found in electronic manufacturing service (EMS) facilities. The cart is resting on a flooring system that utilizes conductive chips. This floor would be categorized as a low density (LD) conductive chip floor. This particular flooring system provides a conductive path from black surface chips through its thickness to a carbon loaded ground plane on the underside. A 24" copper strip was used as a groundable point. When tested with a five-pound (2.27 Kg) NFPA probe measuring 2.5" (6.35 cm) the flooring resistance measures well below 1.0×10^6.

In Figure 2, the cart to ground measurement exceeds the limits ($< 1.0 \times 10^9$) of ANSI/ESD S20.20. In Figure 3, a compliant measurement is the result of a minor change in the position of the same cart on the same floor tile. Just like the results in Table 1, these resistance measurements confirm a high correlation between negligible changes in caster placement and significant changes in resistance.

Like the cart shown in Figures 2 and 3, the carts used by the medical equipment manufacturer were built with four conductive casters. The resistance to ground between the cart and groundable point met ANSI/ESD requirements 84% of the time. An 84% pass rate means that, for 16% of the time, not a single conductive caster made adequate contact with the conductive chip floor.

Another way to look at this would be to view the data from the perspective of the probability of four consecutive events having the same outcome. In this case, the events would be simultaneous. For example, what is the probability of flipping heads four times in a row in a coin toss experiment? The equation would

9 x 10 E6	5 x 10 E6	6 x 10 E6	8 x 10 E6
1 x 10 E7	1 x 10 E6	2 x 10 E7	7 x 10 E6
5 x 10 E6	1 x 10 E6	1 x 10 E7	2 x 10 E2
2 x 10 E8	1 x 10 E12	1 x 10 E8	8 x 10 E6
5 x 10 E7	2 x 10 E7	1 x 10 E7	7 x 10 E6
2 x 10 E6	2 x 10 E6	1 x 10 E1	2 x 10 E6
2 x 10 E10	4 x 10 E9	1 x 10 E8	2 x 10 E10
5 x 10 E6	9 x 10 E7	1 x 10 E6	9 x 10 E6
2 x 10 E11	9 x 10 E8	9 x 10 E9	5 x 10 E7
8 x 10 E7	2 x 10 E9	9 x 10 E6	3 x 10 E9

Table 1: 40 resistance measurements from cart surface to groundable point through medium density ESD floor tiles. Cart locations were altered by as little as one inch between measurements. Test area measured over 100 square feet. Multiple areas were tested. Carts were equipped with four conductive casters.

be the odds of a single event occurring multiplied by itself four times, that is ½ x ½ x ½ x ½ = one in 16.

If we loosely apply this approach to our flooring problem (for simplification we are excluding particle density vs total area), we might say that after 100 tries we can randomly get all four casters to simultaneously not touch a conductive particle 16 times. So, what is the possibility of any single caster not touching a conductive particle? At a minimum, we are questioning the likelihood of four consecutive either/or events occurring. Our simple equation might look as follows. X times X times X times X = 16/100. So, if we solve for X, the fourth root of 16 equals two and the fourth root of 100 equals 3.1. Essentially the odds of any single caster not touching the conductive elements on the floor is 66%.

For starters, this presents a valid argument to install conductive casters on every cart post. But the real takeaway is to pull out that old statistics book and conduct a valid experiment before assuming any ESD floor will ground mobile workstations based on compliant ANSI/ESD 7.1 test results.

EFFECTIVE FLOORING IS THE SOLUTION

This problem can be easily avoided when new floors are purchased. When evaluating an ESD floor, it's imperative to evaluate the floor as part of the facility and the processes within the facility. Flooring should be tested for compatibility with all ESD mitigation components, including material handling processes. A fully functional floor can act as the anchor to all mobile grounding requirements.

A key attribute of many ESD floors is the ability to eliminate cumbersome and redundant tethering processes inside the EPA. ESD floors also eliminate the need for enclosing parts in covered tote boxes and shielding bags. But in order to eliminate the use of cumbersome packaging and tethering protocols, the floor must provide a compliant path to ground for mobile material handling fixtures on casters.

Some ESD floors cannot ground conductive casters effectively due to poor contact between casters or glides and a low density of conductive points or chips on the surface of the floor. In certain cases,

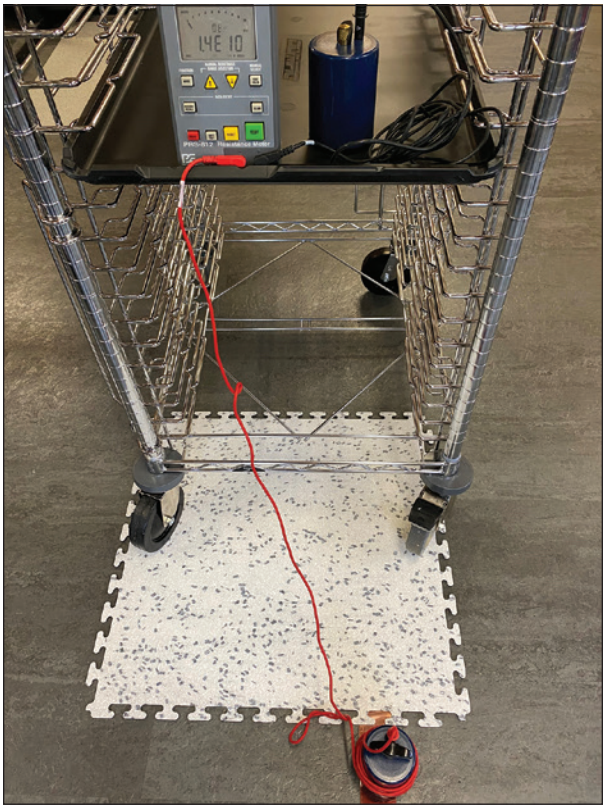

Figure 2

Figure 3

this problem is exacerbated by a micro-thin factory application of low-maintenance polyurethane or ceramic coating on the floor's surface. These UV-cured coatings reduce maintenance at a cost. Most testing shows that micro-thin coatings increase the floor's electrical resistance and diminish the control of walking body voltage.

Figure 4

Figure 5: A space or void would show a contact area/patch between caster and tile.

CHIPS vs. CONDUCTIVE VEINS

Some ESD vinyl tiles derive their conductivity from randomly located conductive chips similar to the tile shown in Figure 4. The black chips are the only conductive element on the tile surface. The rest of the surface is ordinary vinyl, that is, an insulative polymer that provides no connectivity to ground.

As illustrated in Figure 4, we can evaluate this liability by turning our NFPA probe on its edge and measuring a contact area between conductive chips and ground. The tile sample shown in the figure measured less than 1.0×10^6 when the full 31 cm^2 probe surface was used in an ANSI/ESD S7.1 test. However, the polymer between the chips is nonconductive. When a caster contacts the non-conductive polymer in between chips instead of contacting a conductive chip, measurements change by over five orders of magnitude.

For a portable workstation or chair to meet ANSI/ESD S20.20, resistance to ground must be below 1.0×10^9.

CONTACT AREA AND ITS IMPACT ON CONTINUITY

To understand the problem, we looked at the size of the conductive casters and tried to determine how much of their surface area actually touches the floor. First, we tucked four pieces of paper under the caster, sliding the paper from four different directions until it would not slide any further (see Figure 5).

When we lifted the paper, we expected to see a space where the four slips of paper did not meet. The space or void would show us approximately where the castor had been in contact with the floor. Before moving the caster, we taped the pieces of paper together so they would stay in place. Then we rolled the chair off the paper. Because we were able to tuck a fair amount of paper under the castor, we expected the contact area between the castor and floor tile to be small. We were surprised to see that it was barely larger than a sliver. In fact, the actual contact area was smaller than a dime (see Figure 5).

Think of the open space in the paper as a viewing window. We slid the window around the tile. When we don't see a black chip inside the viewing window, we are looking at a section of tile that will not ground a caster. Even when it provides some degree of

conductivity when most of the caster contact area rests on the void between chips, the resistance will likely measure above 1.0 x 10^9.

CASTER BASICS

A typical conductive caster measures approximately 10 cm in diameter but has a contact area of only one square cm. To put this in perspective, the NFPA probe used to measure the resistance from the surface of an ESD floor to ground has a contact area of 31 square centimeters. The distance between conductive particles used in a low-density chip technology (see Figure 9) ESD floor can measure from .5 cm up to 10 cm with an average of 2 to 5 cm. Therefore ANSI/ESD STM 7.1 resistance testing will not predict whether a particular floor will consistently provide electrical contact between casters and flooring.

The only way to make an accurate determination is by conducting a statistically valid sampling of resistance measurements using the carts, casters, and flooring

Figure 6: The solid grey area between the quarter and the dime represents the contact area of the caster and tile.

that will be purchased by the facility. This should be done before any flooring is ordered. Once a floor has been installed, it is too late to address the problem. Most flooring manufacturers do not provide data or warranties involving caster contact resistance.

ESD VINYL AND RUBBER WITH CONDUCTIVE VEIN TECHNOLOGY

If we place the same paper with the caster contact-sized viewing window on an ESD vinyl tile made with a tight matrix of conductive veins, we can move the window any place on the tile and still see veins. Due to the tight distance between veins in this conductive matrix, it's impossible to find an area of the floor that is not conductive. This tight matrix of conductive veins increases contact opportunities between tiny caster surfaces and the conductive elements in the tile. Any place we see veins, the conductivity in the tile will ground chairs and carts.

ESD vinyl tiles made with conductive vein technology contain approximately 150 linear feet of conductive veins per square foot. To put this in perspective, the veins on thirty-six tiles provide one linear mile of conductive contact points. With this many conductive contact points, even contact from a single caster yields an ANSI S20.20-compliant measurement 100% of the time. Can this issue be resolved with floors using conductive chip technology?

Figure 8 provides a visual comparison between a low density (LD) dispersion conductive chip floor with a high density (HD) dispersion conductive chip floor. The distance between chips on an LD floor can range between .5 to 5 centimeters within the same tile or sheet. Chip distances rarely exceed .5 cm on an HD chip floor. Chip technology floors can be produced in sheets or rolls for seamless installations. Vein technology floors cannot be made in rolls due to limitations in the manufacturing process. Vein floors are only available as tiles.

CONCLUSIONS AND TAKEAWAYS

ESD floors should be thoroughly evaluated for multiple functions, including compatibility with material handling equipment. There are two main technologies used for producing ESD tile and sheet flooring: conductive vein technology and conductive chip technology. The technology used to produce ESD flooring influences performance. Conductive vein floors outperform low and medium-density chip technology floors in instances where the floor must

Figure 7: Contact area/patch of caster superimposed over conductive vein technology floor

Figure 8: Low-density chip floor (on left) and high-density chip floor (right)

ground mobile workstations and carts. This is due to an inadequate number of conductive contact points in typical LD and medium-density conductive chip floors. New high-density chip technology solves this problem and offers the same level of performance as conductive vein technology floors.

To wrap up, here are a few key takeaways:

- Don't assume compliant ANSI/ESD S7.1 test results validate a flooring material's ability to ground mobile equipment on casters. STM 7.1 probes make 31 cm^2 of contact. A caster only makes 1 cm^2 of contact.
- Always perform a statistically valid sampling of ANSI/ESD STM 4.1 tests on shelving, carts, and mobile workstations using the ESD floor as ground surface.
- Always move casters and glides between tests. Slight variations in caster location contribute to extreme fluctuations in measurements. Perform tests in multiple areas. Tiles coated with urethane and ceramic exhibit variations from tile to tile.
- Test all potential cart/caster flooring combinations.
- Always use four conductive casters. Use conductive not dissipative casters.
- Never rely on drag chains for mobile workstation ground connections since the contact area is too small.
- Test before you buy. Install a test area of several tiles.
- As always, ESD floors must be tested for walking body voltage generation per ANSI/ESD 97.2.

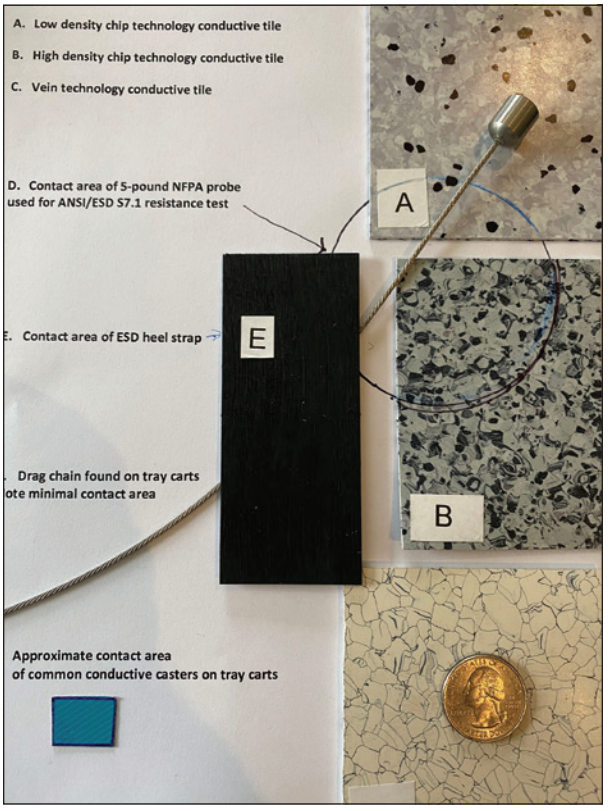

Figure 9: Note the large contact area of an NFPA probe in comparison to actual items intended for grounding through an ESD floor:

- D—NFPA probe contact area = approx. 31 cm^2
- E—Typical heel strap: > 13 cm^2
- G—Caster contact area = 1 cm^2
- F—Ground chain contact area = negligible

Figure 10: A conductive vein matrix ensures compliant grounding.

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September 23
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September 28
IEEE EMC Chicago Mini Symposium

September 30
EMC Fest 2021

October 7
EMC Mini

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