NOVEMBER 2023

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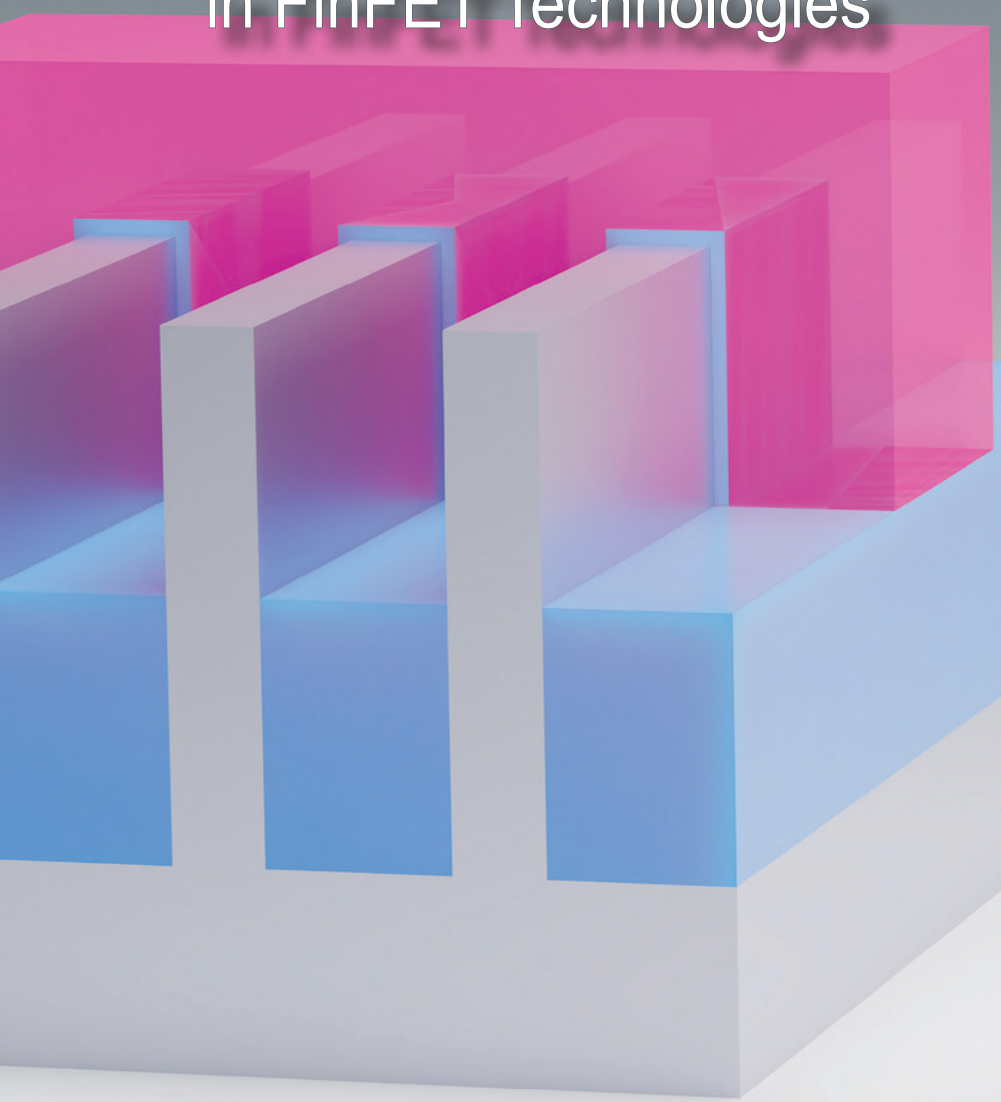
ESD Co-Design

for High-Speed SerDes in FinFET Technologies



PLUS

The EU's New Product Safety Law Will Be a Game Changer

Reduced-Order Modeling of Pennes' Bioheat Equation for Thermal Dose Analysis

The Duty to Warn: Do Warnings Make a Product Safe?

Solid-State Amplifier Selection Tips for EMC Testing

Investigate the following parameters when selecting a solid-state amplifier for EMC testing:

Class of Operation

Class A solid state amplifiers are the preferred technology for EMC RI and CI testing. They are favored for repeatability of test results compared to Class AB and other types. Verify that the Class A amplifier can tolerate load mismatches and simultaneously remain operational, without amplifier damage, foldback or shutdown.

Rated Output Power

Compare actual production power curve test results, and avoid assuming rated power based on model date sheet specifications.

Linearity & Harmonic Distortion

For repeatability of test results, seek amplifiers with good linearity and low harmonic distortion. Linearity should be less than ±1 dB (subject to your application) and harmonics are preferred below 18 dBc.

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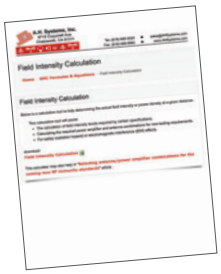

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IN COMPLIANCE

NOVEMBER 2023 CONTENTS

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FCC Chair Rosenworcel Proposes Restoration of Net Neutrality Rules

The Chair of the U.S. Federal Communications Commission (FCC) is reportedly moving forward with a proposal to reestablish the Commission's authority over broadband services across the U.S. by restoring net neutrality rules nationwide.

In a speech before the National Press Club, Rosenworcel laid out her case to reinstate broadband internet services as an essential "telecommunications service" under Title II of the Communications Act. Arguing that the internet is too important to society and the economy not to have effective oversight, Rosenworcel proposed restoring net neutrality rules with the goal of protecting internet openness and consumers, defending national security, and advancing public safety.

"The COVID pandemic taught us—with painful clarity—just how important broadband access is in modern life," Rosenworcel said in her speech. "We have made a historic commitment to ensure high-speed internet access reaches all. We have invested in this infrastructure like never before. Now let's make sure it is fast, open, and fair for consumers everywhere."

The FCC's net neutrality rules were originally adopted by the Commission in 2015, based on a 2005 Policy Statement affirming open internet principles. But the rules were subsequently repealed by the Commission in 2018 under the Trump Administration.

In line with Rosenworcel's proposal, the FCC is expected to release a Notice of Proposed Rulemaking (NPRM) by mid-October, detailing the plan to restore uniform net neutrality rules applicable to broadband providers nationwide.

FDA Issues Guidance on Medical Device Cybersecurity Quality System Considerations

The U.S. Food and Drug Administration (FDA) has released its Final Guidance on cybersecurity considerations for medical devices to assist device manufacturers in preparing premarket submissions.

The Final Guidance, "Cybersecurity in Medical Devices: Quality System Considerations and Content of Premarket Submissions," provides recommendations on cybersecurity device design, labeling, and documentation that the FDA recommends be included in premarket submissions for medical devices that pose a potential cybersecurity risk.

The Final Guidance also recommends that device manufacturers consider adopting a secure product development framework (SPDF), a set of processes aimed at reducing the number and severity of potential vulnerabilities in a given device throughout the device's entire lifecycle.

Apple to Update iPhone 12 Software Following Ban in France

Apple Corporation has notified regulatory authorities in France that it will issue a software update for iPhone 12 users in that country to address concerns about excessive electromagnetic radiation levels associated with the phone model.

France's National Frequency Agency (Agence Nationale des Frequencies, or ANFR) ordered Apple to temporarily withdraw its model iPhone 12 from the French market due to concerns about the device exceeding the regulatory specific absorption rate (SAR) limits established by the Commission of the European Union (EU).

According to an article posted to the website of the Associated Press (AP), Apple claims that the problem raised by the regulators is "related to a specific testing protocol" used by French regulators to assess SARs levels, and that the software update will "accommodate the protocol."

FCC Issue Citations for Harmful Interference Traced to Surveillance Cameras

The U.S. Federal Communications Commission (FCC) has recently issued citations to two separate parties for operating home security cameras that caused harmful interference to licensed radio operations.

The first Citation and Order has been issued against a resident in Joppa, Maryland. Investigating a consumer's complaint in late 2022 that interference from a nearby residence was blocking the reception of transmissions from Sirius XM radio, agents from the FCC's Enforcement Bureau's Columbia Field Office determined that the source of the interference was a surveillance camera located above a garage door of the residence. The camera did not bear any FCC Identifier or any other labeling required under the Commission's rules.

Despite numerous communications and notices issued by the Bureau to the resident, the camera remained in operation, as verified by multiple subsequent visits to the residence by Enforcement Bureau agents.

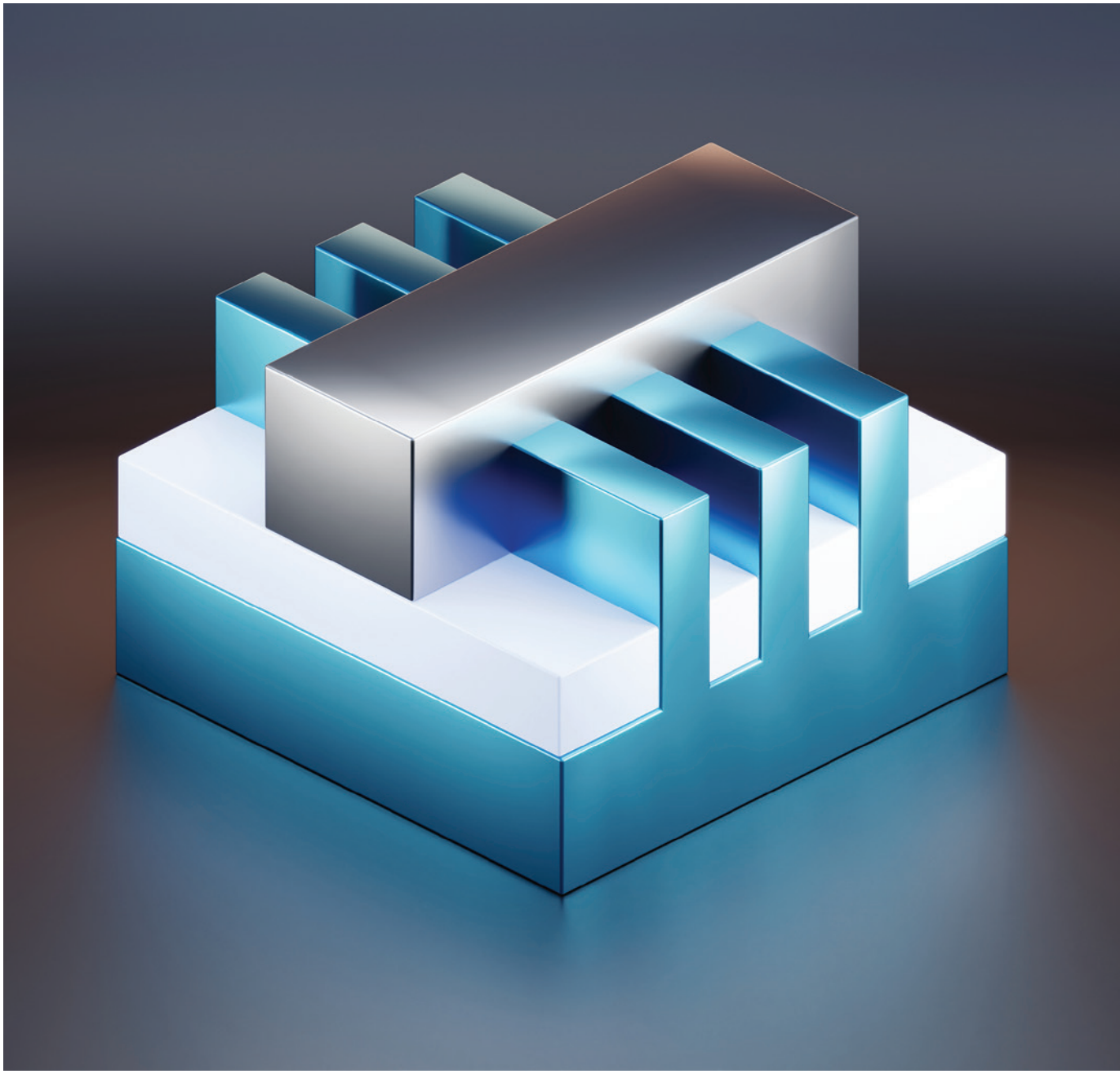
The recipients of the Citations must verify that they have ended the use of their respective camera devices or face fines of up to $23,727 for each day of noncompliance.

A second Citation and Order has been issued against a York, Pennsylvania resident for causing unlawful interference in the 2500 MHz wireless services band. Once again, agents from the Columbia Field Office investigated the interference following receipt of complaints from wireless carrier T-Mobile and traced the interference to a surveillance camera system installed at a York residence. And, again, the camera system remained in operation, despite ongoing communications to the resident from the Bureau.

In both cases, the recipients of the Citations must verify that they have ended the use of their respective camera devices or face fines of up to $23,727 for each day of noncompliance.

ESD CO-DESIGN FOR HIGH-SPEED SERDES IN FINFET TECHNOLOGIES

How to Maximize the ESD Robustness of High-Performance Interface IP



Peter de Jong is an ESD/LU specialist at Synopsys and is responsible for ESD solutions in a wide range of interface IP. He can be reached at pjong@synopsys.com.

By Peter de Jong for the EOS/ESD Association, Inc.

On-chip ESD protections are used to achieve the necessary robustness against ESD threats during the manufacturing and handling of the devices. For high-speed SerDes interfaces, interference by the ESD protection measures (e.g., due to added capacitive load on the I/O) can severely deteriorate performance speed. Together with the continuously decreasing ESD design window in the latest (FinFET) technologies, smart co-design of ESD protection with the SerDes transmitter circuit has become a necessity to accomplish both speed and ESD targets.

In this article, we'll show how parasitic elements in the driver transistors can be exploited in a co-design style to effectively meet the ESD targets while minimally impacting speed performance. And we'll verify the correct implementation of the ESD measures using a programmable electrical rules checking (PERC) tool.

BACKGROUND

An electronic device is susceptible to electrostatic discharge (ESD) damage. To avoid yield loss due to ESD during the assembly and handling phase, on-chip ESD protection measures are applied to provide a certain degree of ESD robustness. The component ESD withstand level is classified in the Charged Device Model[1] (CDM) and Human Body Model[2] (HBM) standards. The ESD targets of the device are set according to the required CDM and HBM levels, and appropriate ESD protection measures are applied to ensure ESD robustness for all exposed device pins.

When the exposed pins are data pins of high bitrate interfaces (e.g., high-speed SerDes like 112G Ethernet and PCI Express®), interference with the necessary ESD protection measures can adversely impact functional performance. Besides, in the latest, most advanced technologies, the so-called ESD design window, which is defined as the difference between the breakdown voltage of the devices and the supply voltage level, has become extremely small[3] (see Figure 1). In order to meet the ESD targets for CDM and HBM, smart co-design of ESD protection with the SerDes transmitter circuit has become a necessity.

This article first details the problem in current FinFET technologies, demonstrating the limits of classical protection methods and the need for enhanced (secondary) protection measures in transmitter circuits. Then, we discuss how to meet the demands of high-speed SerDes interfaces with measures to minimize the capacitive load of the protections, which is accomplished by creating an intrinsic ESD robust transmitter. Next, we discuss options to obtain optimal intrinsic robustness of the transmitter by ESD co-design and their possible limitations and pitfalls. Finally, we propose a set of circuit topology and layout checks to verify ESD robust architectures and correct implementation.

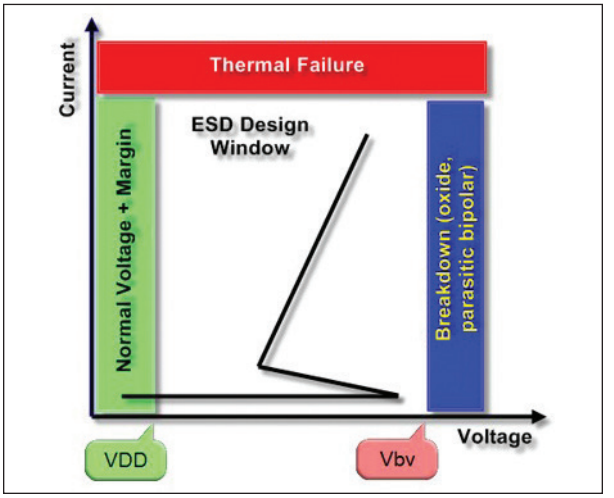


Figure 1: ESD design window is defined by V_{bv} = VDD, where V_{bv} is either gate oxide breakdown under ESD domain or parasitic bipolar trigger voltage.

It is essential to note that, while high-speed performance of the circuits is the primary objective, the challenges for simultaneously meeting minimum CDM targets are also particularly important. (See, for example, Figure 2.[4])

CLASSICAL OUTPUT DRIVER DESIGN

For more than two decades, the dual-diode ESD protection principle, in combination with an active power clamp, has been the standard concept to protect the classical output driver I/O. The basics of the concept are shown in Figure 2.

The purpose of the dual primary protection diodes is to provide a low resistance (forward diode) path for an ESD discharge on the I/O pad for both polarities. The active power clamp consists of a large transistor, often referred to as "BigFET," with a circuit that ensures the BigFET triggers on an ESD pulse and stays conducting for the entire duration of the ESD pulse.

For example, the discharge path is indicated for a positive ESD pulse on I/O with respect to ground. In this case, the discharge current flows through the conducting upper diode and via the power clamp to ground. The discharge of a negative ESD pulse is handled by the lower diode, which is, in that case, in forward conduction mode.

The protection network is adequate if the resulting voltage at the I/O pad is lower than the breakdown voltage of the I/O devices (e.g., the output driver transistors). The clamping voltage across the NFET driver transistor in the example is determined by the voltage drop across the components in the network, which is the primary diode and power clamp, increased by the voltage drop across the interconnect resistances.

To meet the product CDM specification of 250 V, which is the *de facto* standard to date, a CDM design target of 6 A typically suffices. The 6 A ESD current causes roughly ~6 V across the diode, ~1.5 V across the power clamp, and typically a few tenths of volts over the interconnect.

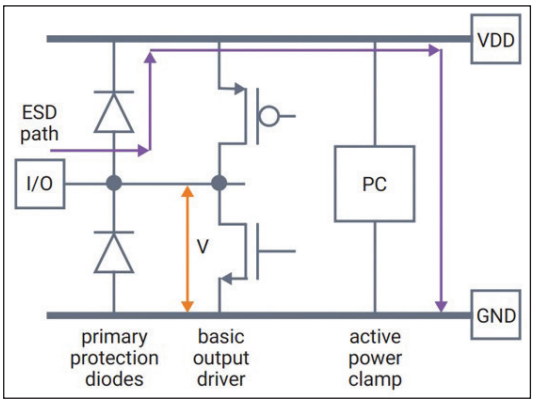


Figure 2: Output driver with dual-diode ESD protection and power clamp

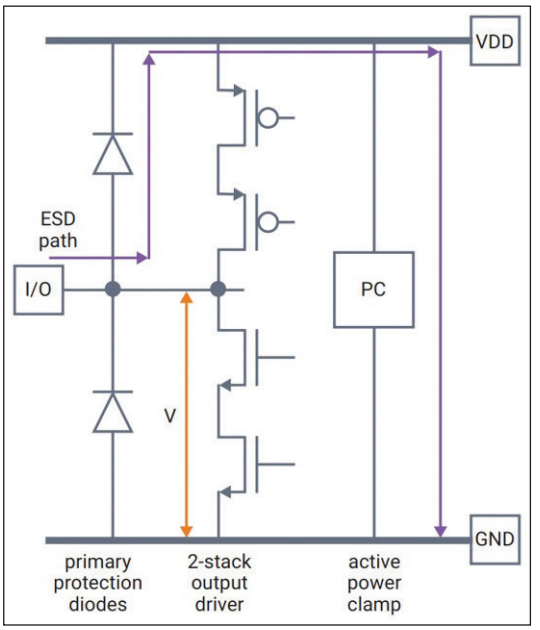


Figure 3: Output with 2-stack driver transistors for increased breakdown tolerance

For many technology generations, this concept worked out well; transistor breakdown levels of junctions and gate oxide were sufficiently high compared to the clamping voltage. In the latest technologies, however, the breakdown voltages are reduced drastically to 4 V or less and the dual-diode concept clearly falls short in protecting the basic output driver configuration. In other words, the window of Figure 1 is rapidly closing.

The protection capability can be improved by increasing the diode and/or power clamp sizes. However, the gain will saturate and practically limit to ~1 V maximum, which is most likely not sufficient.

Another possibility to increase the ESD robustness is by using stacked driver transistors, as shown in the example depicted in Figure 3.

Compared to a single transistor driver, the junction breakdown voltage of the 2-stack transistor is higher,

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depending on the layout geometry of the transistor stack, up to a factor of two. The actual ESD network is unchanged, and so the resulting clamping voltage on the I/O pad is the same, but because of the higher breakdown voltage of the stack, the clamping level might just become sufficient to protect the 2-stack transistors. The concept is extendable to 3-stack, etc. to further increase the junction breakdown level. However, further stacking is no longer beneficial when the gate oxide breakdown becomes the critical constraint.

This concept has worked successfully in the past until the introduction of advanced planar technologies. In the latest FinFET technologies, however, the gain achieved by transistor stacking is generally not sufficient, and a fundamentally different approach is required to improve the robustness of the driver.

ENHANCED ESD PROTECTION FOR OUTPUT DRIVER

A major increase in the ESD withstand level of the output driver requires the ESD protection network to be extended with secondary protection circuitry, with the principle as shown in Figure 4.

Essentially, a secondary ESD discharge path is achieved with extra diodes, separated from the primary dual diodes by a series resistor, dimensioned in such a way that the secondary circuit carries only a small fraction of the total discharge current. This small current, usually in the order of mA to tens of mA, causes a low voltage across the secondary diode, e.g., ~1.5 V. The voltage across the driver transistors, as shown in Figure 4, now determined by the voltage across the secondary diode and power clamp, reduces significantly (e.g., for the 6 A CDM example to ~3 V). The enhancement compared to the earlier estimated ~7.5 V at 6 A CDM in the case of primary protection only is significant.

The protection concept is not new. For many years, secondary protections have been prescribed for pad-connected gates in input circuitry to protect the vulnerable gate oxide. While the secondary protection is generally easily applicable in input (receiver) configurations with moderate effect on the functional performance, in the case of outputs (transmitters), the large series resistor in combination with diodes (adding capacitance) can pose serious challenges in meeting the transmitter specifications, especially in high-speed interfaces. Even a 10 Ohm series resistor can limit the transmission speed to 15 GBs for the 6 A target.

To mitigate the problem of a large series resistor between the driver and pad, a suitable approach is to split the driver into parallel branches, each with its own (large) series resistor. Functionally, when the transistors are conducting, the resistors are in parallel, resulting in a low effective resistance during normal operation. From the ESD point of view, the high resistance in the individual branches counts (i.e., serves the intended purpose). The number of parallel branches should be chosen such that the targeted driver impedance is achieved.

To overcome the problem of the extra capacitance due to secondary protection diodes, an alternative approach of the secondary diodes is proposed in the next section.

INTRINSIC ROBUST OUTPUT DRIVER

As we have argued, secondary protection is essential for a low clamping level. The secondary protection comprises a series resistor and dual diodes to power and ground. When the parasitic drain-well diodes of the driver transistors are exploited to represent the secondary protection diodes, an intrinsic robust driver is obtained. (The principle is illustrated in Figure 5.)

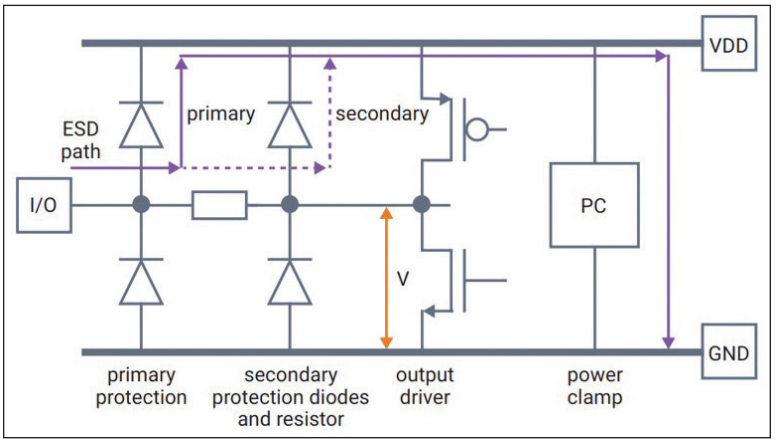


Figure 4: Driver with enhanced protection by additional secondary protection circuit

The secondary current discharge path is achieved by the (forward-connected) parasitic diode of the driver transistors. These parasitic diodes can serve as a full replacement for explicit diodes when certain device and layout constraints are met. This advantageous approach saves the extra layout area needed for diodes and, more importantly, avoids performance loss due to explicit diode capacitance.

COMPLICATIONS AND PITFALLS

It is important to realize that the upper diode (i.e., the PFET) essentially protects the lower diode (i.e., NFET) while the lower diode protects the upper diode. Consequently, for the secondary protection to be effective, it is essential that the upper and lower diodes are both connected to the same resistor node. Special transmitter configurations may require the separation of the pull-up (PFET) and pull-down (NFET) circuits, which means that two resistors must be used, as illustrated in Figure 6.

In this case, the driver transistors lack protection, as one of the essential parasitic diodes is disconnected from the transistor it is intended to protect. The transistor's

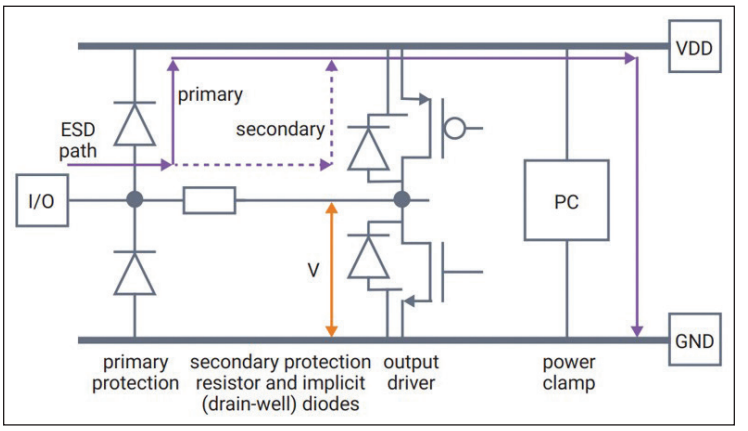


Figure 5: Intrinsic robust driver with parasitic diodes used for secondary protection

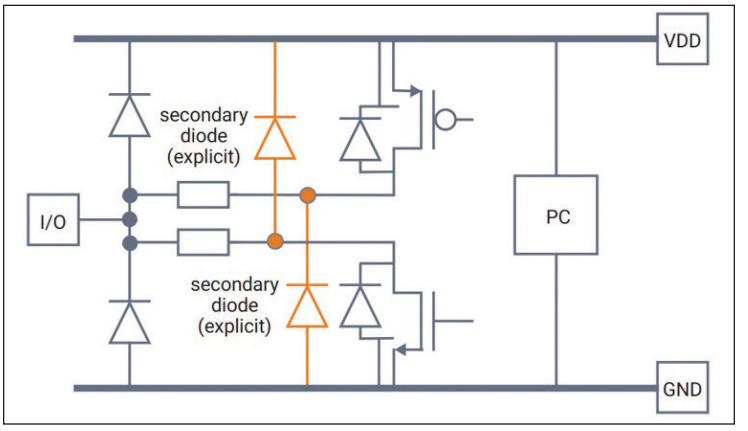
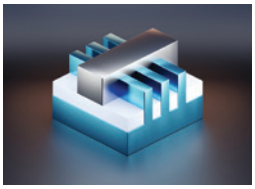


Figure 6: Driver configuration with separated pull-up and pull-down requires additional explicit diodes (indicated in orange) to complement the parasitic transistor diodes



In practice, a set of guidelines regarding minimum diode size and maximum anode-cathode spacing, along with a routing resistance recommendation, are sufficient to make the parasitic diode approach successful.

parasitic diode still plays a role for one discharge polarity, but the missing diode due to the resistor separation needs to be compensated by explicit diodes, as indicated in orange in Figure 6. In case of a separated pull-up and pull-down, it is not possible to only use the driver parasitic diodes.

Another potential pitfall occurs when, for design-specific reasons, the transistor's well (for example, the N-well of the PFET) is not connected to power. The parasitic diode exists but provides no (direct) discharge path to the power clamp. Thus, protection of the NFET is obstructed. A similar problem may occur for NFET in isolated P-well without a direct connection to ground. Depending on the applications, a possible solution is adding explicit protection diodes (stacked, if necessary) to power and ground.

LAYOUT CONSIDERATIONS

Special care is needed in the layout of the driver transistors to ensure that the parasitic diode properties are suitable for protection purposes. Generally, good parasitic diodes are accomplished by simple measures that don't conflict with the functional requirements of the driver but still account for the required extra diode function of the driver devices in the layout phase. Important parameters to consider include:

- The effective diode size (drain diffusion area and perimeter);
- Anode-cathode spacing (drain diffusion to well contacts);
- Routing resistance from the well contacts to the nearest power clamp; and
- Current density requirement in the secondary current path.

These parameters should be adjusted with proper layout measures to achieve low resistance in the secondary protection current path through the diode to the power clamp.

For an accurate evaluation of a secondary protection implementation, the ESD characteristics of the parasitic diodes are needed. However, the parasitic diode protection approach is relatively new, and data on parasitic diodes is often not part of the standard foundry ESD data offering. An additional complicating factor is the unlimited variety of possible driver layout implementations and, thus, diode variants, which cannot be covered by foundry ESD test structures.

Nevertheless, considering the low current through the secondary protections, the resistance realized by the diode implementation is by far not as critical as it is for the primary network. For instance, a resistance of 50 ohm gives a 10 mA current just 0.5 V extra voltage drop, which hardly reduces the huge advantage brought in by the secondary protection.

In summary, exact ESD characteristics of the parasitic diodes are preferred but not necessary. In practice, a set of guidelines regarding minimum diode size and maximum anode-cathode spacing, along with a routing resistance recommendation, are sufficient to make the parasitic diode approach successful.

CIRCUIT AND LAYOUT CHECKS FOR ESD ROBUST DRIVER CONFIGURATIONS

In this section, we offer some recommendations for relevant check items to ensure ESD robust implementation of the driver designs in the IP. The checks include topology on a schematic level as well as checks on the layout.

Important topology checks on the driver schematic include:

- Any driver transistor should have a resistor with a minimum value (e.g., 200 Ω) between drain and I/O bump;
- All driver transistors should have dual diode (explicit and/or implicit) secondary protection;

- Secondary protection diode minimum dimension (area and/or perimeter) depending on the series resistor value; and
- Direct connection of the diodes to the power clamp.
- These topology checks on a schematic level ensure that a robust I/O architecture is applied.
- Supplementary checks on the layout level are also recommended to ensure the efficiency of the implementation. These include:
- Current density for all secondary protection components and connections;
- Anode-cathode spacing should not exceed the maximum distance (e.g., 1 µm), and
- Resistance of the diode connections to the power clamp should not exceed a maximum (e.g., 50 Ω).

The values within brackets are estimates since exact values can vary depending on technology and design strategy. When the implementation of the secondary protection uses implicit diodes, the EDA check tool should be able to find the parasitic elements and subsequently apply the necessary property checks. As an example, Synopsys ICV PERC, used to sign off all Synopsys interface IP, is such a verification tool, capable of recognizing parasitic diodes without the need for marker layers and performing all property checks.

SUMMARY

Due to the narrow ESD design window in modern FinFET technologies, the classical ESD protection concept with dual diode is insufficient to protect transmitters with single or stacked transistor driver configurations. Secondary protection of the driver circuitry is necessary to meet the industry component ESD targets for CDM and HBM.

The series resistor inherent to the secondary protection can be achieved by splitting the driver into multiple parallel paths. When secondary protection diodes can't be implemented in high-speed SerDes designs due to the extra capacitive load, an alternative solution is to use the parasitic diodes of the driver transistors as secondary protection. Successful ESD co-design also includes special care in the layout to ensure that the implicit protection is effective.

We strongly recommend the use of an appropriate EDA tool to check all I/O circuitry thoroughly for the presence of the secondary protections, either using explicit or implicit diodes, and to help ensure robust ESD designs. Besides topology on the schematic level, the checks should also include critical properties in the layout.

For the Synopsys high-speed SerDes IP portfolio, which includes PCIe 6.0, 112G, and 224G, optimal ESD withstand levels within the high-speed performance constraints are achieved by utilizing ESD co-design. ICV PERC delivers an adequate verification solution for these IPs.

ENDNOTES

1. ANSI/ESDA/JEDEC JS-001-2022, "Charged Device Model (CDM) - Device Level," June 2021.
2. ANSI/ESDA/JEDEC JS-001-2017, "Human Body Model (HBM) - Component Level," May 2017.
3. Industry Council on ESD Target Levels, "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements, Rev. 3.0," May 2021.
4. R. Ashton, "Updated Trends in Charge Device Model (CDM)," *In Compliance Magazine*, May 2023.

THE EU'S NEW PRODUCT SAFETY LAW WILL BE A GAME CHANGER

Companies Must Prepare to Embrace the New Rules

Rutger Oldenhuis LLM is an independent business lawyer and the founder of RecallDesk, a one-stop service provider in the field of product compliance, product safety, and recalls. He frequently writes blogs for *Bike Europe* and contributes legal articles to *Sporting Goods Intelligence Europe* and *Eyewear Intelligence*. Oldenhuis can be reached at rutger@recalldesk.com.

By Rutger Oldenhuis

On April 25th, the Council of the European Union (EU) adopted the long-awaited EU General Product Safety Regulation (GPSR). The adoption of the GPSR was the final step of the revision of the outdated EU General Product Safety Directive (Directive 2001/95/EC, or GPSD). The GPSR will enter into application on 13 December, 2024.

The ink has yet to dry, but one thing is certain: selling consumer products in the EU will never be the same. That applies both to manufacturers based in and outside the EU. In this article, I summarize the main highlights of the GPSR.

A REGULATION AND NOT A DIRECTIVE

First of all, the GPSR is a regulation and not a directive. A regulation has a direct effect in all EU Member States without the intervention of national legislators. A directive needs to be transposed into national law and often allows Member States to include deviating provisions, which obviously jeopardizes the single market principle. That is no longer possible with a regulation. The provisions of the GPSR, therefore, apply in full in all EU Member States.

SAFETY NET

Like the GPSD, the GPSR is a legal safety net, but it contains more extensive and more far-reaching provisions than the GPSD. Some of the provisions do not apply to products covered by Union harmonization (or sectoral) legislation since they are already covered in such legislation. Other provisions do apply in order to complement Union harmonization legislation, for example, when certain types of risks are not covered by that legislation. This sometimes makes it a difficult puzzle to determine which provisions of the GPSR do or do not apply to a specific product. It is important to note that the provisions in some areas (for example, recalls and remedies) apply to all products within the scope of the GPSR.

THE SCOPE OF THE GPSR

The GPSR applies to consumer products but excludes the following products:

a. Medicinal products for human or veterinary use;

b. Food;

c. Feed;

d. Living plants and animals, genetically modified organisms, and genetically modified microorganisms in contained use, as well as products of plants and animals relating directly to their future reproduction;

e. Animal by-products and derived products;

f. Plant protection products;

g. Equipment on which consumers ride or travel where that equipment is directly operated by a service provider within the context of a transport service provided to consumers and is not operated by the consumers themselves;

h. Aircraft referred to in Article 2(3), point (d) of Regulation (EU) 2018/1139; and

i. Antiques.

It is worth noting that the GPSR clarifies software-related rules and now explicitly covers software embedded into a product. The GPSR also addresses the safety of products linked to new technologies and the new risks to consumer health, safety, and personal security posed by these technologies.

The regulation is applicable to new, used, repaired, or reconditioned products but does not extend to products marked for repair or reconditioning before use. Furthermore, the GPSR operates without prejudice to the rules established by Union law on consumer protection.

Manufacturers should adopt a broader and more comprehensive perspective when assessing potential health risks associated with the products they bring to the market.

INTRODUCTION OF "HEALTH" CONSIDERATIONS

Remarkably, the GPSR refers to the WHO definition of "health:" *"The World Health Organization defines 'health' as a state of complete physical, mental and social well-being and not merely the absence of disease or infirmity."* The term "product safety" thus takes on a much broader meaning and a whole new dimension.

We should not underestimate the profound implications that this legislative shift can bring to the legal landscape. Manufacturers should adopt a broader and more comprehensive perspective when assessing potential health risks associated with the products they bring to the market.

Let's use mobile phones as an illustrative example. It has become increasingly evident that providers of social media applications employ algorithms intentionally designed to foster addictive behavior. Additionally, a growing body of scientific research underscores the potential adverse effects of mobile phones on the mental well-being of children.

While an outright ban on mobile phones may appear implausible when compared to the regulation of, for example, alcohol or cigarettes, there is a growing recognition of the need for measures to significantly reduce their usage. Within the EU, we are already witnessing the emergence of initial initiatives aimed at addressing this issue.

Furthermore, the proposed EU Product Liability Directive notably introduces a clear definition of "product" that explicitly encompasses "software." Additionally, it specifies that the term "damage" should be understood as "material losses resulting from death or personal injury, including medically recognized harm to psychological health." This reflects the EU's efforts to adapt product liability regulations to the digital age and acknowledge that software, as a product, can have wide-ranging implications, including not only physical harm but also harm to mental health.

The possibility of class-action lawsuits against mobile phone manufacturers and social media giants like Facebook is not beyond consideration.

RISK ASSESSMENT (PRE-MARKET)

Compared to the GPSD, the GPSR gives much more attention to risk assessment. Unless already covered by Union harmonization legislation, the GPSR requires manufacturers to conduct an internal risk analysis and draw up technical documentation. In other words, in most cases, a manufacturer will have to conduct a risk analysis and prepare technical documentation before a product is put on the market.

In line with the previous section, it is remarkable that "mental health" must also be included in that risk assessment. The GPSR, for example, stipulates that a risk assessment:

> *"[…] should take into account the health risk posed by digital connected products, including on mental health, especially on vulnerable consumers, in particular children. Therefore, when assessing the safety of digital connected products likely to have an impact on children, manufacturers should ensure that the products they make available on the market meet the highest standards of safety, security and privacy by design in the best interests of children."*

This may influence the way we assess the risks of, for example, gaming and social media. And what to think of the metaverse?

QR CODE NOT ACCEPTED AS THE ONLY MEANS OF PROVIDING PRODUCT SAFETY INFORMATION

The QR code has been commonly accepted as a means to provide consumers with product safety information

TIPS FOR SELECTING *Chambers*

Presented by RAYMONDEMC

1. Since chamber selection is primarily driven by testing requirements, clearly define applicable test standards, operating frequency range, and whether the chamber will be multi-function.
2. Consider the shape, size, weight, type, and heat generation of devices intended to be tested. Ensure that the chamber dimensions can comfortably accommodate the devices under test.
3. If the chamber will be installed in an existing facility, choose a layout that conforms to space limitations and constraints imposed by the parent room.
4. A chamber manufacturer can help navigate local permitting requirements, fire suppression systems, seismic approvals, structural supports, emergency features, safety systems, and design for extreme environmental conditions.
5. The type, size, placement, and number of RF shielding doors should be decided based on frequency of personnel access and the expected movement of devices under test.
6. Explore options for chamber accessories and test equipment including turntables, antenna masts, test tables, crane or hoisting systems, shielded cameras, ramps, and more.
7. Assess connections to the parent building for electrical, HVAC, and fire suppression systems.
8. Determine if a control room, raised floor, or other custom configuration is required for cable management.
9. A modular chamber design that allows for customization, expansion, upgrades, or potential relocation, can help expand test capabilities and adapt to future needs.
10. To extend the usable lifetime of the chamber and to ensure performance, regular preventative maintenance and chamber validation testing are essential.

and instructions. However, despite heavy lobbying, the GPSR does not accept E-labelling as a replacement for old-fashioned labeling and thick multilingual manuals. Pursuant to the GPSR:

> *"…manufacturers shall ensure that their product is accompanied by clear instructions and safety information in a language which can be easily understood by consumers, as determined by the Member State in which the product is made available on the market. That requirement shall not apply where the product can be used safely and as intended by the manufacturer without such instructions and safety information."*

However, this provision does not apply to products covered by Union harmonization (or sectoral) legislation. For example, pursuant to the upcoming EU Machinery Regulation, which will replace the current Machinery Directive, instructions may be provided digitally.

ONLINE PLATFORMS ARE THE "NEW MARKET SURVEILLANCE AUTHORITIES"

An entirely new section has been included in the GPSR, detailing obligations for "providers of online platforms." This seems to be a real game changer for both providers of online platforms and all economic operators who sell products through online platforms. Although providers of online platforms are not liable for the compliance and safety of the products themselves sold through their platform, they must ensure – through a battery of due diligence obligations – that traders using their platform only sell products that comply with applicable laws and regulations.

These provisions make providers of online platforms *de facto* the new "gatekeepers" when it comes to product compliance and safety. Since most traders sell products through online platforms, this could have a tremendous (and hopefully positive) impact on the level of product compliance and safety. If traders want to sell their products via Amazon or the like, they should be in control of their product compliance and safety processes. In case of repeated non-compliance, pursuant to the GPSR, providers of online platforms will have to suspend their services to that trader until further notice.

TRADERS OUTSIDE THE EU SELLING DIRECTLY TO THE EU SHOULD ESTABLISH IN THE EU

Pursuant to the GPSR, economic operators established outside the EU can no longer sell directly to consumers in the EU through online channels without having a representative established in the EU. The representative established in the EU is the person or entity to be contacted if products do not comply with EU legislation. The GPSR states:

> *"Direct selling by economic operators established outside the Union through online channels hinders the work of market surveillance authorities when tackling dangerous products in the Union, as in many instances economic operators may neither be established nor have a legal representative in the Union. It is therefore necessary to ensure that market surveillance authorities have adequate powers and means to tackle in an effective manner the sale of dangerous products online."*

Economic operators established outside the EU must:

> *"…ensure that there is a responsible economic operator established in the Union, which is entrusted with tasks regarding such products, providing market surveillance authorities with an interlocutor and, where appropriate with regard to the possible risks related to a product, performing specific tasks in a timely manner to ensure that the products are safe. Those specific tasks should include regular checks with regard to compliance with the technical documentation, product and manufacturer information, instruction and safety information."*

Companies located in countries outside the EU (e.g., the United States) that wish to sell directly to consumers and other parties in the EU will have to prepare to comply with this new requirement.

ACCIDENT REPORTING DUTY

The GPSR introduces an obligation for manufacturers to report "without undue delay" accidents caused by products they have placed on the market. Accidents are defined as occurrences that result in an individual's death or serious adverse effects on their health and safety. The report must be made to the competent Market Surveillance Authority of the Member State where the accident occurred. Importers and distributors also play an important role since they must report accidents to the manufacturer.

DO YOU HAVE A RECALL PLAN?

The GPSR prescribes that economic operators shall ensure that they have internal processes for product safety in place, allowing them to comply with the

relevant requirements of the GPSR. This typically includes a Corrective and Preventive Action (CAPA) plan. Again, a reservation must be made regarding products subject to specific Union harmonization legislation.

In any case, it is highly recommended to properly safeguard internal processes for product safety within an organization. For example, companies may ask themselves the following:

- Do we have an adequate risk analysis procedure in place?
- Do we have a CAPA procedure in place?
- Do we have proper design validation procedures in place, considering the intended users and use?
- Do we have a proper complaint system in place?
- Does the executive management team take ownership of product compliance and safety within your company?
- Do we have proper procurement procedures and supplier agreements in place?

Companies seeking to enhance their product safety and recall procedures can consider using two ISO standards that are not widely known: ISO 10377, "Consumer product safety – Guidelines for suppliers," and ISO 10393, "Consumer product recall – Guidelines for suppliers." Both large and small businesses can use these standards to evaluate and enhance their safety procedures throughout the product development, production, and distribution phases. These standards emphasize that defects in design and production can be significantly reduced through preventative measures.

RECALLING A PRODUCT? AT LEAST TWO REMEDIES

In the event of a product recall, the GPSR stipulates that consumers should be given a choice of *at least two* of the following remedies: repair, replacement, or a refund. Consumers may only be offered one remedy if the other remedies are impossible or disproportionate. This obviously leads to a discussion about what is meant by "disproportionate."

I often make a comparison with the car industry, where repair seems the only proportionate remedy. We can all understand that, with some exceptions, a replacement or refund for a car that can be repaired

would be disproportionate. Another example of a recall remedy that appears disproportionate is when a regulatory body responsible for market surveillance demands that a manufacturer of premium e-bikes provide consumers with a refund instead of a repair.

Moreover, from a sustainability point of view, repair is probably the better option. With the new EU proposal on the "right to repair" for consumers, it is remarkable that a minimum of two remedies must be offered for recalls, while repair is clearly the most proportionate and sustainable remedy.

A SNAG THAT CAN MAKE THE BURDEN OF A RECALL EVEN BIGGER THAN IT ALREADY IS

EU legislation normally excels with vague texts and open norms, which need further clarification by means of guidelines or that are expected to be further fleshed out by judges in court. It is, therefore, remarkable that some provisions of the GPSR contain very detailed provisions.

On the one hand, that is commendable; on the other hand, it can be very tricky. Here's an example. In Chapter VIII, the GPSR prescribes that, in the event of a recall, the consumer must be instructed to "immediately stop using the affected product." In addition, the GPSR stipulates that, in the event of a recall, the economic operator must collect the unsafe product from the consumer "if it is not portable."

If we take this literally and apply it to dangerous cars, for example, consumers should stop using that car immediately, and the car would be required to be collected from the consumer by the manufacturer (or dealer). The question is whether this is really intended. It would undoubtedly lead to a logistical nightmare and a huge financial burden. Stakeholders, such as trade associations, seem to have overlooked this in the drafting phase of the GPSR.

GPSR vs. SECTORAL LEGISLATION

I contacted the EU Commission to highlight what appears to be a snag in the GPSR. Using cars as an example, their first reaction was that Chapter VIII of the GPSR does not apply to cars since there is already harmonized legislation in place providing certain provisions, including on recalls (EU Regulation 2018/858). However, the question is whether that is a correct assessment.

The EU GPSR is a so-called horizontal regulation that sets out general safety requirements for all consumer products (except if explicitly excluded from its scope) sold in the EU, including motor vehicles. Sectoral car legislation, such as EU Regulation 2018/858 on the approval and market surveillance of motor vehicles and their trailers, provides more specific safety requirements for motor vehicles and their components. However, it does not replace or derogate from the requirements of the GPSR. The sectoral legislation sets out additional requirements for the safety and performance of motor vehicles and their components but does not relieve manufacturers of their obligations under the GPSR. Therefore, any additional obligations under the GPSR would still apply to the car industry alongside the requirements of the sectorial car legislation.

Since the GPSR stipulates more detailed obligations with regard to remedies and recalls, such obligations would apply to all consumer products sold in the European Union that fall within the scope of the GPSR, including motor vehicles. The sectoral car legislation does not exempt motor vehicles from the requirements of the GPSR. Therefore, any additional obligations under the GPSR regarding recalls would be applicable to the car industry, as well as other industries. There are no provisions in Regulation 2018/858 specifically dealing with recall notices (e.g., "stop riding") and remedies (e.g., collecting non-portable products). Hence, we may argue that Chapter VIII is also applicable to cars and other products that are covered by sectoral legislation.

If the Commission intended to exempt products covered by sectoral legislation from the application of Chapter VIII of the GPSR, then Chapter VIII should have been listed in Article 2(1)(b), which outlines the chapters exempted from the scope of the GPSR.

At the time of writing this article, my discussion with the EU Commission was still ongoing. Based on their latest reaction, it seems that they understand my concern. The EU Commission is still in the process of internal discussions regarding this matter. It is anticipated that the EU Commission will release guidelines aimed at assisting industries and other stakeholders in comprehending and applying the GPSR. These guidelines might offer some flexibility and proportionality with regard to the concerns addressed.

However, it is important to note that these guidelines do not carry the same legal weight as the GPSR itself, which is an official law. Consumers or their representative associations have the right to directly reference the explicit text of the GPSR when seeking to address related issues.

IT WILL BE EASIER FOR CONSUMERS TO SUBMIT COMPLAINTS TO AUTHORITIES

The "Union Rapid Information System," previously known as RAPEX, will be modernized to enable more efficient corrective measures to be taken across the EU. One of the aims is to make it easier to inform the public and enable consumers to submit complaints. Manufacturers and their reputation for product quality and safety will, therefore, have increased exposure.

PENALTIES

As a final comment, it is important to realize that the GPSR introduces penalties for those who violate the GPSR. *"Member States shall lay down the rules on penalties applicable to infringements of the GPSR that impose obligations on economic operators and providers of online marketplaces and shall take all measures necessary to ensure that they are implemented in accordance with national law."*

The EU Commission *"should carry out an evaluation of the implementation of the penalties laid down under the GPSR as regards their effectiveness and deterrent effects, and, where appropriate, adopt a legislative proposal in relation to their enforcement."*

CONCLUSION

A new wind is blowing in the EU in the field of product safety. Although the GPSR is not perfect, we can only welcome its arrival. Clearly, if you sell consumer products in the EU, you need to have your product compliance and safety processes in place. Only companies that take product safety seriously will be the winners in a market where product laws and regulations are becoming increasingly complex and demanding.

REDUCED-ORDER MODELING OF PENNES' BIOHEAT EQUATION FOR THERMAL DOSE ANALYSIS

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INTRODUCTION

Present users of wearable devices expect to be able to wear their devices for an entire day to make use of "always-on" functionalities such as step counting, heart-rate monitoring, and sleep quality tracking. This is especially true of wrist wearable devices such as smart watches and fitness trackers. In 2021, a record number of wearable devices were shipped for retail (over 530 million devices), representing a 20% increase in the number of devices shipped in 2020 [1]. As a result, more humans are maintaining longer duration contact with their powered electronic devices than ever before. Due to the necessity of direct contact between a user and a wearable device, some of the heat dissipated by the active elements of the device is transferred to the user's skin. The objective of this study is to establish a methodology for building tractable "reduced order" models that can characterize and forecast the heat transfer between a device and a user and the potential for thermal injury. These reduced-order models can be implemented and solved efficiently in the context, for example, a control algorithm.

For the purposes of this study, heat that is dissipated from a powered device into the body is assumed to be conducted through four distinct tissue layers, as shown in Figure 1. The outermost layer is the epidermis,

Watson can be reached at watsonh@exponent.com.
Colella can be reached at fcolella@exponent.com.

By Harry Alexander James Watson and Francesco Colella

which forms a thin, protective barrier for the deeper layers of tissue. The epidermis is constantly shedding old cells but is maintained by new cell growth at the basal layer, which is the deepest portion of the epidermis. Beneath the basal layer is the dermis, which is a thicker layer of connective tissue that forms the core of the skin. The subcutaneous fat (also called the hypodermis) layer connects the dermis to the underlying inner tissue, composed of e.g., muscle and bone. Each of these tissues is distinct in their geometric, thermal, and physiological properties. In particular, the epidermis is not perfused by blood, while the other three tissues have vasculature. The perfusing blood can either remove or supply heat to these tissues, depending on their temperature. Skin burns are characterized by the depth of tissue that is damaged: first-degree burns damage but do not cause complete necrosis of the epidermis; second-degree burns cause complete necrosis of the epidermis but do not cause permanent damage to the dermis; and third-degree burns cause complete necrosis of the epidermis and significantly damage at least 75% of the dermis [2].

Quantitative thermal damage assessments are based on the temperatures experienced by the tissues and the duration of the thermal exposure. The thermal dose

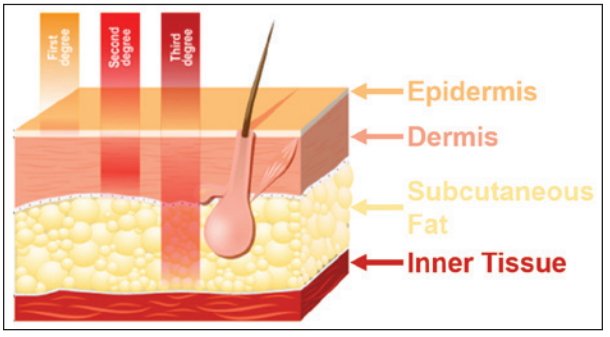

Figure 1: Layers of the skin and classification of skin burns

is often estimated in terms of Cumulative Equivalent Minutes at 43°C (CEM43°C) [3].

Any time-temperature history can be converted to an equivalent duration exposure at 43°C as follows:

$$\mathrm{CEM43°C} \equiv \int R^{43-T(t)}dt, \qquad \text{Eq. 1}$$

where CEM43°C is the cumulative equivalent minutes at 43°C, T is the temperature of the tissue, t is physical time, and R is a piecewise-constant function of temperature given by:

$$R(T) = \begin{cases} 0.25, & T \leq 43°\mathrm{C}, \\ 0.5, & T > 43°\mathrm{C}. \end{cases} \qquad \text{Eq. 2}$$

Threshold values of CEM43°C that can lead to skin tissue damage are available from the literature, many of which have been derived from the work of Henriques and Moritz [4]. In the case of the skin tissues, the CEM43°C value that delineates injurious from non-injurious conditions ranges from approximately 300 to 600 minutes.

GOVERNING EQUATIONS

The heat equation for conduction through a material containing a volumetric heat source, Q, is a partial differential equation (PDE) given by:

$$\rho c_p \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + Q, \qquad \text{Eq. 3}$$

where ρ is the density of the material, c_p is the specific heat of the material, T is the temperature, t is physical time and k is the thermal conductivity of the material. The equation governing the thermal response of a tissue perfused by blood is instead modeled using Pennes' Bioheat Equation as follows [5]:

$$\rho c_p \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) - \beta (T - T_b) + Q_{\text{met}}, \qquad \text{Eq. 4}$$

where β is the "perfusion coefficient" (defined as the product of perfusion rate, blood density, and blood heat capacity), T_b is the temperature of the perfusing blood, and Q_{met} is the metabolic heat generation within the tissue. Note that (4) simplifies to (3) in the case that β = 0 and $Q_{\text{met}} = Q$. These equations can be solved by classical "full space" methods such as the finite difference or finite volume methods; however, these numerical methods become computationally expensive as the sizes of a simulation's temporal and spatial domains grow. In particular, many modern consumer electronics contain a large number of different components and have complex internal geometries.

PROPER ORTHOGONAL DECOMPOSITION

Proper orthogonal decomposition (POD) is a numerical technique for projecting high-dimensional data into a lower-dimensional space that has been widely applied to heat, mass, and momentum transport problems. Given a dataset (e.g., temperature-time data from a thermal simulation), the POD technique finds a set of orthogonal basis vectors that will maximize the total variance of the data when projected onto these coordinates. In the parlance of POD, these orthogonal basis vectors are known as the *spatial modes* of the system.

The central assumption of the reduced-order model is that the temperature field calculated by the full space model can be approximated sufficiently well by a truncated sum of the first *m* POD spatial modes if they are appropriately modulated through time by *temporal coefficients*. This approximation can be written as:

$$T(t, x, y, z) \approx U_0(x, y, z) + \sum_{i=1}^{m} a_i(t) \varphi_i(x, y, z), \qquad \text{Eq. 5}$$

where $a_i(t)$ is the ith temporal coefficient, $\varphi_i(x, y, z)$ is the ith spatial mode, and $U_0(x, y, z)$ is a term that can be included to homogenize or center the temperature field. In particular, the inclusion of the $U_0(x, y, z)$ term is useful for handling non-homogeneous Dirichlet (e.g., specified temperature) boundary conditions.

As suggested by (5), the temperature data from a thermal simulation may initially be stored in the form of an array with entries $T(i, j, k, l)$, with the first index running over the simulation timesteps and the remaining indices running over the spatial coordinates. In order to use the POD technique, this array must first be reshaped into a two-dimensional matrix, T, in which each row contains the temperature at every point in the domain for a particular timestep. Once the data is organized in this way, the POD can be computed by several methods, including Singular Value Decomposition (SVD) or the Method of Snapshots [6]. The Method of Snapshots is the more efficient procedure when the number of timesteps (rows of T) is significantly smaller than the total number of spatial elements (columns of T), which is typically the case for simulation data. In the Method of Snapshots, the correlation matrix, χ, is first formed:

$$\boldsymbol{\chi} \equiv \left(\frac{1}{N_t - 1} \right) \mathbf{T}\mathbf{T}^T, \qquad \text{Eq. 6}$$

where N_t is the number of snapshots. Note that the size of the matrix TT^T is $N_t \times N_t$ and is therefore independent of the number of spatial elements in the simulation. An eigenvalue problem is then solved for the eigenvectors A and the matrix **Ω** with the corresponding eigenvalues on its diagonal:

$$\boldsymbol{\chi}\boldsymbol{\Omega} = \mathbf{A}\boldsymbol{\Omega}. \qquad \text{Eq. 7}$$

The columns of A hold the values of each temporal coefficient at all snapshotted times. A matrix (denoted by **Φ**) containing the spatial modes of the system in its columns can be obtained from $\boldsymbol{\Phi} = \mathbf{T}^T \mathbf{A}$. Typically, each column of **Φ** is then normalized to unit magnitude, in which case the adjusted temporal coefficient values corresponding to the normalized spatial modes are given by the product of **T** and the normalized spatial mode matrix.

The number of POD modes retained in the approximation given by (5) influences the computational requirements of the reduced-order model and the fidelity of the approximation of the physics of the full space problem. Selecting too few POD modes may limit the ability of the reduced-order model to represent true physical phenomena, while retaining too many can introduce spurious dynamics or instability into the reduced-order model.

A common heuristic is to retain modes such that a large fraction of the total variance of the entire mode spectrum is retained (this is sometimes referred to as the "energy" of the POD modes), i.e., choose m such that:

$$\frac{\sum_i^m \lambda_i}{\sum_i^{N_t} \lambda_i} > 1 - \varepsilon_{\text{tol}}, \qquad \text{Eq. 8}$$

where λ_i is the ith eigenvalue of χ when ordered from largest to smallest and ε_{tol} is a user-defined tolerance.

Performing POD on a set of simulation data yields both spatial modes and temporal coefficients; however, these temporal coefficients only represent the dynamics in the original simulation data on which the decomposition was performed. Therefore, the temporal coefficients obtained during the decomposition are not useful in general. Instead, the temporal coefficients corresponding to arbitrary system dynamics can be calculated by projecting the full model onto a subset of the spatial modes, as detailed in the following section. The projection onto m spatial modes reduces the problem of solving the PDEs (3) and (4) to solving a system of m ordinary differential equations for the temporal coefficients.

PROJECTION METHODS

Once a reduced basis has been obtained from POD, the full physical model must be projected onto this low-dimensional space to form the ROM. There are two classes of methods that can be used to perform this projection: *intrusive* and *non-intrusive* methods. Intrusive methods require the modeler to know the differential and algebraic operators of the full space model and explicitly form their counterparts in the reduced space. In non-intrusive methods, the operators

for the reduced order model are inferred directly from the same simulation data that was decomposed to find the POD modes.

Intrusive Projection of Pennes' Bioheat Equation

The most common intrusive projection method used with POD-based ROMs is Galerkin's method of weighted residuals. In this method, the approximation of the temperature field given by (5) is first substituted into the governing equations. This approximation introduces some error into the model. The method of weighted residuals attempts to minimize this error by requiring that the inner product of the model's residual and a set of weight functions is equal to zero. When using the Galerkin method, these weight functions are taken to be the spatial modes of the system. Applying this methodology, with m spatial modes the original PDE (4) becomes a system of m ODEs:

$$\mathbf{M}\dot{\mathbf{a}}(t) = \mathbf{B}\mathbf{a}(t) + \mathbf{f}(t), \qquad \text{Eq. 9}$$

where $\mathbf{a} \in \mathbb{R}^m$ is the vector of temporal POD coefficients, $\dot{\mathbf{a}} \in \mathbb{R}^m$ is the vector of the time derivatives of a, and the other matrices $\mathbf{M}, \mathbf{B} \in \mathbb{R}^{m\times m}$ and vector $\mathbf{f} \in \mathbb{R}^m$ have elements:

$$\begin{aligned}
M_{ij} &= \int_\Omega \varphi_i \cdot (\rho c_p \varphi_j)\, d\Omega, \\
B_{ij} &= -\int_\Omega (\nabla\varphi_i)^{\mathrm{T}} (k\nabla\varphi_j) + \varphi_i \cdot (\beta\varphi_j)\, d\Omega, \\
f_i &= -\int_\Omega (\nabla\varphi_i)^{\mathrm{T}} (k\nabla U_0) + \varphi_i \cdot (\beta U_0)\, d\Omega, \\
&\quad + \int_\Omega \varphi_i \cdot (\beta T_b + Q_{\mathrm{met}})\, d\Omega \\
&\quad + \int_{\Gamma_D} \varphi_i \cdot (k\nabla\varphi_j)\, d\Gamma_D \\
&\quad + \int_{\Gamma_N} \varphi_i \cdot \mathbf{q}\, d\Gamma_N,
\end{aligned}$$

where Ω represents the spatial domain of the simulation, Γ_D represents the boundary of Ω on which Dirichlet conditions are specified, and Γ_N represents the boundary of Ω on which Neumann conditions are specified (the boundary heat flux is denoted here by q). Note that the heat conduction term was integrated by parts to avoid the need for calculating second derivatives of numerical data. The initial condition for (9) is found by projecting the initial temperature condition $T_0(x, y, z) \equiv T(t = 0, x, y, z)$ onto the spatial modes:

$$a_i^0 \equiv \varphi_i \cdot (T_0 - U_0), \quad \forall i = 1, ..., m. \qquad \text{Eq. 10}$$

The matrices M and B and several terms in the vector f are not time-dependent and can therefore be pre-calculated prior to integrating the ODE system to speed up the solution process. The projection of the heat equation for non-perfuse tissue can also be recovered here by taking β equal to zero and replacing Q_{met} with an arbitrary (possibly time-varying) heat source.

Non-intrusive Projection of Pennes' Bioheat Equation

Noting that Pennes' Bioheat Equation is a linear PDE, the reduced-order model is also assumed to be a linear dynamical system. Therefore, a generic reduced-order model for Pennes' Equation can be written in the form:

$$\dot{\mathbf{a}}(t) = \mathbf{C}\mathbf{a}(t) + \mathbf{D}\mathbf{u}(t), \qquad \text{Eq. 11}$$

where the matrix $\mathbf{C} \in \mathbb{R}^{m\times m}$ is an inferred linear operator for the ODE system and the matrix $\mathbf{D} \in \mathbb{R}^{m\times p}$ is an inferred operator on the input vector $\mathbf{u} \in \mathbb{R}^p$ to the ODE system. In the context of the examples studied in this article, the vector **u** will contain a constant term, any time-varying boundary fluxes, and any the time-varying heat sources.

As shown by Peherstorfer and Wilcox [7], the matrices **C** and **D** can be obtained by fitting of the dynamics of a full space thermal simulation to the model given by (11). Given the values of m temporal coefficients through time (e.g., those corresponding to the first m spatial modes that were obtained by performing POD on the original simulation data), their time derivatives (estimated by e.g., numerical differencing), and the vector u(t) that was used to perform the simulation, the matrices C and D in (11) can be directly estimated by solving an ordinary least squares problem.

THERMAL DOSE MODELING WITH ROMS

The goal of the modeling in this article is to solve for the thermal dose received from a powered wearable device by the skin, which requires solution of the PDEs (3) and (4) in the device and the skin. The

projection of the governing PDEs onto a reduced space spanned by a set of POD modes yields a simple ODE system that can be solved more efficiently than the full model. The suggested workflow to solve (3) and (4) and calculate (and validate) the thermal dose received by the skin is as follows:

1. Perform a representative training simulation using a full-space model to obtain $T(t, x, y, z)$ data.
2. Perform POD (e.g., using the Method of Snapshots [6]) on the temperature data to extract the spatial modes.
3. Choose the dimensionality m of the reduced space (e.g., according to the criteria (8) and retain the m spatial modes with the largest eigenvalues.
4. Compute time-independent terms in the matrices and vectors of either (9) or (11) in the m-dimensional reduced space.
5. Choose new dynamics for time-varying source and boundary terms and a new simulation duration.
6. Integrate (9) or (11) using an ODE solver, such as `ode15s` in Matlab, updating time-dependent source and boundary terms as needed at each timestep.
7. Reconstruct the temperature field from the spatial modes and the temporal coefficients using (5).
8. (For validation) Perform an additional full-space simulation to verify the accuracy of the ROM temperature field.

Once the long duration simulation is complete, the CEM43°C value for the exposure can be calculated from (1) and compared to threshold values for the skin tissues.

ILLUSTRATIVE EXAMPLE

This example considers a long-duration (8-hour) one-dimensional transient simulation of a powered device in contact with the skin. The device and skin are modeled as a multilayered medium with the materials and their respective thicknesses given in Table 1 on page 30, listed in order from outermost to innermost layer. In the unmodeled spatial dimensions, the device is assumed to be 2.5 cm by 2.5 cm in size.

There are two heat generating components within the device: the chip and the battery. For the purposes of this illustrative example, the heat generated (in Watts)

by these components over eight hours of continuous use were given by (12) and (13):

$$Q_{\text{chip}}(t) = 0.08 - 0.04\left(\frac{2}{\pi}\right)\text{atan}\left(\cot\left(\frac{\pi t}{7200}\right)\right), \quad \text{Eq. 12}$$

$$Q_{\text{batt}}(t) = 0.07 + (10^{-6}t + 0.03)\text{sgn}\left(\cos\left(\frac{\pi t}{5000}\right)\right). \quad \text{Eq. 13}$$

These power profiles are plotted in Figure 2, expressed as an equivalent heat flux based on the assumed cross-sectional area (6.25×10^{-4}m^2) of the device.

The outermost glass layer of the device was assumed to be in contact with ambient temperature air at all times. The boundary condition at this surface was a convective heat transfer with a constant heat transfer coefficient of 5 W/m^2-K and a time-varying ambient temperature profile, T_{amb}, given by:

$$T_{\text{amb}}(t) = 20 + 10\sin\left(\frac{\pi t}{28800}\right). \quad \text{Eq. 14}$$

The boundary deep within the skin at the end of the modeled inner tissue was represented by constant temperature conditions at the temperature of the blood within the perfuse tissue. The temperature of blood is assumed to be constant at 37°C. The physical properties for the materials and tissues used in this Example are given in Table 2.

All simulations were performed using code written in Matlab R2018b on a Windows laptop with an i7-7600 CPU (2.8 GHz) and 16 GB of RAM.

Following the analysis procedure outlined in the previous section, the first step was to perform a training simulation to generate representative temperature data. In this case, a 15-minute simulation

Material	Thickness (mm)
Glass	1.0
Plastic	1.5
Chip	0.7
PCB	0.8
Battery	5.0
Plastic	1.0
Epidermis	0.4
Dermis	1.5
Subcutaneous	0.6
Inner Tissue	15

Table 1: Device and skin layers and their thicknesses

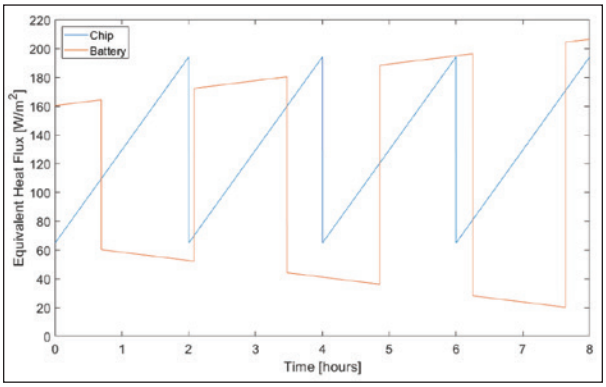

Figure 2: Heat generation profiles within the chip and the battery layers of the device in the example

Layer	Density (kg/m^3)	Specific Heat (J/kg-K)	Conductivity (W/m-K)	Perfusion Rate (1/s)	Heat Gen. (W/m^3)
Glass	2,600	670	1.05	–	–
Plastic	1,050	2,100	0.20	–	–
Chip	2,000	395	15	–	Varies
PCB	4,800	450	3	–	–
Battery	2,200	1,400	0.6	–	Varies
Epidermis	1,200	3,590	0.24	–	–
Dermis	1,200	3,300	0.45	0.00125	370
Subcutaneous Fat	1,000	2,500	0.19	0.00125	370
Inner Tissue	1,000	4,000	0.50	0.00125	370
Blood	1,060	3,770	–	–	–

Table 2: Thermophysical properties for the materials and tissues in the example

was performed using greatly simplified boundary conditions and heat generation profiles. Therefore, instead of the power profiles given in (12) and (13), constant heat generation rates of 0.2 W and 0.6 W were assigned to the chip and battery, respectively. Similarly, a constant ambient temperature of 30°C was modeled instead of the profile given in (14). This training simulation was performed using a finite-volume implementation of the governing equations on a grid of 2,750 elements of equal size (10^{-5} m) and a constant timestep of 0.5 seconds.

Next, the method of snapshots was used to extract the POD modes. The term U_0 in (5) was chosen to be a constant vector with value 37°C at all points in space to homogenize the inner tissue boundary. The fraction of the total variance captured by each of the first 50 modes is shown in Figure 3. As expected, there is rapid decay after the first few POD modes.

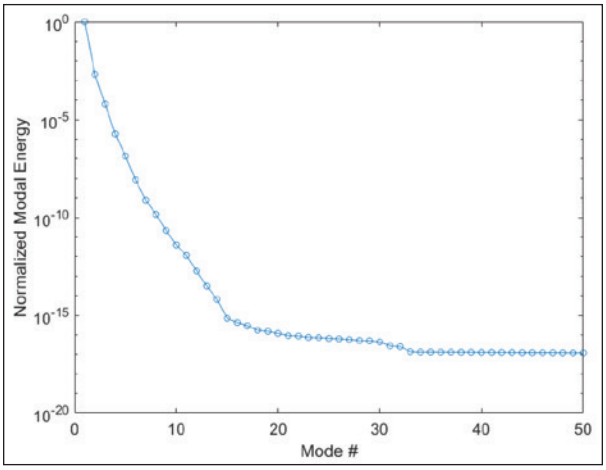

Figure 3: Fraction of the total modal energy captured by each of the first 50 POD spatial modes

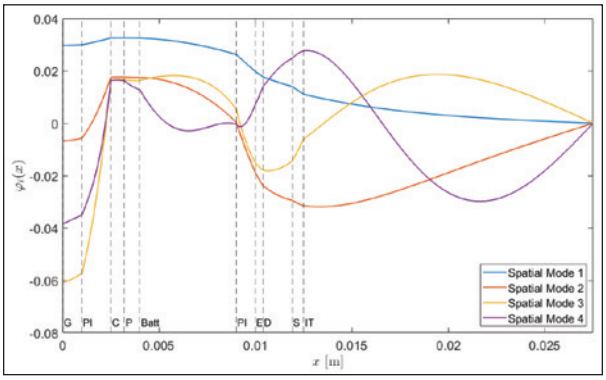

Figure 4: The first four POD spatial modes for the example simulation. The transition between layers is indicated by the dashed lines. G = Glass, Pl = Plastic, C = Chip, P = PCB, Batt = Battery, E = Epidermis, D = Dermis, S = Subcutaneous Fat, and IT = Inner Tissue.

Choosing $\varepsilon_{tol} = 10^{-6}$ in (8), the reduced space is formed using the first four POD modes. These spatial modes are plotted in Figure 4.

Intrusive Projection

An intrusive method of projection was considered first and the matrices in (9) were computed using the Galerkin method. The resulting system of four ODEs was then solved using `ode15s` in Matlab for the full eight-hour duration using the power profiles given in (12) and (13) and the ambient temperature profile given in (14). The solution of the ODE system over this entire time horizon takes approximately 1.5 seconds on the hardware indicated previously. The resulting temperature profiles for the surface of the

device that is in contact with the epidermis and the basal layer are shown in Figure 5.

The full simulation was then performed using the finite volume method for validation. Resolving the full eight-hour profile with the full order method takes approximately 15 seconds, an order of magnitude longer. The CEM43°C profile was calculated using (1) from both the reduced order model temperature field and the full order model temperature field. The profiles are compared in Figure 6. As Figure 6 shows, the two simulations are in excellent agreement. After eight hours of exposure, the predicted CEM43°C values between the two methods differ by only 0.014 minutes (0.04% relative error for the reduced order method).

This simulation result also shows that even though the surface temperature of the device in contact with the skin exceeded 43°C for over 15 minutes, the total thermal dose as measured by CEM43°C is only 38.4 minutes after eight hours, which is far below the threshold for injurious conditions.

Non-intrusive Projection

The thermal dose analysis was also performed using the non-intrusive projection method. When using this method, some additional requirements must be placed on the training simulation to ensure that the dynamics of the model can be learned from the data. In the intrusive method considered previously, the training simulation was performed with a constant ambient temperature and constant power generation in the heat sources. With the non-intrusive method, simple dynamics were included in the training simulation to differentiate the impacts of the two heat sources, the convective boundary condition, and the time-invariant terms in the model.

For this example, the total duration of the training simulation in the non-intrusive case was also increased to 30 minutes. The chip power was set to increase linearly from 0.1 W to 0.2 W over 15 minutes, and then decrease back to 0.1 W over 15 minutes. Similarly, the battery power increased linearly from 0.3 W to 0.6 W over 15 minutes, and then decreased back to 0.3 W over 15 minutes. The ambient temperature varied quadratically between 27.5°C and 32.5°C according to $T_{\text{train}}(t) = 27.5 + 20 \cdot ((t - 900)/1800)^2$.

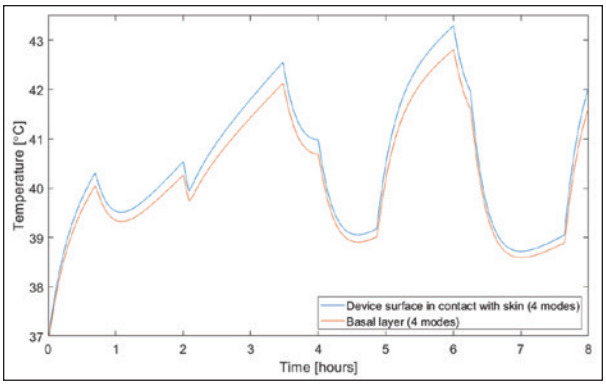

Figure 5: Device surface (in contact with skin) and basal layer temperature profiles simulated with four POD modes using the Galerkin method

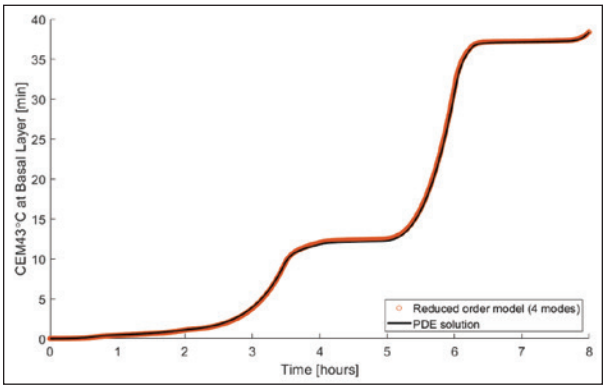

Figure 6: Predicted CEM43°C for the basal layer from the finite volume solution and the solution of the reduced-order model created using the Galerkin method

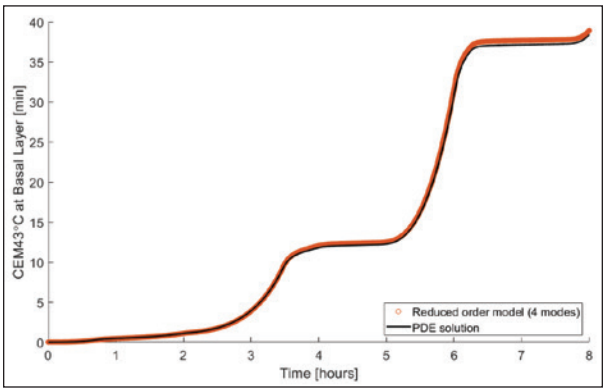

Figure 7: Predicted CEM43°C for the basal layer from the finite volume solution and from the solution of the non-intrusive reduced-order method

Note that these dynamics are still substantially simpler than those in the full duration simulation.

As with the previous training simulation, the POD modes were calculated from the temperature data and a reduced order model was built using the first four spatial modes. The ODE system was constructed by fitting the training simulation data to (11) using linear least squares. The reduced-order model for the eight-hour simulation was then solved as before using `ode15s`, which took approximately 1.1 seconds on the indicated hardware. A comparison of the predicted CEM43°C values from this method and the finite volume method is shown in Figure 7. At the end of the eight-hour simulation, the difference between the predicted CEM43°C value between the two methods was 0.51 minutes (1.3% relative error for the reduced order method).

While the non-intrusive method required a slightly more complex training simulation and gave a marginally less accurate result, it must be emphasized that the construction of the ODE system using this method is trivial. There is no need to perform any numerical integration to construct the matrices for the dynamical system (11). No information about the geometry and physical properties of modeled system is needed after the training simulation data has been obtained.

FUTURE WORK

While the examples shown in this article have focused on a one-dimensional simulation, both the intrusive and non-intrusive methods generalize directly to two and three spatial dimensions. The potential reduction in simulation time is substantial in higher dimensions because the size of the reduced-order model is controlled by the number of modes retained and not the mesh size of the domain. However, practical considerations such as simulation domain size, data storage, and effective training simulations become more challenging in higher dimensions. In future studies, higher dimensional simulations will be performed following the analysis technique established in this article. The implementation of reduced-order models in device control algorithms to understand and forecast thermal shutdown or power throttling requirements for user safety is also an area for future study and development.

CONCLUSIONS

In this article, methods have been developed for evaluating thermal doses received by a user from a powered wearable device. These methods do not require repeatedly finding the solution of a complex PDE model to account for changing boundary conditions or heat sources. Once a ROM has been generated using these methods, it can be solved much more efficiently that the full-space PDE model. The predictions from these ROMs can be highly accurate even when evaluating thermal responses to significantly different or more complex dynamics than those on which they were trained. The solution of this heat transfer problem can therefore be divided into two steps: an "offline" step in which the ROM is first generated, and then an "online" step in which the ROM can be run repeatedly, accurately, and efficiently.

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THE DUTY TO WARN

Do Warnings Make a Product Safe?

There have been several recent articles challenging the efficacy of warnings on products. One of the articles was published on the CNBC website on July 23, 2023, and is titled: "Warning labels in the U.S. seem to be everywhere. Here's why they may be pointless." This article was accompanied by a lengthy video commenting on this subject.[1]

The main points in the article are that people are desensitized to warning labels because they are everywhere, and warnings are the last solution to a safety hazard after design and guarding. Kip Viscusi, a law professor, said in the article that, "There's a tendency to say things are risky [and] slap a warning on it, and that tends to dilute the impact of the other warnings that are out there."

While it is true that some manufacturers add warning labels when they should instead design their product more safely, most manufacturers must make difficult decisions knowing that not everyone reads and follows warnings.

The difficult question arises as to whether a manufacturer can make a safe product by fully relying on a warning or instruction that, if followed, would have prevented the accident. On that point, Bob Adler, the former Acting Chair of the U.S. Consumer Product Safety Commission (CPSC), observed that

Kenneth Ross is a Senior Contributor to *In Compliance Magazine*, and a former partner and now Of Counsel to Bowman and Brooke LLP. He provides legal and practical advice to manufacturers and other product sellers in all areas of product safety, regulatory compliance, and product liability prevention, including risk assessment, design, warnings and instructions, safety management, litigation management, post-sale duties, recalls, dealing with the CPSC, contracts, and document management. Ross can be reached at 952-210-2212 or at kenrossesq@gmail.com. Ken's other articles can be accessed at https://incompliancemag.com/author/kennethross.

By Kenneth Ross

there are differences between a safe product and a product that can be defended in a product liability case. He said:

> *"…. [t]he law is clear: consumers' 'misuse' of a product may serve to defeat or diminish the recovery in a product liability lawsuit, but rarely does it provide a basis for invalidating a product safety rule.*
>
> *"Product safety operates under different assumptions from product liability. Product liability affixes blame. Product safety fixes products. Product safety regulators look to whether an item can be made safe at minimal cost and inconvenience, regardless of a consumer's use or misuse of it."*[2]

Some members of the compliance staff at the CPSC believe that a product that hurts users when they don't follow warnings should be recalled. So, the question is whether a product that has been designed as safely as possible can be sold if the consumer must follow certain warnings and instructions to eliminate any hazards. The reality is that almost every product sold must be properly assembled, installed, used, and maintained for it to be safe and remain safe during its useful life. Thus, assuming that not all users will follow the warnings and instructions that help with safe use, one can only conclude that you can't sell a product where warnings and instructions must be followed. Thus, the only acceptable product is one that has been designed so safely that it can't hurt anyone. That is impossible and not a viable goal.

While adding an adequate warning to your product may result in a defense verdict in a product liability trial, it may not result in a safe product. Therefore, manufacturers need to consider what the law requires and whether it is acceptable from a safety standpoint to rely on a warning rather than designing out the hazard.

First, let's discuss the three kinds of defects and how the law describes the duty to warn.

DEFECTS

Product liability focuses on defects in products that exist at the time of sale. Over the years, there have been three clearly defined kinds of defects.

Manufacturing Defects

A manufacturing defect exists if the product "departs from its intended design even though all possible care was exercised in the preparation and marketing of the product." In other words, even if the manufacturer's quality control was the best in the world, the fact that the product departed from its intended design meant that it had a manufacturing defect. The plaintiff need not prove that the manufacturer was negligent, just that the product was defective. The focus is on the product, not on the conduct of the manufacturer.

Design Defects

There are usually only a handful of products that have manufacturing flaws. And it usually is proven that someone made a mistake or was negligent. It is different with design defects.

The manufacturer intended for the product to be designed and manufactured in a certain way. And the product turned out the way it was designed. The problem was that there was something deficient with the design.

A product is deemed to be defective in design if a foreseeable risk of harm posed by the product "could have been reduced or avoided by the adoption of a reasonable alternative design," and the failure to use this alternative design makes the product not reasonably safe. With this definition, a jury can rule that the product could have been and should have been made safer.

These tests are much more subjective than the test for manufacturing defects, and this subjectivity is the cause of most of the problems in product liability today. Manufacturers cannot easily determine how safe is safe enough and cannot predict how a jury will judge their products based on these tests. It is up to the jury to decide whether the manufacturer was reasonable or should have made a safer product.

The law involving design defects includes the concept that it is better to design out the hazard than just warn or instruct about how to minimize or avoid the hazard. This is because warnings are less effective since people do not always follow them.

Therefore, the question is when you must design out the hazard and when can you rely on a warning that may or may not be effective.

Warnings and Instructions

The third main kind of defect involves inadequacies in warnings and instructions. The definition is similar to that of design defect and says that there is a defect if foreseeable risks of harm posed by the product "could have been reduced or avoided by …reasonable instructions or warnings," and this omission makes the product not reasonably safe.

Again, this is an extremely subjective test that uses negligence principles as a basis for a jury to decide. As with design, it is difficult for a manufacturer to know how far to go to warn and instruct about safety hazards that remain in the product.

Therefore, determining when there is a duty to warn or instruct and how far that duty extends is one of the more difficult questions that needs to be answered by any manufacturer. The jury can easily conclude that an injured plaintiff would not want to be hurt or killed and if the manufacturer had provided adequate warnings and instructions, the plaintiff would have followed them and not been hurt or killed. The fact that an accident occurred can mean, by definition, that it is possible that the warnings and instructions were inadequate.

This makes it easy for the plaintiff to argue that there was a defect in warnings and instructions and that the defect caused the injury. In such cases, it is also sometimes difficult for the manufacturer to explain why its warnings and instructions should not or could not have been better. And it is also easy for the plaintiff to argue that, since not everyone follows warnings, the design should have been safer.

DUTY TO WARN AND INSTRUCT

A manufacturer has a duty to warn where: 1) the product is dangerous; 2) the danger is or should be known by the manufacturer; 3) the danger is present when the product is used in the usual and expected manner; and 4) the danger is not obvious or well known to the user.

Another way to state this is that there is a defect in the warnings when reasonably foreseeable risks of harm posed by the product could have been reduced or avoided by providing reasonable instructions or warnings and that their omission renders the product not reasonably safe.

There is an interrelationship between adequate design and adequate warnings. For this article, we will assume that the manufacturer designed the product as safely as possible and that hazards remain. No matter how safe the design, most products have residual risks and need warnings, either affixed to the product or in the instructions.

Warnings alert users and consumers to the existence and nature of product risks. Instructions affirmatively inform people about how to use and consume products safely. Generally, warnings tend to be negative statements about things not to do or affirmative statements about things to always do. Instructions tend to describe in more detail how to do something safely and correctly.

The safety information on warning labels attached to the product can be a mix of affirmative, negative, or instructional information. The same is true for safety information in instructions that accompany the product. With this combination of information, users can minimize the risk of harm by following the warnings and instructions during use or by choosing not to use the product.

Warnings are usually contained in labels attached to the product or to the packaging or in hang tags that are attached to the product but are thrown away after purchase. Warnings can also be included in instructions that accompany the product and on a company's website and promotional literature.

DETERMINING RISK AND WHETHER TO WARN

During the design phase, manufacturers should do a risk assessment. This assessment identifies possible hazards with using the product and quantifies the probability that this hazard will occur and the severity of the harm that will be suffered if it occurs.

When this is completed and the product's design has been established, it should be relatively easy to identify residual risks which should require a warning. If the risk is not sufficient or not reasonably foreseeable, then a warning may not be necessary. There are no rules under the common law that tell a manufacturer when the risk is too small to warn about or when a risk is reasonably foreseeable. The jury gets to second guess the manufacturer's decision about whether to warn and about the content of the warning.

If the risk is obvious, a warning may not be needed. But this decision must be made carefully because the risk and the probability and severity of harm may not be obvious to some potential product users. Unfortunately, there are very few clear guidelines in this area. This is one reason why many manufacturers warn about many hazards, including remote ones and obvious ones.

However, once a warning is created, the guidelines, standards, and laws are a little more clear. But making this initial decision can be tough and one that should be done with legal counsel or a safety professional who is experienced in warnings.

ADEQUACY OF WARNINGS

Once the decision has been made to warn, the manufacturer needs to determine who to warn, how to warn, and whether the warning is adequate. The common law has said that a warning is legally adequate if:

- It is in a form that could reasonably be expected to catch the attention of a reasonably prudent person in the circumstances of the product's use;
- The content is of such a nature as to be comprehensible to the average user; and
- It conveys a fair indication of the nature and extent of the danger to the mind of a reasonably prudent person.

Despite this definition, terms such as "reasonable user," "fair indication," and "reasonably be expected to catch the attention of the user" make it clear that the jury gets to decide the adequacy of the warnings. Also, previously litigated cases are not particularly helpful because there are so many variables with each hazard, the avoidance procedures, and the experience of the readers of the warnings. Is the reader educated, uneducated, skilled, unskilled, or illiterate, or do they have poor reading skills?

On the positive side, there are U.S. standards (one of them is referred to as ANSI Z535.4) for designing warning labels that, if followed, will result in labels that look uniform. The ANSI standard requires that labels use a signal word – DANGER, WARNING, or CAUTION – and, in some cases, a pictorial or symbol, and then text. And the text is supposed to describe the hazard, the probability of harm, the severity of the harm, and how to avoid the harm.

Beyond that, the ANSI standards do not tell a manufacturer how to determine if a warning is required and what language or picture to put on the label. For that, the manufacturer needs to make some important decisions. Again, because of the significant legal consequences that come from making a bad decision, consulting someone experienced with developing warnings is helpful.

A consultant may not be necessary if you are copying competitors' labels that appear to have been developed by competent people. But it is still a good idea for competent label specialists to review the labels to be sure they apply to your product and are likely to comply with applicable laws and standards and, if followed, would prevent incidents.

As Bob Adler said, a jury might believe that your warnings were adequate and rule in favor of the manufacturer. However, the product might result in accidents because people are not following the warnings. So, is the product safe? And does the manufacturer have a duty to inform the CPSC?

There are many examples of reports to the CPSC and recalls undertaken because accidents were occurring on products that had excellent warnings, but a small number of consumers were ignoring them and injuring themselves or others. Unfortunately,

a CPSC-sponsored recall of a product makes the defense of future litigation a bit more difficult. But, from a safety standpoint, it is hard to argue that a recall or other corrective action, such as a safety education campaign, is not appropriate if consumers are being injured or killed from ignoring the warnings or instructions.

OTHER CONSIDERATIONS

Difficult issues remain that must be decided by the manufacturer. Does a label have to be attached to the product, or can the information be placed in the manual instead? How big should the label be? Where should it be placed? What kind of material should it be made of? How should it be attached? Should any language other than English be on the label? Should the warning on the label be repeated in the instructions?

The manufacturer must anticipate how it will defend itself by arguing that the information was clear and accessible and that the user understood the importance of reading and following the warnings and instructions in the event the product becomes the target of a failure to warn claim.

There are no clear guidelines about what warnings should be placed on the product and which ones should be included in the instructions. The manufacturer must decide, based in part on whether it is necessary for the user to see the warning each time the product is used, or only once, or only periodically when the manual is read or referenced.

In addition, the location of the safety information in the manual is important to enhance the argument that the user must have seen the warnings given the placement and prominence of the information. Usually, manuals of some length include a safety section at the front where safety information and reproductions of the safety labels are included. This safety information may be repeated in the text of the manual in the location where the hazard exists. In short manuals, this section may not need to be included, and the safety information is just in the instructional text.

The manufacturer must consider how to get the manual to the user and make it accessible during the use or maintenance of the product. This cannot always be done, and many times, the warnings on the product will have to stand alone in providing critical safety information during use.

OTHER SAFETY COMMUNICATIONS

Many times, people do not read warnings and instructions until they are having problems with the product or until they hurt themselves. We cannot make people read safety communications. But one reason they do not read them is that they are not very interesting and are often difficult to understand.

So, when considering safety information, we should think about other ways to communicate in a more interesting and informative way. Instructional or safety videos, posters, and web-based interactive safety training may be important to supplement the written material. The technology is available to create such materials, and the cost is not that significant. Manufacturers should consider going beyond written safety communications to adequately communicate the message.

CONCLUSION

This area of product liability law is dangerous because it is so easy for a plaintiff to argue that the manufacturer should have added a few more words, and the accident would not have happened. As a result, creating new warnings and instructions (or updating your current warnings and instructions) should not be done without first obtaining assistance from legal counsel or other warnings consultants who know how to design and produce labels and manuals that comply with any applicable laws and standards and that are likely to be followed by most of the users.

Complying with the duty to warn and instruct in the United States and in foreign countries is not easy. The manufacturer must seriously undertake an effort to do so, both for the safety of the product and to enhance the ability to sell the product both here and abroad.

ENDNOTES

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PRODUCT Showcase

CORRELATION BETWEEN INSERTION LOSS AND INPUT IMPEDANCE OF EMC FILTERS

Part 2: π and T Filters

By Bogdan Adamczyk and Jake Timmerman

This is the second of a three-article series devoted to the correlation between the insertion loss and input impedance of passive EMC filters. In the first article, [1], *LC* and *CL* filters were discussed. This article focuses on *π* and *T* filters. Analysis, simulation, and measurement results show that the frequencies at which the insertion losses of these filters are equal are the same frequencies at which the input impedances are equal. These frequencies define the regions where one filter configuration outperforms the other (with respect to the insertion loss). To determine these regions analytically, we compare the input impedances of the two filters. The next article will focus on cascaded *LC* and *CL* configurations.

INPUT IMPEDANCE TO THE π FILTER

The input impedance, $\hat{Z}_{IN}$, to the π filter is calculated from the circuit shown in Figure 1.

The equivalent impedance of the parallel *RC* configuration is

$$R \left\| \frac{1}{sC} = \frac{R(1/sC)}{R+1/sC} = \frac{R}{sRC+1} \right. \quad (1)$$

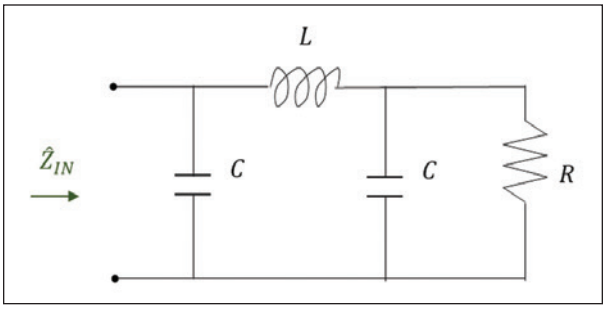

Figure 1: Input impedance to the π filter

Dr. Bogdan Adamczyk is professor and director of the EMC Center at Grand Valley State University (http://www.gvsu.edu/emccenter) where he performs EMC educational research and regularly teaches EMC certificate courses for industry. He is an iNARTE certified EMC Master Design Engineer. He is the author of the textbook "Foundations of Electromagnetic Compatibility with Practical Applications" (Wiley, 2017) and the upcoming textbook "Principles of Electromagnetic Compatibility: Laboratory Exercises and Lectures" (Wiley, 2024). He has been writing this column since January 2017. He can be reached at adamczyb@gvsu.edu.

Jake Timmerman is an EMC Engineer at E3 Compliance, which specializes in EMC & SIPI design, simulation, pre-compliance testing, and diagnostics. He received his B.S.E in Electrical Engineering from Grand Valley State University. Jake participates in the industrial collaboration with GVSU at the EMC Center. He can be reached at jacob.timmerman@e3compliance.com.

This impedance is in series with the impedance of the inductor

$$sL + \frac{R}{sRC+1} = \frac{sL(sRC+1)+R}{sRC+1} = \frac{s^2LRC+sL+R}{sRC+1} \quad (2)$$

which, in turn, is parallel with the impedance of the capacitor. Thus, the input impedance to the filter is

$$\hat{Z}_{IN}(s) = \left(\frac{1}{sC}\right) \left\| \left(\frac{s^2LRC+sL+R}{sRC+1}\right) \right. \quad (3)$$

or [2],

$$\hat{Z}_{IN}(s) = \frac{s^2LRC+sL+R}{s^3LRC^2+s^2LC+s2RC+1} \quad (4)$$

or, in terms of the frequency

$$\hat{Z}_{IN}(j\omega) = \frac{(R-\omega^2LRC)+j\omega L}{(1-\omega^2LC)+j(\omega 2RC-\omega^3LRC^2)} \quad (5)$$

The magnitude of the input impedance is

$$Z_{IN} = \frac{\sqrt{(R-\omega^2 LRC)^2+(\omega L)^2}}{\sqrt{(1-\omega^2 LC)^2+(\omega 2RC-\omega^3 LRC^2)^2}} \quad (6)$$

INPUT IMPEDANCE TO THE *T* FILTER

The input impedance, $\hat{Z}_{IN}$, to the *T* filter is calculated from the circuit shown in Figure 2.

The equivalent impedance of resistor/inductor in parallel with the capacitor is

$$(sL+R)\left\|\frac{1}{sC}\right. = \frac{(sL+R)(1/sC)}{\mathrm{sL+R+}{}^{1}/_{sC}} = \frac{sL+R}{s^2LC+sRC+1} \quad (7)$$

Thus, the input impedance to the filter is

$$\hat{Z}_{IN}(s) = sL + \frac{sL+R}{s^2LC+sRC+1} \quad (8)$$

or, [2],

$$\hat{Z}_{IN}(s) = \frac{s^3L^2C+s^2LRC+s2L+R}{s^2LC+sRC+1} \quad (9)$$

or, in terms of the frequency

$$\hat{Z}_{IN}(j\omega) = \frac{(R-\omega^2 LRC)+j(\omega 2L-\omega^3 L^2 C)}{(1-\omega^2 LC)+j\omega RC} \quad (10)$$

The magnitude of the input impedance is

$$Z_{IN} = \frac{\sqrt{(R-\omega^2 LRC)^2+(\omega 2L-\omega^3 L^2 C)^2}}{\sqrt{(1-\omega^2 LC)^2+(\omega RC)^2}} \quad (11)$$

π FILTER VS. *T* FILTER – INPUT IMPEDANCE – SIMULATIONS AND CALCULATIONS

Let's look at the input impedances of the two filters. The simulation circuit for this comparison is shown in Figure 3.

The input impedances of the two filter configurations are shown in Figure 4.

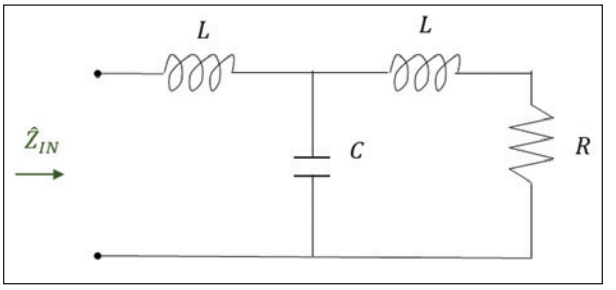

Figure 2: Input impedance to the *T* filter

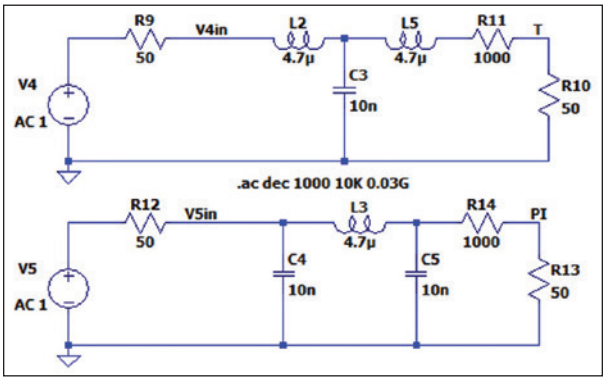

Figure 3: Simulation circuit for comparison of input impedances

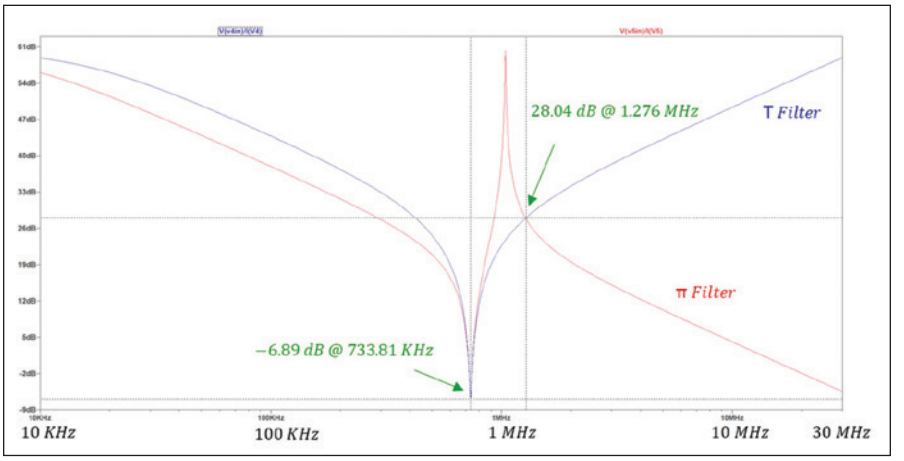

Figure 4: Simulation results: Input impedance – π filter vs *T* filter

Note that the two input impedances are equal at two frequencies: 733.81 kHz and 1.276 MHz.

Next, let's calculate the frequency at which the input impedances of the two filters are equal. Equating the expressions in equations (6) and (11) produces

$$\frac{\sqrt{(R-\omega^2 LRC)^2+(\omega L)^2}}{\sqrt{(1-\omega^2 LC)^2+(\omega 2RC-\omega^3 LRC^2)^2}} = \frac{\sqrt{(R-\omega^2 LRC)^2+(\omega 2L-\omega^3 L^2 C)^2}}{\sqrt{(1-\omega^2 LC)^2+(\omega RC)^2}} \quad (12)$$

This equation can be solved for ω, [2], resulting in

$$\omega_1 = \sqrt{\frac{1}{LC}} \quad (13a)$$

$$\omega_2 = \sqrt{\frac{3}{LC}} \quad (13b)$$

The corresponding frequencies in Hertz are

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} = \frac{1}{2\pi\sqrt{4.7\times10^{-6}\times10\times10^{-9}}} = 733.98\ kHz \quad (14a)$$

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{3}{LC}} = \frac{\sqrt{3}}{2\pi\sqrt{4.7\times10^{-6}\times10\times10^{-9}}} = 1.271\ MHz \quad (14b)$$

which are consistent with the values obtained from the simulation in Figure 4.

π FILTER VS. *T* FILTER – INSERTION LOSS – SIMULATIONS AND MEASUREMENTS

Figure 5 shows the simulation circuit used for the comparison of insertion losses, [3].

The simulation results are shown in Figure 6.

At 734 kHz and 1.27 MHz, the insertion losses of the two filters are equal. These are the same frequencies at which the input impedances of the two filters were equal!

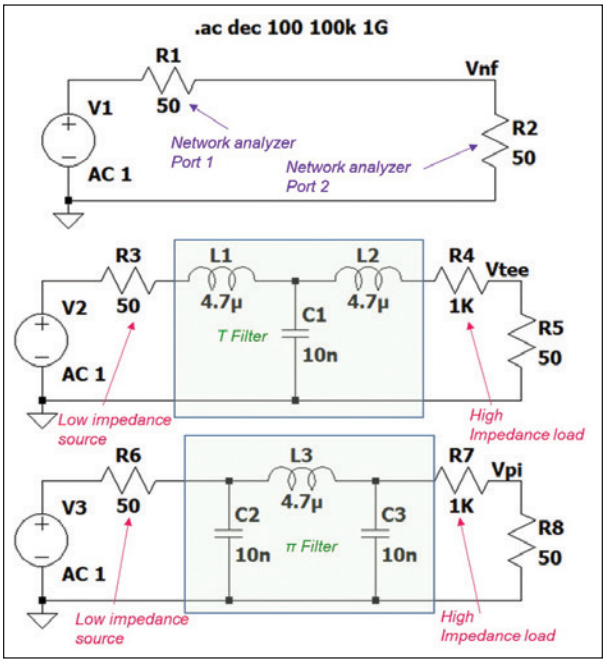

Figure 5: Simulation circuit for comparison of insertion losses

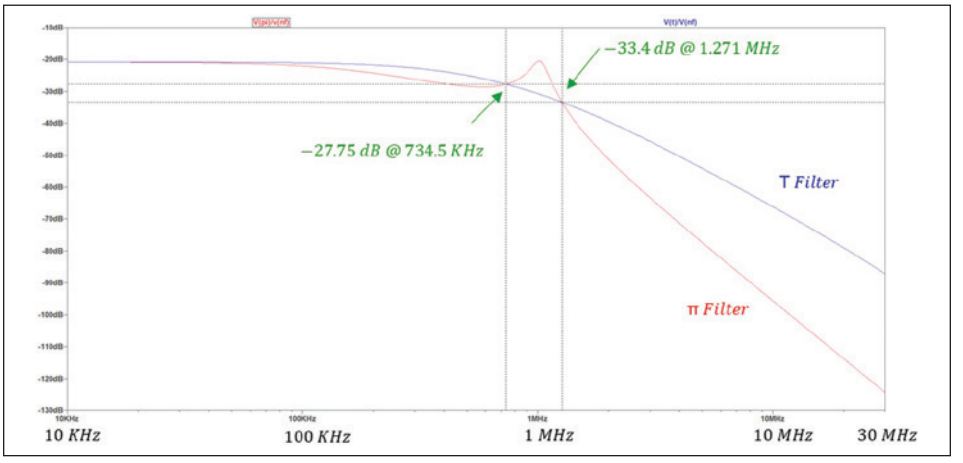

Figure 6: Simulation results: Insertion loss – π filter vs. *T* filter

Note that up to the frequency of 734 kHz, the insertion loss of an π filter is larger than that of the *T* filter. Between the frequencies of 734 kHz and 1.27 MHz, the insertion loss of the *T* filter is larger. Beyond the frequency of 1.27 MHz, the insertion loss of the π filter is again larger.

Again, [1], we have arrived at a very important observation: once the filter components values *L* and *C* are chosen, we can determine the frequencies at which the insertion losses of π and *T* filters are equal. These are the frequencies at which the input impedances are equal, given by Equations 14a and 14b.

To verify the simulation results of the insertion loss, the measurement setup shown in Figure 7 was used. The measurement results are shown in Figure 8.

Note that the measurement results agree with the calculated and simulated results.

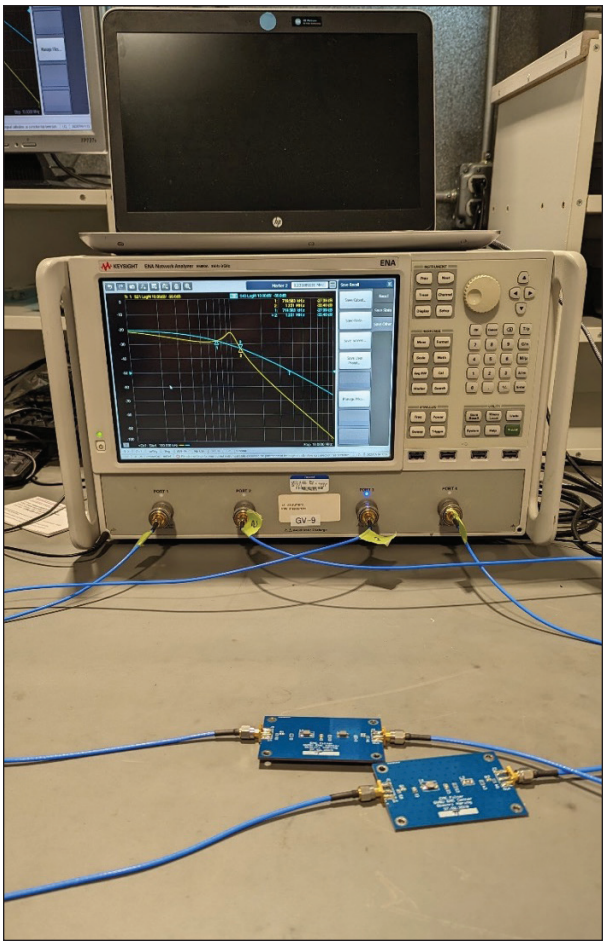

Figure 7: Measurement setup: Insertion loss – π filter vs. *T* filter

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3. Bogdan Adamczyk and Brian Gilbert, "EMC Filters Comparison Part II: π and *T* Filters," *In Compliance Magazine*, January 2020.

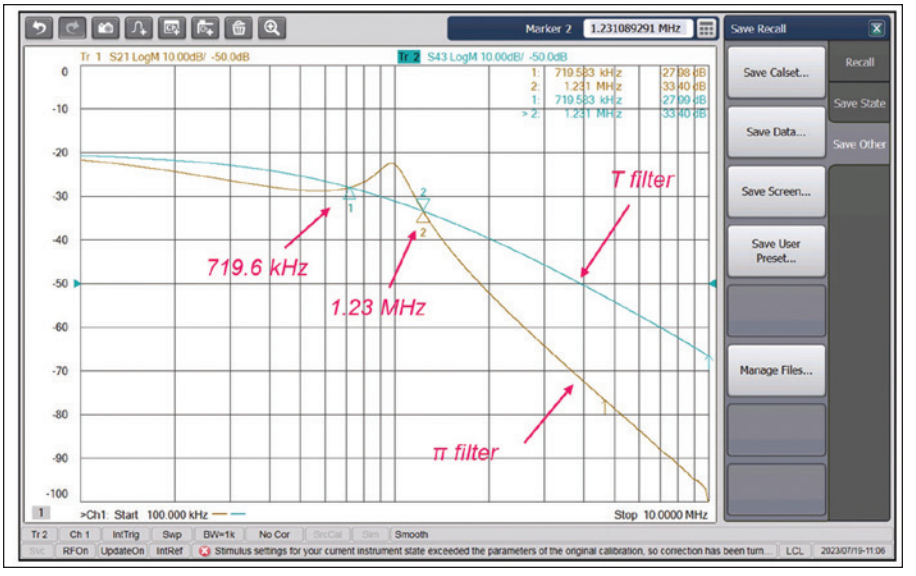

Figure 8: Measurement results: Insertion loss – π filter vs. *T* filter

UNDERSTANDING EMBEDDED ON-CHIP ESD DETECTION, PART 1

By Jeffrey C. Dunnihoo, on behalf of EOS/ESD Association, Inc.

Jeffrey Dunnihoo founded Pragma Design in 1997, specializing in interface design architecture and ESD, EOS, and other transient analysis technologies. He has presented at IEEE EMC Society, the EOS/ESD Association, and ISTFA, and has co-authored a new textbook with other ESD experts on ESD co-design fundamentals, as well as a children's book series on technology and microelectronics. He has also been a contributor to industry groups and standards bodies, such as USB, IEEE 802.11, VESA/DisplayPort, ESD Industry Council, and has served on ESDA working groups.

Founded in 1982, EOS/ESD Association, Inc. is a not for profit, professional organization, dedicated to education and furthering the technology Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, tutorials, and foster the exchange of technical information among its members and others.

INTRODUCTION

Electrostatic Discharge (ESD) poses a significant threat to the reliability and longevity of electronic devices. As integrated circuits (ICs) continue to shrink in size and increase in complexity, they become more susceptible to ESD damage in the factory and soft-errors and upsets in the field, especially wearable and medical devices.[1] (See Figure 1.)

Merely "increasing" ESD protection won't solve all of these problems going forward and may even make some worse. In this 3-part series, we will introduce the growing challenges of soft-upsets and latent ESD damage and outline the benefits of embedded ESD detection as a solution to this problem.

Chip-level ESD designers have been in an arms race to achieve lower clamping voltages and higher clamping currents to prevent factory returns and failure analysis costs for the chip vendor.

Unfortunately, solving the factory equation in isolation creates other headaches for system designers, including more ESD upsets and soft-errors and more constraints in TVS protection selection.

ESD "event detectors" have been used for years in factory environments to identify and remediate ESD discharges during manufacturing. Now design engineers are embedding system-level and on-chip ESD detection technologies into their systems to analyze and recover from both factory and field ESD events.

THE NEED FOR EMBEDDED ESD DETECTION

Complexity of Advanced Integrated Circuits

Over the years, there has been a relentless drive toward smaller, faster, and more power-efficient integrated circuits. This drive has led to the development of advanced semiconductor process nodes with smaller feature sizes, allowing for greater numbers of transistors to be packed onto a single

chip. However, this miniaturization comes with a significant downside: increased sensitivity to ESD events.[2] (See Figure 1.)

As ICs technology nodes become smaller, gate oxides become thinner, metallization narrower, and cross-domain voltage clamping becomes more challenging, ever smaller and smaller electrostatic discharges can now cause catastrophic damage to an IC. Moreover, even the clamped pulses that are survivable can wreak havoc on the system state and coherency and cause soft-errors, upsets, and data loss.

Vulnerability of Modern ICs to ESD Damage and Upset

ESD damage can manifest in various ways, from immediate and catastrophic failures to latent defects that only surface after the device has been in use for some time. Such damage can result in costly warranty claims, recalls, and a tarnished brand reputation for manufacturers.

For the system to pass successfully, it is essential that both the system-level TVS protection and chip-level protection work together effectively to achieve the target system stress levels. The ESD Industry Council introduced the System Efficient ESD Method (SEED) to address this.[3] Pragma Design has implemented the free PESTO analysis tool to help test different protection devices and devices to be protected. But due to soft-upsets, just because the system merely survives does not mean it will pass qualification!

Let's consider four distinct scenarios shown in Figure 2:

1. **Desired Operation**: If the system-level ESD Protection activates and restricts the voltage below the chip-level protection's triggering point, minimal current enters the chip.
2. **Inadequate TVS Design**: Here, the system-level ESD Protection activates, but it restricts the voltage just above the chip-level protection's failure threshold, rendering the chip-level protection ineffective. This mismatch can put the chip's integrity at risk, emphasizing the need for well-matched protection mechanisms between system-level and chip-level components.
3. **Overzealous IC Design Leading to Self-Destruction**: When chip-level protection is "too good" and triggers and prevents the system-level TVS protection from activation, it results in the chip-level protection clamping the entire event. While the robustness of chip-level protection is very good for HBM or CDM pulses, it may still prove insufficient to handle the full system ESD event, leading to a design failure.

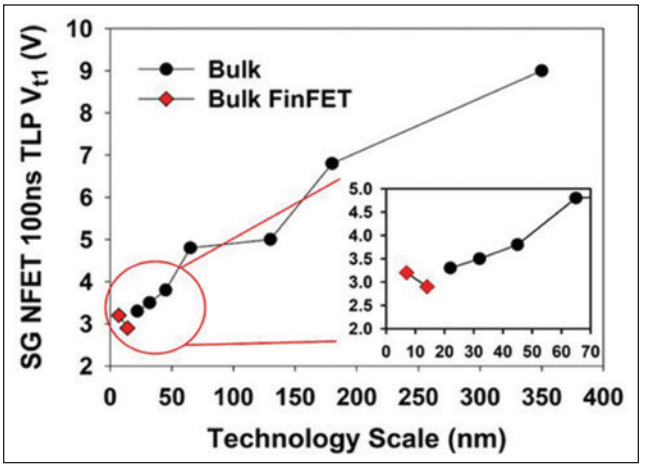

Figure 1: In Compliance 2021 - Advances in CMOS Technologies Leading to Lower CDM Target Levels

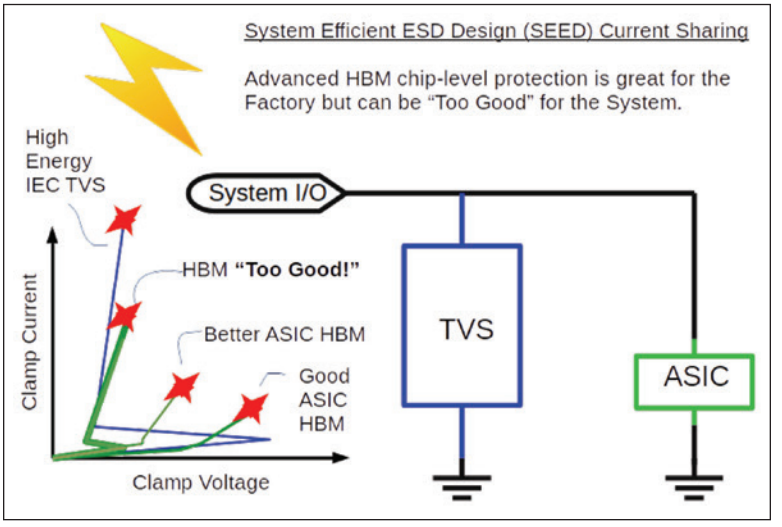

Figure 2: Interactions of I/V characteristics in a "System Efficient ESD Design" (SEED)

4. **Overzealous IC Design Causing Soft Errors and Upsets:** If the chip-level device protection circuit triggers in a way that disrupts VDD-to-VSS voltage, causing a reset or other cross-domain power sequencing issues without causing damage, the system may survive the ESD strike but lose data and functional coherency. In this case, while the on-chip protection may be effective in reducing F/A returns from factory damage, it can also increase the system's susceptibility to glitches and near-field coupled pulses.

Given these growing challenges, there is a growing need for embedded ESD detection solutions that can detect and respond to ESD events that may otherwise be incurable.

EMBEDDED DETECTION TECHNOLOGY

Pragma Design and Certus Semiconductor have introduced real-time, on-chip ESD detection I/O cell design and characterization for standard and custom processes, and many OEM semiconductor manufacturers have also invested in (and incorporated into their design flow) on-chip ESD technology in their products. Unfortunately, as an internal design tool, it may not be advertised in the product specifications. Even though it may be undocumented, ask your chip vendor if they already have or can provide this feature. It can help them with failure analysis, and it can help the system designer optimize their ESD protection budget.[4]

How Embedded Detection Works

Embedded detection technology can be appended to a system, but ideally, it is designed directly into integrated circuits during the chip design phase. It works by recording ESD detection events at all or selected I/O pads and power pins. (See Figure 3.) When an event is detected, embedded detection can respond in various ways, such as triggering protective measures, logging event data, or providing feedback to the device's operating system.

Key components and functionalities of embedded detection technology include:

1. **Detectors**: Embedded detection includes specialized ESD sensors distributed strategically among the chips I/O cells. These sensors are designed to detect electrostatic discharge events and record the events so that they can be read back from registers or via JTAG.
2. **Real-Time Monitoring**: Embedded detection continuously monitors the state of the chip in real-time, and can create software interrupts and logic resets as needed.

3. **Event Classification**: When an ESD event is detected, embedded detection can characterize it by location and effective external threat level.
4. **Response Mechanisms**: Embedded detection can be configured to trigger specific responses to detected events. For example, it can disable affected circuits, redirect signals, or reset components to prevent damage.
5. **Data Logging**: Embedded detection can log event data, allowing designers and manufacturers to analyze and diagnose ESD events that occur during the device's lifetime.

Benefits of Using Embedded Detection

The integration of embedded detection technology into IC designs offers several advantages:

1. **Real-Time Protection**: Embedded detection provides real-time protection against ESD events, reducing the impact of soft-errors and upsets.
2. **Improved Reliability**: By responding to ESD events proactively, embedded detection enhances the reliability and lifespan of electronic devices.
3. **Lower Manufacturing Costs**: Embedded detection reduces the uncertainty of external threats, and can help optimize external protection components, resulting in cost savings during manufacturing.
4. **Performance Optimization**: Embedded detection can be used to optimize the performance of ICs by allowing them to continue operating in the presence of ESD events that would otherwise cause shutdown.
5. **Data Analytics**: The data logged by embedded detection can be invaluable for diagnosing and mitigating ESD-related issues during product development and in the field.

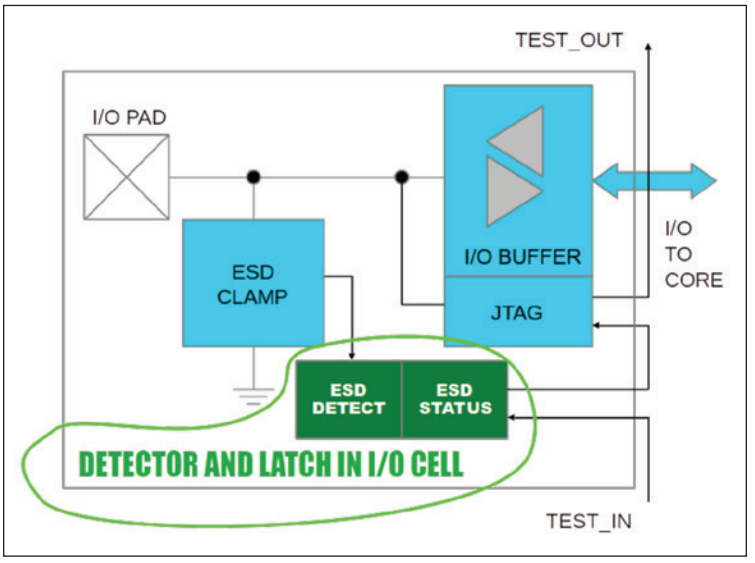

Figure 3: I/O Cell Block diagram with ESD Detection (Green)

CONCLUSION

In Part 1 of this article series, we've explored the critical need for embedded on-chip and system-level ESD detection in the context of modern integrated circuits. The vulnerabilities of advanced ICs to ESD damage have necessitated the development of innovative solutions like embedded detection technology. Embedded detection's real-time monitoring and response capabilities offer a new level of protection and reliability to electronic devices.

In Parts 2 and 3, we will consider the practical aspects of implementing embedded ESD detection and provide guidance on integrating these technologies into semiconductor and system designs and ensuring the robustness of their electronic devices.

ENDNOTES

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SETTING UP A BENCHTOP CONDUCTED EMISSION TEST

By Dr. Min Zhang

As the shift towards electrification gains momentum, an increasing number of companies are venturing into the development of products and systems used in electric vehicles or compact electric aerial vehicles like unmanned drones. These products, often referred to as electric control units (ECUs) in the automotive industry, typically operate on a DC supply voltage of less than 60 V (12V, 24V, and 48 V). Unless you're dealing with high-power conversion, the current draw is usually below 10 A. This makes it quite feasible to establish an affordable benchtop conducted emission setup during the product's research and development phase.

The advantage of having a pre-compliance conducted emission test setup lies in its ability to enable design engineers to identify potential design issues early on, thereby averting costly last-minute modifications. Conducted emission tests can provide reasonably accurate results and also serve as a reliable indicator of radiated emissions, as some of these emissions propagate through cable wiring.

SETTING UP THE BENCHTOP TEST

Fortunately, there are manufacturers that offer low-cost line impedance stability networks (LISNs) characterized up to the 120 MHz range, as illustrated in Figure 1. In this setup, we follow the CISPR 25 standard for EMC testing. Given that the specifics of an EMC test setup often hinge on parasitic elements (like stray capacitance, which affects the common mode current return path), the key elements in this arrangement are:

1. *LISNs ground connection to the test ground plane:* I typically use a galvanized steel plate, readily available at the local tool shop. The LISNs need to be bonded firmly to the plate.

Dr. Min Zhang is the founder and principal EMC consultant of Mach One Design Ltd, a UK-based engineering firm that specializes in EMC consulting, troubleshooting, and training. His in-depth knowledge in power electronics, digital electronics, electric machines, and product design has benefitted companies worldwide. Zhang can be reached at info@mach1desgin.co.uk.

2. *Wiring connection between the device under test (DUT) and the LISNs:* The length should be around 20 cm, in accordance with the standard.
3. *Insulation support:* Its height needs to be 5 cm above the test ground plane, as this dictates the parasitic capacitance between the DUT and the ground.

MINIMIZING THE AMBIENT NOISE

To perform the conducted emission test, we require an electromagnetically quiet environment. Typically, in the R&D workspace, such interference originates from:

1. Noise generated by the benchtop power supply;
2. Noise generated by nearby equipment, which radiates out and couples with the cables of the benchtop power supply and the wiring connection between the DUT and the LISNs; or
3. Local radio transmitter signals coupled to the wiring.

It is generally considered good practice to install a DC filter between the benchtop power supply and the LISNs. Alternatively, depending on the noise characteristics of the supply, it is often possible to mitigate the noise by applying multiple-turn ferrite cores. During my assistance with clients in setting up tests in their offices, I observed that placing a two-turn ferrite core on the mains input cable to the power

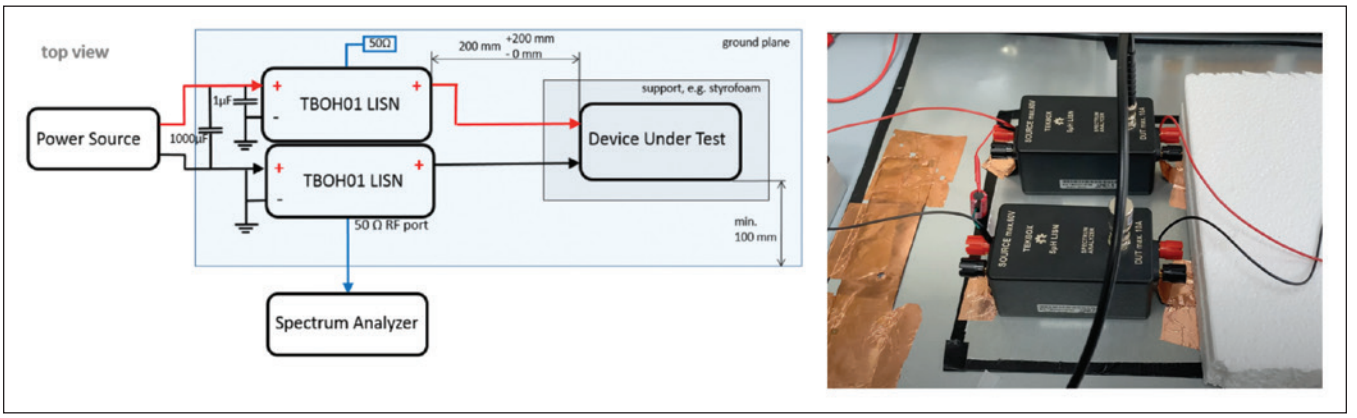

Figure 1: A typical bench LISN set-up for conducted emissions tests

supply also significantly aids in noise suppression. This is particularly effective because switched-mode power supplies generate common-mode noise, so addressing noise from both ends of the power supply is advantageous.

Suppressing signals measured in the FM band due to local radio transmitters is often impossible without an EMC tent or chamber. However, it is worth noting that the characteristics of the radio signal spectrum in this band are distinctive and can be readily identified.

I have a video link that demonstrates how to minimize ambient noise [1].

THE DEVIL OFTEN LIES IN THE DETAILS

Since, in this case, the test is often performed by electronics design engineers rather than skilled EMC engineers, unnoticed mistakes are often made. One of the most commonly seen mistakes is that the test engineer forgets to terminate the LISNs using the 50-ohm termination. This can lead to measurement errors of up to a few dBs.

Another topic I would like to discuss is the 1 µF input capacitor to the LISNs. In certain commercially available LISNs, there's a switch designed for toggling the 1µF input capacitor. This capacitor proves useful in conducted emission tests but must be switched off when conducting any form of transient test. Failing to do so might result in the capacitor inadvertently shorting the transient.

It's worth noting that the LISNs featured in this article do not come equipped with the 1µF input capacitor. The manufacturer recommends that users install it themselves for the correct setup.

UTILIZING A REFERENCE NOISE SOURCE

It's always advantageous to employ a reference noise source when assessing noise levels with a spectrum analyzer. This enables you to check the setup's integrity. In accredited test labs, it's common practice to verify setups with a reference signal source. I came across a Texas Instruments small evaluation board TPS54361EVM-555 [2] with conducted emission test results [3], and I've adopted it as my personal reference source.

REFERENCES

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2. https://www.ti.com/tool/TPS54361EVM-555
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