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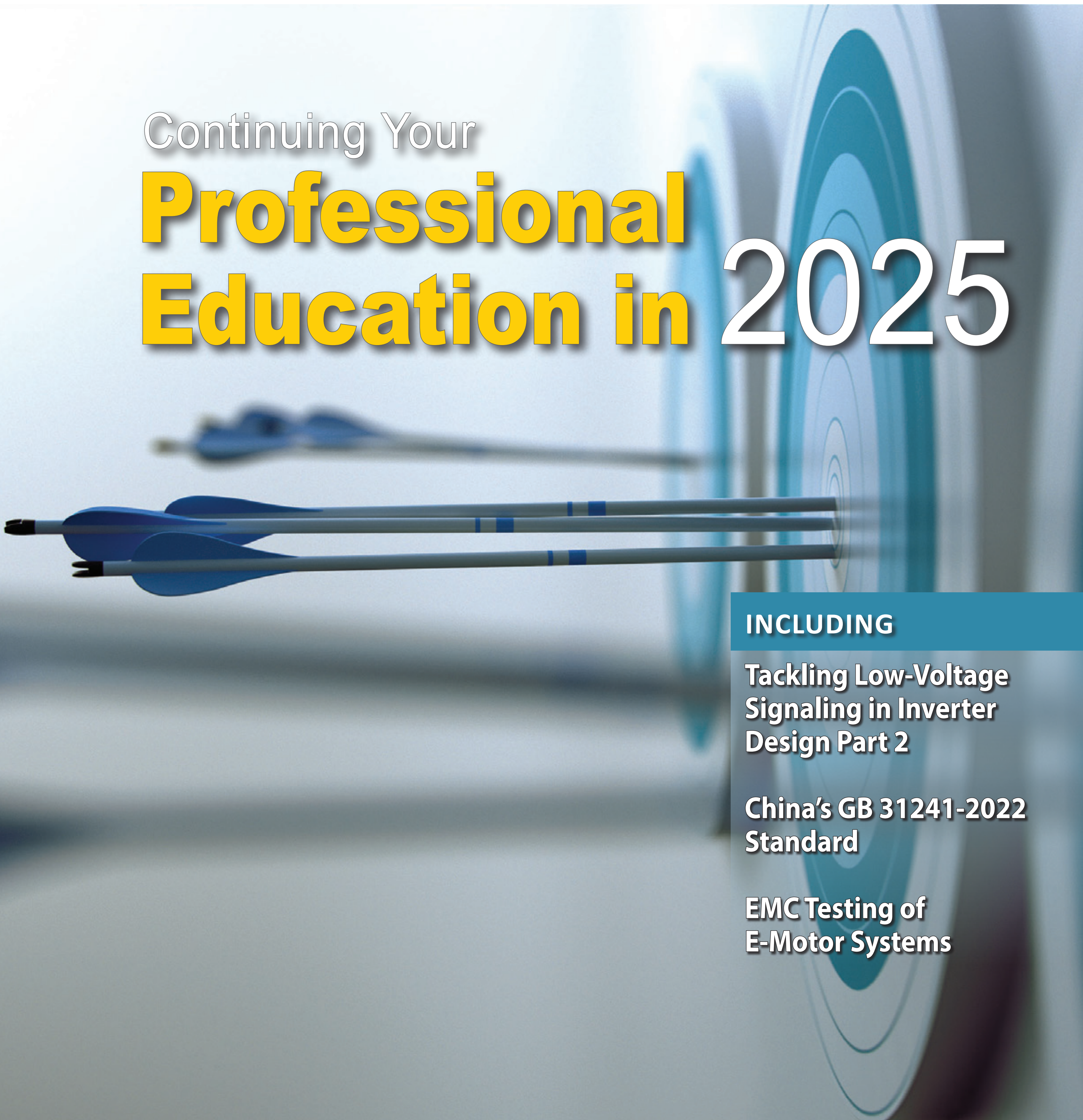

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In ***Product Insights***, Don MacArthur dives deep into practical EMI mitigation challenges, offering solutions for capacitor behavior, ferrite selection, differential probes, and more to optimize designs and advance engineering careers.

Ken Wyatt's ***EMC Bench Notes*** helps engineers identify and resolve EMC issues early in the design cycle using in-house pre-compliance testing tools, enhancing troubleshooting skills and reducing costly testing failures.

Patrick Andre's ***Military and Aerospace EMC*** shares valuable insights into EMC challenges in high-stakes environments like defense, aerospace, and military systems, offering engineers practical solutions and expertise.

Karen Burnham's ***Standards Practice*** explores immunity standards and advanced testing methods, helping engineers navigate compliance challenges in industries like defense, aerospace, and automotive with techniques like reverberation chamber testing.

Kimball Williams' ***Signals and Solutions*** connects the foundational techniques of amateur radio, such as Morse code, to modern EMC engineering, offering fresh perspectives on troubleshooting, testing, and innovation.

Full Collection of Blogs, Posts and Author Bios:
https://incompliancemag.com/expert-insights

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SPECIAL COVERAGE: PRACTICAL ENGINEERING

FEATURE ARTICLES

COLUMNS

DEPARTMENTS

FCC Clarifies Satellite System Spectrum Sharing Rules

The U.S. Federal Communications Commission (FCC) has recently revised its spectrum-sharing rules to support the further deployment of advanced fixed-satellite services and applications.

In a Report and Order, the Commission clarified certain technical details of the degraded throughput methodology used as part of its compatibility analysis of non-geostationary satellite orbit, fixed satellite service (NGSO FSS) licensees. Specifically, the clarification adopts a 3% time-weighted average throughput degradation as a long-term interference protection criterion and a 0.4% absolute increase in link unavailability as a short-term interference protection criterion.

The intent of the changes is to ensure that NGSO FSS licensees authorized in more recent years are compatible with NGSO FSS systems previously licensed by the Commission.

In the same Report and Order, the FCC declined to adopt protection metric modifications or an aggregate limit on interference that were applied in later rounds of NGSO FSS license reviews to licenses reviewed in earlier rounds.

FDA Issues Digital Health and AI Glossary

The U.S. Food and Drug Administration (FDA) has released a helpful glossary of commonly used terms in connection with digital health devices and medical devices that use artificial intelligence (AI) or machine learning.

Titled "FDA Digital Health and Artificial Intelligence Glossary—Educational Resource," the FDA's glossary includes detailed definitions of more than 50 different terms. Of course, it includes several of the more widely-used terms like "Artificial Intelligence," "Digital Twin," and the "Internet of Things." But the glossary also includes several terms probably known only to those immersed in developing and leveraging the relevant technologies, such as "Convolutional Neural Network," "Data Drift," "Explainability," and "Federated Learning."

Each term presented in the glossary also includes links to the sources of the terminology, as well as a list of related terms.

The FDA notes that its Digital Health and Artificial Intelligence Glossary is intended only for educational purposes and does not represent FDA policy nor constitute legally enforceable requirements.

FCC Issues Annual Voice Telephone Services Report

The Federal Communications Commission (FCC) has released its most recent report on voice telephone services available to consumers in the United States.

The report, titled "Voice Telephone Services: Status as of December 31, 2023," clearly shows the significant decline in the use of legacy wireline technologies in favor of mobile wireless technologies. Specifically, as of the end of 2023, wireline technologies accounted for just over 18% of the 471 million retail voice telephone service connections in the U.S., with mobile voice subscriptions equaling nearly 82% of total service connections.

Further, the report highlights the growing trend in the shift to mobile wireless technologies. According to the report, during the three years from 2021 through 2023, mobile voice subscriptions increased at a compound annual growth rate (CAGR) of 3.1%, while interconnect VoIP (wired) subscriptions declined at a CAGR of 1.6% and retail switched access (wired) lines declined at a CAGR of 15.7% year.

The Growing Use of Generative AI Will Generate More E-Waste

Who knew!!!

As our use of artificial intelligence (AI) grows exponentially, researchers and scientists are beginning to sound the alarm about the potential environmental effects linked to AI.

According to a recent article posted to the website of Scientific American magazine, scientists are already estimating that the projected global use of AI by the year 2027 could consume as much electricity as all of the Netherlands. Further, a separate study published in Nature Computational Science predicts that generative AI applications could add between 1.2-5 million metric tons of electronic waste worldwide by the year 2030.

The Scientific American article provides details on some of the stark consequences associated with the use of generative AI. For example, creating two separate images using AI-generative technology can consume as much energy as charging a smartphone. And a single exchange with ChatGPT can lift the temperature of the physical server generating the exchange enough to require the equivalent of a bottle of water to bring the temperature back to a normal level.

To help alleviate the potential environmental impact linked to the use of AI, the article identifies some potential solutions to help minimize the environmental impact of the use of AI. The list includes more efficient chip and AI algorithm design, more regular maintenance and updating of data servers, and finding more ways to refurbish or reuse obsolete hardware components. Researchers project that implementing these and other strategies could reduce e-waste associated with AI by as much as 86%.

PRACTICAL ENGINEERING

How to Become a Great Compliance Engineering Professional

By Don MacArthur

Compliance engineering is a critical field that ensures products meet safety, quality, and regulatory standards. Whether you're just starting your career or looking to enhance your expertise, here are practical steps to become a great compliance engineering professional.

MASTER THE BASICS

Understand safety regulations (including labeling, insulation systems, spacings, dielectric strength, and impulse), electromagnetic compatibility (EMC) (radiated and conducted emissions, and immunity against conducted disturbances, electrostatic discharge, electrical fast transients, surges, damped oscillatory waves, and magnetic fields and so on), environmental factors (such as hot/cold conditions, steady-state humidity, and cyclic humidity), vibration (shock, bump, seismic), packaging (drop testing), and compliance with WEEE, RoHS, and REACH directives.

Familiarize yourself with industry standards such as IEC, UL, CSA, FCC, EN, CISPR, ANSI, and ASTM requirements.

STAY UP-TO-DATE

Regulations evolve, so stay informed about changes. Subscribe to industry newsletters, attend webinars, and participate in relevant forums.

Follow updates from regulatory bodies and standards organizations.

LEARN FROM EXPERIENCE

Work on real-world projects. Practical experience is invaluable.

Collaborate with experienced engineers and other compliance professionals and learn from their insights. Don't just copy what you learn. Make what you learn your own.

ATTENTION TO DETAIL

Compliance engineering involves meticulous documentation. Pay attention to details when creating test plans, reports, and certifications.

Keep accurate records of tests, measurements, and findings.

GET AND STAY ORGANIZED

Organization is a critical skill for any compliance engineering professional. See "The Most Important Skill to Develop as a Compliance Professional" (April 2024, In Compliance website) for more information.

PROBLEM-SOLVING SKILLS

Compliance engineers and other compliance professionals often encounter complex issues. Develop problem-solving skills to troubleshoot and find solutions.

Analyze failures and identify root causes.

TESTING AND VALIDATION

Understand testing methodologies. Learn how to perform tests for EMC, safety, and environmental compliance.

Validate product designs against specifications.

COLLABORATE ACROSS TEAMS

Work closely with design, manufacturing, and quality assurance teams.

Effective communication is key. Learn how to explain compliance requirements so they are easy to understand. This will make it easier to collaborate with others on solutions.

RISK ASSESSMENT

Evaluate risks associated with non-compliance. Prioritize corrective actions.

Understand the impact of non-compliance on product safety and market access.

CONTINUAL LEARNING

Attend workshops, conferences, and training sessions.

Pursue certifications relevant to compliance engineering.

Practice the 5-Hour rule. See "The 5-Hour Rule for Career Advancement and Overall Life Satisfaction" on page 10.

Read continually. See "Practical Engineering: The Importance of Reading and What Every Electronics Engineer Needs to Know About: Training."

ETHICAL CONDUCT

Uphold professional ethics. Compliance professionals play a crucial role in ensuring public safety.

Be transparent, honest, and unbiased in your assessments.

PROJECT MANAGEMENT

Project Management for compliance professionals: Understand how project methodologies empower compliance professionals to proactively address certification challenges and that effective project management practices facilitate clear communication, transparency, and alignment of goals, ensuring timely compliance while minimizing costly errors. Become good at managing compliance engineer projects or projects that have certifications requirements.

LEADERSHIP

Develop leadership skills. Organizations seek individuals who can lead compliance engineering efforts. See "Leadership Best Practices" and "Let's Talk About Leadership in Compliance Engineering."

INTRAPRENEURSHIP

Identify opportunities to support your organization's success by addressing pain points during certification processes. Act like an intrapreneur, and don't be the compliance pain point!

WRITING

Effective communication: Compliance professionals must convey complex technical information to various stakeholders. Clear writing ensures that safety protocols, regulations, and procedures are understood accurately.

Documentation: Writing allows compliance professionals to document processes, test results, and certification efforts. Proper documentation is essential for audits, traceability, and legal compliance.

Risk mitigation: Well-written reports help identify risks and potential issues during compliance projects. By documenting challenges and solutions, compliance professionals can proactively address problems.

Career advancement: Good writing skills enhance job applications, cover letters, and resumes. They demonstrate professionalism and attention to detail, making engineers stand out.

CONCLUSION

Remember, becoming a great compliance engineering professional is a journey. Stay curious, adapt to changes, and contribute to making safer, better products for everyone.

I've tailored these practical steps to help you excel in compliance engineering. If you'd like more specific advice or have additional questions, feel free to ask!

PRODUCT INSIGHTS

The 5-Hour Rule for Career Advancement and Overall Life Satisfaction

By Don MacArthur

Some people aimlessly progress through careers and life, gaining little progress or satisfaction. They are nearly the same place at the end of their careers as they were at the beginning. Lack of progress or satisfaction is most likely caused by not setting clear goals and not knowing how to make smart goals a reality. Once formal education ends, many people invest little time honing and developing new skills. Excuses include not having enough time (we are all busy working 40+ hours per week) or not knowing what to study. If this situation sounds familiar, read on. The solution, the 5-Hour Rule, is a simple concept many successful people use. Benjamin Franklin, one of the United States' most famous founding fathers, developed the 5-hour rule, investing roughly one hour a day, five days a week, in deliberate learning. As Franklin once said, "An investment in knowledge pays the best interest."

WHAT IS THE 5-HOUR RULE?

In short, the 5-Hour rule is a very simple rule that means dedicating at least five hours per week (one hour per day, during the weekday) to developing a new skill or learning something new, something that helps you meet (or get closer to meeting) one or more of your smart goals.

BENEFITS OF PRACTICING THE 5-HOUR RULE

A couple of old sayings go: "The more you learn, the more you'll earn" and "When you stop growing, you start dying." The more you can contribute to your profession and others, the more you will receive back. Once you master any skill, you can create consistency in your life, improve your time-management skills, increase your long-term productivity, and take on new opportunities as they happen.

HOW DO I MAKE THE TIME FOR THE 5-HOUR RULE?

There are two kinds of people in the world: Those who are "early risers," people who do their best work (or study) early in the morning, or those who are the "night owls," the ones who are more inclined to have their best brain activity later in the day or evening. Determine which camp you belong to and when you should fit in an extra hour of study time each day during the week. It's easy for an early riser. They need to get up an hour early each day.

If you have done everything you can and still cannot find the time to devote to learning an hour daily, consider reducing time spent on social media, watching television, or spending your hour on some other nonvalue-added activity. Focus on learning first, and then only when you are ready to take it easy, participate in these other activities.

WHAT SHOULD I LEARN?

The topics are endless, and you will never complete everything you want in a lifetime, so it is best to concentrate your study time on a topic that interests you the most and gets you closer to meeting your career goals. For someone working in compliance, perhaps there is a new standard you want to learn or a better way of performing it (if it is a test standard). How about understanding RoHS, WEEE, or

REACH regulations much better than you do now? Or maybe you want to improve design for product safety, signal integrity, or EMC? How about improving general skills, such as public speaking, writing, programming, or office productivity tools (word processing, spreadsheet, or drawing software packages)? It is up to you, and you get to decide, but the most important thing is getting started and committing to continual learning throughout your career. Set small goals and practice the 5-Hour Rule to achieve them!

FOLLOW-UP ACTIVITIES

Once you have learned something useful, do not just sit it aside and move on. Ruminate on it for a while. Try deliberately practicing what you learned and try to solve problems as they arise. Make what you learned a part of your daily professional life from that point forward.

SUMMARY

Practice the 5-Hour Rule and go to bed each night a little wiser than when you got up that day. Practice the 5-Hour Rule and experience constant growth and constant success. Seamlessly take on new opportunities as they arise. Become the compliance expert you always wanted to be.

REFERENCES: FURTHER READING AND WATCHING

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2. Management Consulted, "5 Hour Rule: A Learner's Success Model" (November 17, 2023).
3. Frank, T., "The 5 Hour Rule."
4. The Art of Improvement, "Why Constant Learners All Embrace the 5-Hour Rule."
5. SUCCESS INSIDER, "Why Successful People All Embrace the 5-Hour Rule."
6. Develop Good Habits, "The 5-Hour Rule: A Simple Technique to Master ANY Skill."
7. Michael Simmons, "Warren Buffett's No. 1 Lifelong Habit: The 5-Hour Rule."
8. Vihan Chelliah, "The 5 Hour Rule | Why Constant Learners Become Successful People."

Q&A WITH THE AUTHOR

In response to our December 2024 article "Obtaining NRTL Approvals," we received thoughtful questions from a reader about the certification process. Here, author Don MacArthur addresses inquiries from Huzaifa Imran, P.Eng.

Q: *Do critical component lists change over time as described by the NRTL, or can we reference critical component lists from legacy projects during product development?*

How does NRTL design a test plan? Do they refer to standard templates (lists of tests) created by NRTL/IEC for both NRTL/C and CB test reports and integrate the relevant tests as part of their testing criteria?

A: Thank you for your inquiries regarding Critical Component Lists and NRTL Test Plan Design. Here is a comprehensive response:

Critical Component Lists

Critical component lists can indeed change over time. According to the NRTL guidelines, safety-critical components must have current recognition or listing. This means that while you can reference critical component lists from legacy projects, it's essential to ensure that the components still meet current standards and certifications. Any changes in component specifications or standards may require re-evaluation and updating of the critical component list.

NRTL Test Plan Design

NRTLs design test plans by referring to standard templates and lists of tests created by organizations like IEC and ANSI. These templates provide a comprehensive set of tests that cover various safety standards. The NRTL integrates these relevant tests into their testing criteria to ensure that products meet the necessary safety requirements. The process typically involves an initial engineering review, a findings report, a modifications assessment, and an official conformity assessment.

Q: *Do manufacturers have access to standard templates and test procedures created by organizations like IEC and ANSI for pre-compliance review?*

A: Yes, manufacturers do have access to standard templates and test procedures created by organizations like the International Electrotechnical Commission (IEC) and the American National Standards Institute (ANSI) for pre-compliance review. These organizations provide various resources, including templates, guidelines, and standards that manufacturers can use to ensure their products meet the necessary requirements before undergoing formal compliance testing.

For example, the IEC offers templates for drafting standards and other publications, which can be used to create documentation that aligns with international standards. Similarly, ANSI provides standards and guidelines for various industries, including electrical power equipment and systems, which manufacturers can refer to during the pre-compliance review process.

CONTINUING YOUR PROFESSIONAL EDUCATION IN 2025

Compiled by the *In Compliance Magazine* Staff

Welcome to 2025! Regardless of where you are in your career, your ongoing efforts to refresh or expand your technical knowledge and skills are essential to your continued professional and personal growth and success. So, as the new year begins, we've once again queried training resources throughout our industry to provide you with an overview of free or affordable solutions to meet your training goals and to help you on your journey to becoming your best self in the new year.

In this article, you'll find sources of compliance-related seminars, workshops, and other types of training, offered live, including both virtual and in-person options, as well as pre-recorded webinars and on-demand training offerings. We've also included a list of industry symposia, conferences, and exhibitions to be held in both the U.S. and around the world.

The information that follows is current as we go to press (early December 2024). But please note that dates for live in-person seminars, workshops, and symposia provided here are subject to change. So check the listed websites for the most up-to-date information on scheduling. Finally, we invite you to submit updates and corrections as well as suggestions for additional listings for our Events section. Please send your comments to us at editor@incompliancemag.com.

LIVE VIRTUAL AND IN-PERSON SEMINARS AND WORKSHOPS

The **American Association for Laboratory Accreditation (A2LA)** WorkPlace Training portal offers both in-person and virtual classroom trainings in both English and Spanish, featuring live instructor-led sessions. Currently, there are more than fifteen separate training offerings, covering areas including international standards, management systems, technical subjects, and soft skills. Course instructors are subject matter experts with many years of professional training experience. Additional details are available at https://a2lawpt.org/courses. (Also see listings under "In-House/Custom Seminars and Workshops" and "Recorded Webinars and On-Demand Training")

Cherry Clough Consultants Ltd. is pleased to announce that the 2025 EMC and Compliance International Conference will be held May 19-21, 2025 in Oxford, United Kingdom. Our annual global gathering of EMC experts, researchers, and engineers offers a dynamic platform for sharing the latest innovations and techniques in EMC, radio engineering, functional safety, electrical safety, and compliance. Featuring keynote sessions, workshops, tutorials, and trainings, the Conference covers a broad range of topics, including measurement techniques, design for EMC, troubleshooting, and EMC for platforms, systems, and installations. Join us for three days of insightful discussions, collaboration, and exploration in a city famous for inspiring great minds. We look forward to your participation and to making EMC&CI 2025 a truly memorable event. For more information or to register, go to https://www.emcandci.com.

The **Equipment Reliability Institute** offers several live, in-person public classes throughout the year, including courses on "Military Standard 810 Testing" and "Fundamentals of Random Vibration and Shock Testing." For complete information and 2025 training dates, go to https://equipment-reliability.com and click on "Scheduled Trainings" in the box in the middle of the home page. (Also see listing under "In-House/Custom Seminars and Workshops")

The **EOS/ESD Association, Inc.** offers access to a wide variety of online and in-person educational opportunities throughout the year. These courses and certifications provide ESD professionals with the knowledge, tools, and credentials needed to meet the challenges of ESD in their companies. The Association offers courses at different locations and also during the annual EOS/ESD Symposium. Further, the Association publishes and distributes numerous educational materials on ESD and has pathways built to navigate training and certification programs and levels. For full details, visit the Association's website at https://www.esda.org and click on the links in the boxes on the home page for "Training & Education," "Certification," and "Events." (Also see listings under "Recorded Webinars and On-Demand Training" and "Industry Symposia, Conferences, and Exhibits")

Eurofins York offers in-person classroom compliance training throughout the year at various locations in the United Kingdom. Visit https://www.yorkemc.com/services/training for more information. (Also see listings under "In-House/Custom Seminars and Workshops")

Dr. Bogdan Adamczyk of **Grand Valley State University** (GVSU) will offer his two-day EMC Certificate course for industry on April 24-25, 2025 and on October 2-3, 2025 at the GVSU EMC Center in Grand Rapids, Michigan. Numerous measurements and demonstrations reinforce the course topics. The course is intended for both the practicing professionals and the new engineers entering the field. For additional details, go to https://www.gvsu.edu/emccenter.

The **IEEE EMC Society** offers access to a number of in-person and virtual presentations and webinars on a variety of EMC-related subjects. For more information, go to https://www.emcs.org/virtual-and-webinar-events.html. (Also see listings under "Recorded Webinars and On-Demand Training" and "Industry Symposia, Conferences, and Exhibits")

Intertek offers live virtual and in-person public seminars and workshops throughout the year at various locations in the U.S. and around the world. Additional information is available at the company's "Knowledge and Education" portal at https://www.intertek.com/knowledge-education. (Also see listing under "Recorded Webinars and On-Demand Training")

Dr. Todd Hubing of **LearnEMC** offers a series of live online courses covering EMC topics ranging from fundamentals to advanced design and modeling techniques. Courses include "Printed Circuit Board Design for EMC and Signal Integrity" and "Power Electronics Designs for Electromagnetic Compatibility." For additional details, go to https://learnemc.com.

The **Rohde & Schwarz** Technology Academy offers a comprehensive selection of live virtual and in-person courses on a wide variety of technical subjects dealing with EMC and RF testing and measurement. More information is available at https://www.rohde-schwarz.com/us/knowledge-center/technology-academy/ta-overview_256215.html. (Also see listing under "Recorded Webinars and On-Demand Training")

Silent Solutions will offer several EMC courses during 2025, including "Applying Practical EMI Design and Troubleshooting Techniques," "Advanced PCB Design for EMC & SI," and "Mechanical Design for EMC." For training locations and dates, visit https://www.silent-solutions.com.

TÜV SÜD America offers live virtual public and private training courses and webinars that are enhanced by the real-life experiences of its auditing and testing teams, offering years of experience in the worldwide international standards arena. These courses can help prepare you for the most challenging compliance issues. To see the current offerings, visit the TÜV SÜD Resource Centre at https://www.tuvsud.com/en/resource-centre. (Also see listing under "Recorded Webinars and On-Demand Training")

UL is currently offering live events and seminars, virtual webinars, and other forms of training in the U.S. and locations around the world. The world's most progressive and safety-conscious companies rely on UL's educational programs for the expertise and tools required to design and install safer products, increase efficiency, realize improved speed to market, and advance their approach to prevention and compliance. A current listing of 2025 programs and dates is available at https://www.ul.com/events. (Also see listing under "Recorded Webinars and On-Demand Training")

Washington Laboratories offers a wide variety of hybrid workshops and training sessions through its Washington Laboratories Academy. From Cybersecurity to Radio Regulations and from MIL-STD 461/810 to the Internet of Things, these comprehensive webinars, seminars, and workshops combine in-depth technical information with practical, real-world engineering insights and solutions to meet today's engineering challenges. For more information, go to https://www.wll.com/schedule.

Kenneth Wyatt of **Wyatt Technical Services, LLC** is an independent consultant based in Northern Colorado, specializing in EMC design, troubleshooting, and training services. Specialties include EMC troubleshooting, pre-compliance testing, and design reviews. Visit http://www.emc-seminars.com/index.html. For further information on his public seminar schedule for 2025. (Also see listing under "Recorded Webinars and On-Demand Training")

IN-HOUSE/CUSTOM SEMINARS AND WORKSHOPS

Many experts and training organizations offer standard and/or customized workshops and seminars and workshops on an in-house basis. These training programs offer companies an opportunity to train multiple compliance personnel with a specialized approach designed for their needs. The following is a list of organizations and trainers that offer both virtual and in-person seminars and workshops for in-house presentation.

The **American Association for Laboratory Accreditation (A2LA)** offers customized laboratory staff training on a number of topics. For more information, go to https://www.a2lawpt.org/training, click on the pull-down tab for "Courses" and select "Custom Training." (Also see listings under "Live Virtual and In-Person Public Seminars and Workshops" and "Recorded Webinars and On-Demand Training")

Vladimir Kraz of **BestESD Technical Services** provides customer-oriented classes and workshops on practical aspects of managing EMI, EOS, and ESD within the factory environment, using a results-based approach to provide participants with a fuller understanding of managed parameters. Classes and workshops are conducted on the customer premises and can include hands-on demonstrations and training on actual tools and processes in production. Specifics include overview and compliance with SEMI E.176 standard and current ESDA work on EOS. For additional information, go to https://www.bestesd.com.

The EMC Academy offers an array of workshops and seminars both virtually and in-person. The Academy's extensive training portfolio covers a wide range of topics, and customized or more specialized training is also available. For more information, go to https://www.emcstandards.co.uk.

Equipment Reliability Institute also provides On-site training on a broad range of testing and design topics. For more information, go to https://equipment-reliability.com, and click on "Onsite Training" in the box in the middle of the home page. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

Eurofins York offers customized, in-house training offerings in addition to their comprehensive schedule of public training programs. For additional details on their "bespoke" training options, go to https://www.yorkemc.com/services/training/on-site-training. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

StaticWorx provides in-person and online custom training on electrostatic discharge and anti-static flooring. Sessions help architects and designers learn how to specify ESD flooring and include subjects such as: differentiating between conductive and dissipative floors; meeting ANSI/ESD S20.20 when working with ESD-sensitive electronic parts and assemblies; and meeting DoD standards when handling explosives. The company's "Architects' Workshop" on ESD flooring is an AIA-IDEC accredited course. For additional information, go to https://staticworx.com/anti-static-flooring-basics-idec-accredited-course. (Also see listing under "Recorded Webinars and On-Demand Training")

RECORDED WEBINARS AND ON-DEMAND TRAINING

Your time is valuable, and your schedule doesn't always allow you to participate in live virtual and in-person presentations. But there are plenty of training options that you can take advantage of, right from the comfort of your daily workspace. Many organizations and training experts provide on-demand webinars, as well as books, podcasts, and e-learning programs. Here are a few options to get you started.

The **American Council of Independent Laboratories (ACIL)** hosts an archive of previously recorded webinars that are available on-demand, covering EMC standards, key EMC committee meetings, and other EMC activities. For more information, go to https://www.acil.org and click on the word "On Demand Education" in the box at the top right corner of the page.

The **American Association for Laboratory Accreditation (A2LA)** offers a comprehensive suite of self-paced e-learning options on metrology and calibration through its WorkPlace Training portal. More than thirty different courses providing the equivalent of hundreds of hours of training are currently available, including online training on ISO/IEC 17025 compliance. For more information, go to https://a2lawpt.org/e-learning, and click on "E-Learning" in the bar at the top of the home page. (Also see listings under "Live Virtual and In-Person Public Seminars and Workshops" and "In-House/Custom Seminars and Workshops")

EMC Fast Pass provides comprehensive online training courses and short courses to assist electronic engineers, compliance specialists, and hardware manufacturers design and test products that pass EMC and RF certifications the first time. Course offerings include:

- EMC Design for Compliance: Immunity
- EMC Design for Compliance: Emissions
- Intrinsically Safe (IS) Hardware Design
- FCC Wireless (RF) Pre-Compliance
- EMC Technician Training

Visit https://emcfastpass.com for further information on his public seminar schedule for 2025. (Click on the link in the box "Online Training Courses.")

The **EOS/ESD Association, Inc.**, in addition to its courses and certifications offered at events, has a wide variety of online classes, online certification programs, training videos, and complementary educational resources at https://www.esda.org. Click on the link in the box "Training & Education" on the home page for more information. Complementary ESD videos are available under the heading "ESD Overview" on the home page. (Also see listings under "Live Virtual and In-Person Public Seminars and Workshops" and "Industry Symposia, Conferences, and Exhibits")

ETS-Lindgren offers a number of recorded webinars that are available on-demand covering topics such as EMC testing, wireless/5G testing, automotive testing (including e-motor and autonomous vehicles), ANSC C63® standards updates, and electro-magnetic protection. Additional details about the company's on-demand offerings are available at http://www.ets-lindgren.com/services/education-training. The company's YouTube channel at https://www.youtube.com/@etslindgrenvideo features many educational videos, including the popular mode filtered demonstration of the new EMC test site validation technique proposed for ANSI C63.25.3 (available at https://www.youtube.com/watch?v=42uLkR2uFe8).

The **IEEE EMC Society** also provides access to several on-demand recordings of recent presentations at Society and Chapter events. Further information is available at https://www.emcs.org/virtual-and-webinar-events.html. (Also see listings under "Live Virtual and In-Person Public Seminars and Workshops" and "Industry Symposia, Conferences, and Exhibits")

Intertek's extensive catalog of live and on-demand webinars complements the company's live virtual and in-person training options. Additional information is available at https://www.intertek.com/knowledge-education/webinars. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

Rohde & Schwarz offers a comprehensive selection of webinars, virtual demonstrations, videos, and other virtual learning options covering a wide variety of technical subjects. Learn more by accessing the Rohde & Schwarz Technology Academy at https://www.rohde-schwarz.com/us/knowledge-center/technology-academy/ta-overview_256215.html. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

StaticWorx also offers a collection of nearly 90 brief, on-demand videos about static electricity that have been viewed over 2.5 million times. These videos answer frequently asked questions, explain complex technical terms, help you understand static-control flooring, and address problems caused by random static discharge. Visit the company's YouTube channel at https://www.youtube.com/c/staticworx to access their video library. (Also see listing under "In-House/Custom Seminars and Workshops")

TÜV SÜD America also offers on-demand webinars covering various topics in the areas of product safety, EMC, management systems, and competency assessments. To learn more, go to the TÜV SÜD Resource Centre at https://www.tuvsud.com/en/resource-centre?intlnk_group=navigation&intlnk_target=resources&intlnk_origin=mainnavi-resources. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

UL also provides safety- and compliance-related training delivered via its extensive library of on-demand webinars. Topic areas include hazard-based safety engineering, global market access, and global directives, code compliance, conformity assessment, sustainability, responsible sourcing, social auditing, and many more. For additional details, visit https://www.ul.com/events/on-demand-webinars. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

Kenneth Wyatt of **Wyatt Technical Services, LLC** offers several webinar- and video-based trainings. Topics include EMC theory, product design for compliance, PC board design for low EMI, taming wireless self-interference, and benchtop EMC troubleshooting. For more information, visit http://www.emc-seminars.com/index.html. (Also see listing under "Live Virtual and In-Person Public Seminars and Workshops")

INDUSTRY SYMPOSIA, CONFERENCES, AND EXHIBITS

Annual symposia are an excellent resource for extensive technical training, as well as the exchange of new ideas and technical concepts. The benefit of attending these events is that attendees can sample a vast array of workshops quickly and efficiently while connecting with colleagues and professionals with the same interests. (The symposia listed below are planned as live in-person events unless otherwise noted. Please check the listed website for the most current information on dates and locations.)

DesignCon 2025
January 28-30, 2025 – Santa Clara, California (U.S.)
https://designcon.com

EMV 2025
March 25-27, 2025 – Stuttgart, Germany
https://emv.mesago.com/koeln/en.html

EuCAP 2025 – The 19th European Conference on Antennas and Propagation
March 30-April 4, 2025 – Stockholm, Sweden
http://www.eucap2025.org

A2LA Annual Conference 2025 (AnnCon25)
April 6-9, 2025—Dallas, Texas (U.S.)
https://a2la.org/annual_conference

2025 International ESD Workshop (IEW)—Europe
May 12-16, 2025, Zagreb, Croatia
https://www.esda.org/events/2025-international-esd-workshop-iew-europe

2025 IEEE International Symposium on Product Compliance Engineering (ISPCE)
May 13-15, 2025 – San Francisco, California (U.S.)
http://2025.psessymposium.org

2025 International Applied Computational Electromagnetics Society (ACES) Symposium
May 18-21, 2025 – Orlando, Florida (U.S.)
http://www.aces-society.org/conference/Orlando_2025

EMC & Compliance International Exhibition & Workshops
May 19-21, 2025 – Oxford, United Kingdom
https://www.emcandci.com

2025 IEEE International Instrumentation and Measurement Technology Conference (I^{2}MTC)
May 19-22, 2025 – Chemnitz, Germany
http://i2mtc2025.ieee-ims.org

IMS 2025 – IEEE International Microwave Symposium
June 15-20, 2025 – San Francisco, California (U.S.)
https://ims-ieee.org

Sensors Expo & Conference
June 24-26, 2025 – Santa Clara, California (U.S.)
https://www.sensorsexpo.com

2025 IEEE International Symposium on Antennas and Propagation & ITNC-USNC-URSI Radio Science Meeting
July 13-18, 2025 – Ottawa, Canada
https://2025.apsursi.org

2025 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC + SIPI)
August 18-22, 2025 – Raleigh, North Carolina (U.S.)
https://www.emc2025.org

EMC Europe 2025
September 1-5, 2025 – Paris, France
https://premc.org/emceurope2025

47th Annual Electrical Overstress/Electrostatic Discharge Symposium
September 13-18, 2025 – Riverside, California (U.S.)
https://www.esda.org/events/47th-annual-eosesd-symposium-and-exhibits

European Microwave Week 2025
September 21-26, 2025 – Utrecht, The Netherlands
https://www.eumweek.com

The Battery Show 2025, North America
October 6-9, 2025 – Detroit, Michigan (U.S.)
https://thebatteryshow.com

47th Annual Meeting and Symposium of the Antenna Measurement Techniques Association (AMTA)
November 2-7, 2025 – Tucson, Arizona (U.S.)
https://2025.amta.org

IEEE EMC SOCIETY 2025 REGIONAL EVENTS

2025 Chicago IEEE EMC Mini Symposium
May 6, 2025 – Schaumburg, Illinois (U.S.)
http://www.emcchicago.org/sectfiles/events.htm

Southeastern Michigan EMC Fest 2025
May 8, 2025 – Livonia, Michigan (U.S.)
http://www.emcfest.org

2025 Minnesota EMC Event
September 25, 2025 – Bloomington, Minnesota (U.S.)
https://www.mnemcevent.com

We hope this list will help you meet your professional development goals in 2025. Many additional trainings and events will be planned throughout the year, so be sure to check our events calendar at https://incompliancemag.com/calendar to find the most up-to-date information. Another way to brush up on the basics and delve deep into advanced topics is by visiting our online resource center, the *In Compliance* **Electrical Engineering Resource Center (EERC)** at http://incompliancemag.com/eerc.

In the meantime, we hope that the year ahead brings only good health and happiness to you and your loved ones!

TACKLING LOW-VOLTAGE SIGNALING IN INVERTER DESIGN: PART 2

Managing High-Power Inverter Noise to Protect Low-Voltage Signals

In Part 1 of this two-part article (see In Compliance Magazine, December 2024), we discussed the challenges involved in designing, building, and debugging a high-power mixed-signal inverter, and examining common application-specific integrated circuits (ASICs) that work alongside FETs (field effect transistor) and MCUs, focusing on their roles in interfacing and driving. In Part 2, we'll discuss the importance of choosing the correct PCB stack up during component selection and placement, as well as component and layout mitigation strategies.

COMPONENTS FOR MITIGATING COUPLED NOISE

Mitigating the impact of transient signals on inverter systems requires a combination of component-level solutions and effective PCB design practices. Equally important are layout and routing techniques. In the following sections, we'll dive into discussing several component selection strategies a designer can choose early on to protect against these types of failures, and then cover routing and stack-up techniques to minimize noise and interference.

The Schmidt Trigger or Buffer

The primary challenge in interfacing with gate driver ASICs and other components that use a reduced VIO is managing the signal-to-noise ratio, which includes the intended signal, and the noise generated by electrical transients coupled onto the victim trace or the shared reference plane. One effective solution is the use of an external buffer or Schmitt trigger (see Figure 1). These devices, referenced at a higher VIO referenced to VDD, thus offer greater robustness against transients and ground bounce, much like the MCU's output drive circuitry.

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By Christopher James Semanson

Key electrical characteristics to consider include:

- Operating temperature of the buffer since, the warmer the inverter gets due to its proximity to the output stage of the device, the greater the likelihood that the operating point will shift;
- Ensuring that the propagation delay from input to output does not impact the functionality of the drive signal or the communication bus;
- Verifying that the VIH and VIL thresholds are compatible with your gate driver IO voltage and sufficiently high to provide immunity from stray transients; and
- Paying attention to the type of signal being buffered or level shifted. A driven IO signal, such as SPI or a low-side gate drive input, does not require a pullup resistor like I2C.

Additionally, it is crucial to ensure that the buffer is powered and ready at the time of communication and actuation. Also, care must be taken to analyze the power rail and reset values should there be a momentary dropout or power cut of the buffer. Overall, this device is particularly effective, though expensive, in single board designs where space constraints prevent adequate physical separation between victim and aggressor traces.

As for placement, it depends upon the type of crosstalk you're getting since you're looking to utilize the higher VIH/VIL thresholds of the buffer. You generally want to place the component close to the gate driver since any transient signals coupled onto the trace will have a harder time coupling (see Figure 2). Placing it near the MCU can leave the trace as an antenna, which is less effective.

Terminating Components

If your design cannot accommodate the overhead buffer circuitry for noise immunity, the next best strategy is to leverage the inherent capacitance of the trace running

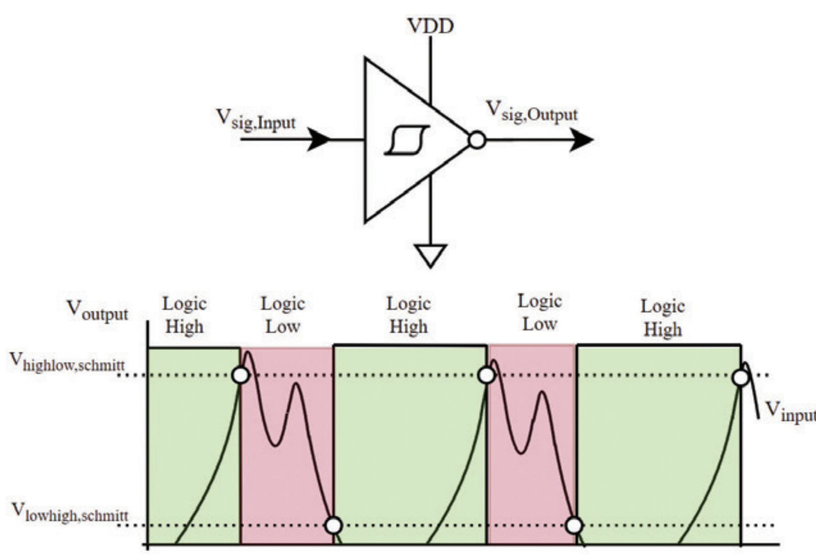

Figure 1: An externally referenced Schmidt trigger and an example signal

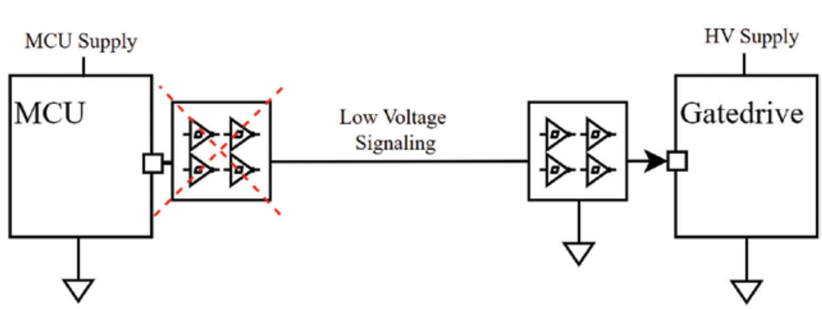

Figure 2: Placement of a Schmidt trigger IC close to the gate drive to buffer gate driver device

from the MCU to the gate driver ASIC. By adding a series termination resistor, you create a small low-pass filter that helps snub transient signals. A common recommendation in early prototype designs is to include the pads for these components and connect them with either a solder bridge or a 0-ohm resistor (see Figure 3).

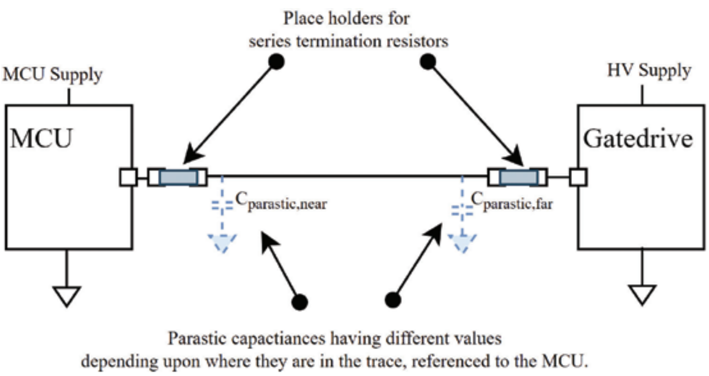

Figure 3: Placeholder for termination resistor on either the near or far end of a low voltage signaling bus

Again, you'll want to use your best judgment in terms of near end (near the MCU) or far end (near the gate drive ASIC, see Figure 4). You'll have more parasitic capacitance the more of the trace you leave and further away it's placed to the ASIC, depending on which component end is driving the pulses.

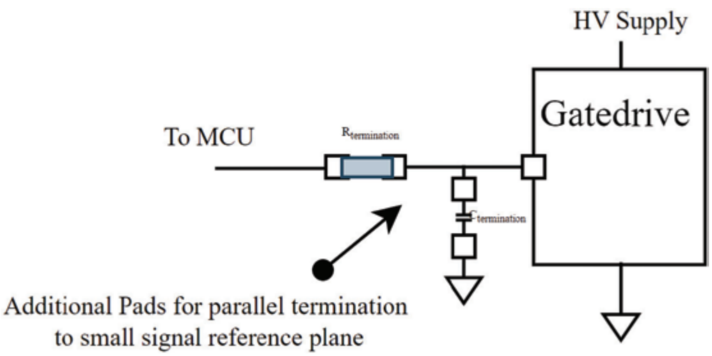

Figure 4: Placeholder for termination resistor and capacitor on either the far end of a low voltage signaling bus

Additionally, adding a small parallel capacitor to ground can enhance the filtering effectiveness, depending on the drive strength of the signal. The key is to add enough capacitance to effectively filter transient glitches without impacting critical factors such as the rise and fall times of the propagating signal. Incorrect communication timing or control could result if these factors are compromised. In communication signaling, setup and hold times, as specified in the ASIC datasheet, are particularly sensitive to these changes.

While managing noise on the victim's side is effective, addressing the high voltage side is equally important. Designers can use two main techniques to protect against transients: snubber circuits and slowing down the edge rate (either through drive strength modifications of the gate drive strength; or a physical resistance in the gate path).

RC Snubber Circuits

Implementing an RC snubber circuit on the high voltage side can mitigate high-frequency ringing during the switching rise and fall time which improves EMI. This can be done using a resistor-capacitor snubber to ground across V_{gs} or decoupling capacitors across V_{ds}. An example is shown in Figure 5.

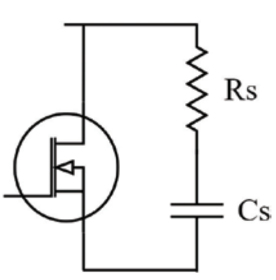

Figure 5: An RC snubber circuit across a power FET used to dissipate oscillation to heat

The snubber circuit is designed to dampen oscillations and absorb the excess energy from switching transients. Typically, the values of the resistor and capacitor are chosen based on the ringing frequency and the impedance of the circuit. A typical procedure might suggest starting with a capacitor value that resonates with the parasitic inductance at the ringing frequency, and then tuning the resistor to critically dampen the oscillation. Note that, while adding snubber circuity (or placeholders for snubbers) is useful, their usage will create power loss.

$$P_{loss} = 2\left(\frac{1}{2}C_S V_{ds}\right) f_{sw}$$

It's typical for a designer to place the snubber structures as close as possible to the switching device to minimize parasitic inductances and capacitances that could negate the snubber's effectiveness, thus increasing the heat dissipated across R_S.

Slowing Down the Rise Time

Slowing the output drive speed by adding a series resistor from the output of the gate driver to the input of the power FET, or modifying the drive strength of the smart ASIC, can also help manage noise. The value of the gate resistor is the ability to select the rise and fall times of the FET gate voltage, thereby reducing the di/dt and dv/dt during switching.

Application notes typically recommend starting with a small resistor (e.g., 10-20 ohms) and adjusting based on performance, both EMI (electromagnetic interference) and efficiency. In addition, the designer can choose the drive strength, usually represented as either percentages (the appropriately named fast/nominal/slow) or in amps.

$$R_{gate} = \frac{\left(\frac{V_{gate}}{I_{gate}}\right)}{\left(\frac{t_{rise}}{t_{fall}}\right)}$$

Snubber circuits and controlling the edge rate are straightforward solutions to incorporate during the design phase by including appropriate pads near the gate drivers and populating them as needed. However, these options have efficiency trade-offs:

- *Increased deadtime*—Slowing down the gate drive signal increases the need for deadtime, resulting in more off-time and reduced efficiency; and
- *Power dissipation*—Snubbing the drive signal to reduce ringing dissipates energy as heat in the resistor-capacitor combination. The power dissipation in the snubber resistor can be significant and must be considered in thermal management planning.

Whether using a more robust solution like a buffer or adding critical components to key areas, component choice and placement can provide essential last-minute solutions.

Next, we'll explore stack up, routing and grounding.

STACK UP

When sitting down to layout the schematic, it's important to keep in mind a list of objectives that the design must accomplish in order to help naturally keep

Example 4 Layer	Component Examples
Power Components, Power Signals, high voltage power plane	Phase Connectors, DC Bus Cap, Power FETs
Reference for Power Components	-
Reference for Small Signal	-
Small Signal Components, low voltage power plane, and signaling	MCU, Communication, Sensing Signals

Example 6 Layer	Component Examples
Power Components, Power Planes, traces and islands for Phases, Reference	Phase Connectors, DC Bus Cap, Power FETs
Reference	-
Small Signal Routing	High Speed Signals if applicable
Small Signal Routing	High Speed Signals if applicable
Reference/Power	-
Small Signal Components, Small Signal Power and Reference Plane	MCU, Sensor interfacing Memory

Example 8 Layer	Component Examples
Power Components, Power Traces, Power Reference, Island for Phases	Phase Connectors, DC Bus Cap, Power FETs
Large Signal Reference Layer	-
Switching signal Routing	
Internal Reference Layer	-
Internal Power Layer	-
Small signal routing	High Frequency Signals
Small Signal Reference Layer	-
Small Signal Components, Small Signal Power and Reference Plane	Low Frequency Signals, MCU, Sensor and Memory Interfacing

Figure 6: Examples of a recommended stack up for a 4-, 6-, and 8-layer board

sensitive nets sufficiently isolated. These objectives are similar to that of a high-speed layout, with the following major differences:

- A complete assembly usually focuses on including as much reference plane as possible to ensure proper heat and to meet rigidity concerns;
- The power levels that the assembly supports on both the input DC bus and the output generally requires "fingers" around each phase connection on exposed layer power planes to support the higher currents necessary; and
- Depending on circuitry needed for communication and logging, the fanouts and low voltage traces are limited to drive traces, CAN or ethernet communication, and sensors.

These last two points specifically can allow the design to focus mostly on impedance continuity, as there should be fewer traces to cut up internal reference planes, and power is generally fed via power planning due to the current amplitudes involved.

With that said, the options to consider in a design include the number of layers and planes, the ordering of those layers, and the spacing between the layers. Considering these design constraints, we can define the following traditional objectives when deciding on a stack up to help shield your sensitive traces from high voltage ones and to help with component placement:

1. A signal layer should always be adjacent to the plane;
2. Signals should be routed adjacent to the plane in which the components are referenced, which often results in the use of two reference planes;
3. When a power plane is used, it should be placed close together to a reference plane;
4. When possible, use reference layers to sandwich traces you want to either shield or keep from radiating; and
5. Using more than one reference plane is very advantageous in design as it provides shielding and low impedance.

In most designs, you will generally see options #2 and #3 difficult to achieve simultaneously. As such, it's recommended to err on the side of multiple dedicated reference planes that are tied together at multiple points vs. a mixed reference and power plane. Nevertheless, combining these objectives and characteristics in a unique inverter design, we can come up with the example stack ups shown in Figure 6.

The recommendations for a four-, six- and eight-layer board shown in Figure 6 help provide a foundation for the designer to start with. In addition to layer designation, the design also can further control coupling by changing the spacing between the various layers.

If the goal is to create tighter signal coupling between adjacent layers of the same signal type, the design then makes the interlayer spacing between these two groups thicker to allow for more isolation. An example of this is shown in Figure 7.

Additionally, if cost allows, a carrier board concept allows for natural isolation between the low voltage and high voltage side of the system, interfaced at a specific header connection (see Figure 8). The added benefit here is that the isolation of low voltage referencing and signal planes are more naturally confined to the carrier board, and it allows you to swap to different power boards. The downside is that the form factor of the design is now a concern and added cost.

Regardless of form factor or stack up you use, we now need to address the next challenge, which is how to best take advantage of these options when planning a design.

The answer to this question is to first identify the component categories, and thus their associated traces, and separate them into high and low voltage. By doing this, we keep a twofold goal in mind, first to keep high-power circulating return currents away from low voltage victim traces and, second to ensure a low impedance return path for those currents, preventing noise voltages from coupling onto victim traces.

This proposed methodology splits signals into small and large signal referencing and routing planes. An example using an earlier diagram is shown in Figure 9 on page 26, where we room or separate the components into high (red) and low voltage signaling (blue).

The signals and their references are described as:

- Low voltage PWM GPIO and communication lines (I2C/SPI), which should be referenced to a plane separate from the "high power" plane, with their traces adjacent to it. Often, you'll see terms like signal ground (s), digital ground (d), or analog ground (a) used to describe these low-voltage references. In general, they should encompass the space between the MCU and associated ASIC components (gate drives).
- Large signal referencing, which generally refers to high side PWM GPIO and their drive signals, should be referenced to a "high power" plane, where schematic symbols and pins refer this to power ground (p).

The goal is to apply the aforementioned rules, reference similar signal types together to the same plane, and then

Figure 7: A stack up with a thicker center, allowing for more isolation and spacing between sections of the stack up

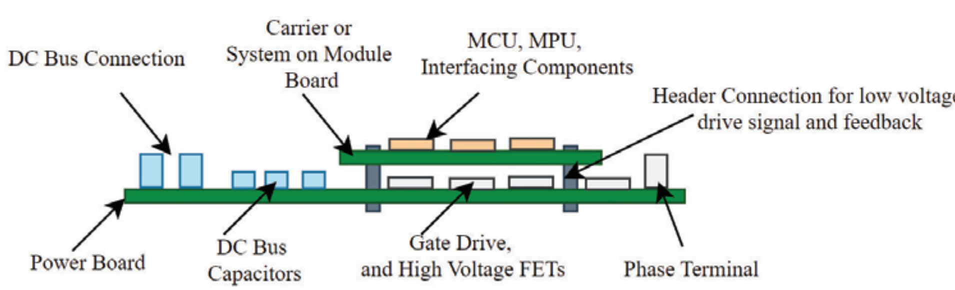

Figure 8: A carrier board interfacing with a power board

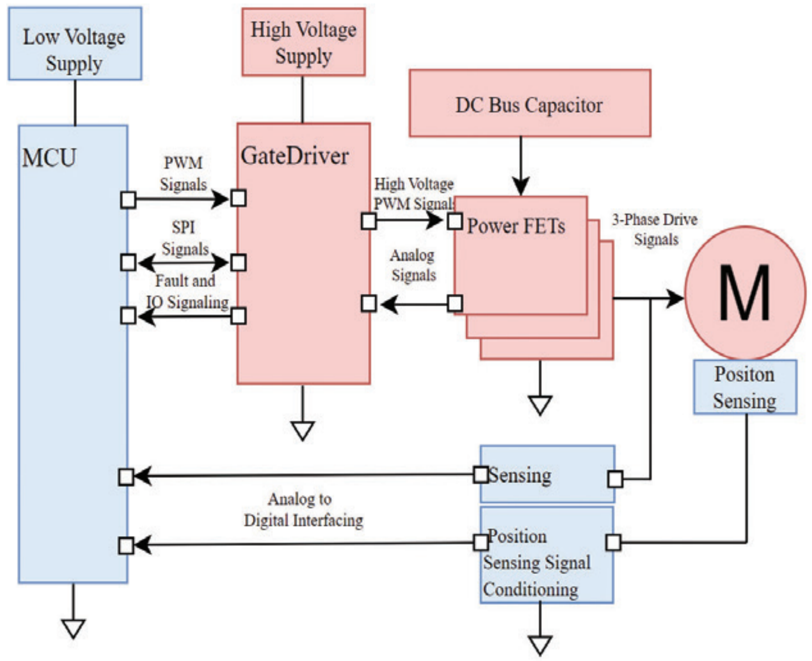

Figure 9: Our earlier inverter system, separated into high- and low-voltage subsystems

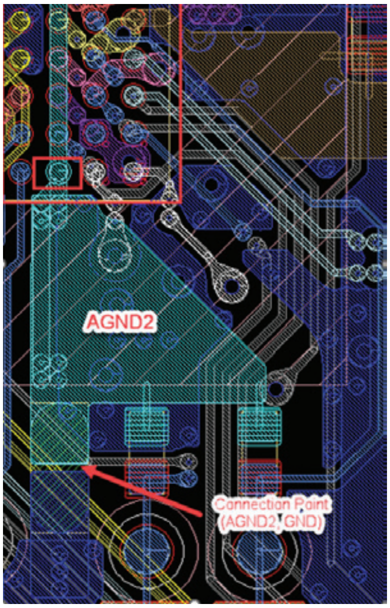

Figure 10: An example of two reference nets (AGND2 and GND) connected at one point

bond those planes together which reduces loop area and coupling. Additionally, to handle the current density denoted by the higher power ratings, the inverter phases and DC bus tend to form fingers that encompass the path between the DC link, bus capacitors to the power FETs, and phase connections. This can make decoupling any high-frequency transients associated with these FETs challenging due to space constraints. Therefore, the layers should be chosen in such a way as to be able to decouple in the smallest loop area possible.

Finally, when planning for the interconnection of these various plane layers together, it's tempting to try and galvanically isolate the high voltage switching ("noisy ground") and low voltage ("quiet ground") with strict adherence but often without care as to how these concepts play into the modules "system ground."

- By galvanically isolating, or otherwise offering a single point of connection, which creates the possibility of high impedance interconnections, resulting in an increase in common mode noise voltages and currents; or
- Physical cuts in the plane, either via trace or removal of copper for galvanic isolation, which can result in an increase in radiated emissions as currents capacitively couple across the discontinuities.

Both scenarios should be avoided to maintain signal integrity and reduce noise.

An example of a single-point connection between reference planes is shown in Figure 10, in which any electrical transients referenced to AGND but coupled onto a trace referenced to GND will have to travel back through this single-point connection.

Another example is shown in Figure 11, this time I^2C lines from an ASIC going to a level shifter.

The light blue is the I^2C's reference plane, meaning any electrical transients coupled onto that plane must traverse through that small plane through a single point connection to the system, reference on the top left of the light blue polygon.

In the last section of this article, we'll introduce the concept of rooming as a precursor to actual design.

CONNECTOR AND COMPONENT PLACEMENT

The design constraints imposed upon an inverter module aren't limited to mitigation of electromagnetics, but also to address cooling and ruggedness considerations. And, for that reason, designers will often find themselves working with a PCB assembly whose form factor and cooling requirements are already given to them, rather than designing a case around the assembly. And, as such, a popular strategy that should always be applied before designing any circuit board is floor planning using your favorite diagramming tool. This allows visualization of three key areas of an inverter and their relation to phase cabling:

- *Low voltage signaling*—Typically made up of an MCU and supporting devices (such as flash, Ethernet or CAN PHY, and sensors), and half of the gate driver circuit.
- *High voltage input section*—Includes input connectors that carry the brunt of the power from the bus voltage and the DC bus caps that stabilize the DC bus during actuation.
- *High voltage switching section*—Comprises various sections of the three phases, the output switches, and the other half of the gate driver.

An example of a floor plan and how it can help visualize planning currents is shown in Figure 12. In the example to the left, there is a risk of signals running near each other causing unintended coupling. In the example to the right, placing the connector farther away reduces the concern.

CONCLUSION

With the push across various industries to hybridize machines that would otherwise be pneumatic or hydraulically driven, inverters are becoming prolific. This two-part article details the importance of starting with a solid foundation, first by creating a rooming plan, and then choosing the correct PCB stack up during component selection and placement, including placeholders for components that otherwise can be unpopulated. These decisions, when done early, allow the designer flexibility when an otherwise difficult-to-diagnose problem comes up, such as incorrect actuation of a gate drive, or communication lines causing the software to lock up.

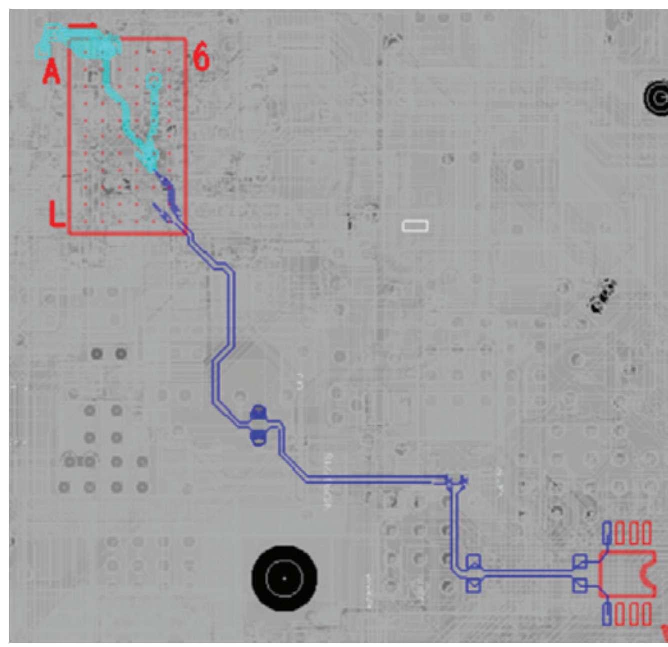

Figure 11: Another example of a single-point reference connection, and I^2C lines being referenced at a single point from the system

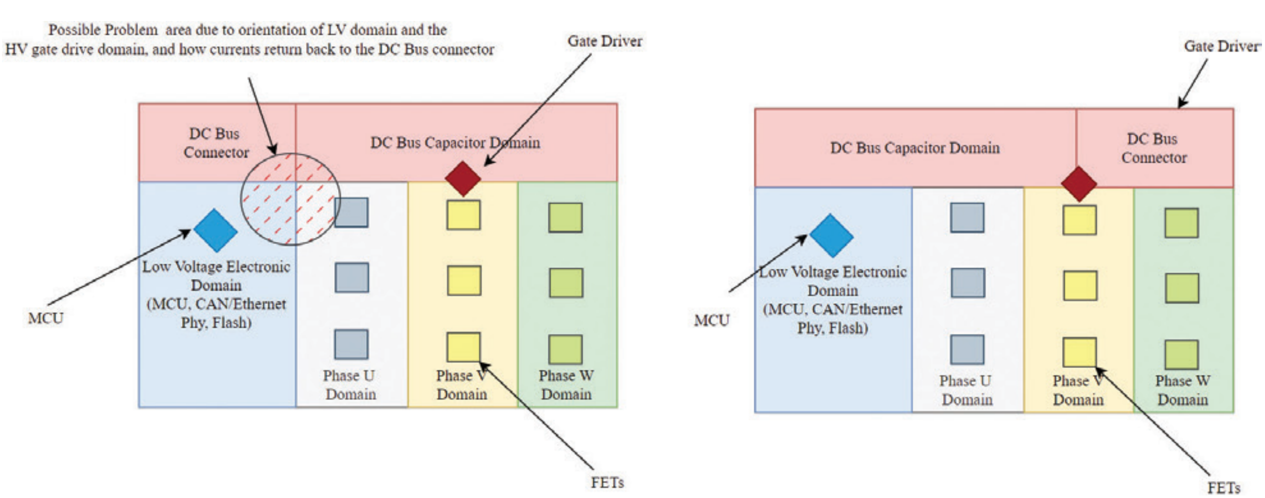

Figure 12: An example of rooming, and how it can help identify problem areas in the planning phase of a design

CHINA'S GB 31241-2022 STANDARD

The New Safety Standard for Lithium-Ion Cells and Batteries

Lithium-ion cells and batteries produced in or imported into China are now regulated in accordance with China's Compulsory Certification (CCC) system. The China State Administration for Market Regulation (SAMR) announced CCC requirement for lithium-ion cells and batteries used in portable electronic equipment through Notice No. 10 issued in 2023.[1] Effective August 1, 2024, all regulated lithium-ion cells and batteries must be CCC-certified for compliance with the requirements set forth in GB 31241.

GB 31241, "Lithium-ion cells and batteries used in portable electronic equipment – Safety technical specification," was originally issued in 2014 and more recently replaced by the 2022 version, GB 31241-2022.[2] GB 31241-2022 is not equivalent to any current international standard. However, relevant reference standards include, but are not limited to, IEC 62133-2:2017,[3] UN 38.3 (7th Revision),[4] and UL 1642:2020.[5]

GB 31241-2022 imposes new and updated requirements on manufacturers of lithium-ion cells and batteries. This article provides a summary of the requirements in GB 31241-2022 and guidance on their application.

SCOPE

GB 31241-2022 specifies safety technical requirements for lithium-ion cells and batteries used in portable electronic equipment. Examples include:

- *Portable office products*: notebook computers, tablets, etc.;
- *Mobile communications products*: mobile phones, cordless telephones, walkie talkies, etc.;

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- *Portable audio/video products*: portable televisions, portable audio/video players, cameras, video recorders, voice recorders, Bluetooth headsets, portable speakers, etc.; and
- *Other portable products*: electronic navigators, digital picture frames, game consoles, e-books, mobile power supplies, portable energy storage power supplies, portable projectors, wearable equipment, etc.

There may be additional requirements for cells and batteries used in portable electronic products in vehicles, ships, aircraft, etc., and for other devices used in the fields of medical, mining, and undersea operations.

However, GB 31241-2022 is not applicable to lithium-ion cells and batteries used in electronic cigarettes.

TERMS AND DEFINITIONS

Terms and definitions specific to this standard and/or not commonly used in the other standards are listed in Table 1. Terms including "nominal voltage," "nominal energy," "reference test current," "end-of-discharge voltage," "lower limit charging temperature," "lower limit discharging temperature," and "allowable maximum surface temperature" are new to the 2022 edition of GB 31241. At the same time, the standard no longer defines or uses the terms "venting," "rupture," and "routine test."

Terms	Clause*	Definition
Lithium-ion cell	3.1	a device that relies on the movement of lithium ions between the positive and negative electrodes to convert chemical energy into electrical energy and is designed to be rechargeable
Lithium-ion battery	3.2	a ready-to-use assembly of any number of lithium-ion cells including protective circuit
Nominal energy	3.9	an approximate value of the voltage used to designate or identify a cell or battery
Over voltage for charge protection U_{cp}	3.12	protection circuit operating voltage during high voltage charging specified by the manufacturer
Limited charging voltage U_{cl}	3.13	the rated maximum charging voltage of a cell or battery as specified by the manufacturer
End-of-discharge voltage U_{de}	3.14	Manufacturer recommended voltage of a cell or battery at the end of discharge
Low voltage for discharge protection U_{dp}	3.15	protection circuit operating voltage during low voltage discharging specified by the manufacturer
Discharge cut-off voltage U_{do}	3.16	the minimum load voltage specified by the manufacturer for safe discharge of a cell or battery
Over current for charge protection I_{cp}	3.18	protection circuit operating current during large current charging specified by the manufacturer
Recommendation charging current I_{cr}	3.19	manufacturer's recommended constant-current charging current
Maximum discharging current I_{dm}	3.20	maximum continuous discharge current specified by the manufacturer
Over current for discharge protection I_{dp}	3.21	protection circuit operating current during large current discharging specified by the manufacturer
Recommendation discharging current I_{dr}	3.22	manufacturer's recommended continuous discharge current
Upper limit charging temperature T_{cm}	3.23	the highest temperature during charging a cell or battery specified by the manufacturer
Lower limit charging temperature T_{cl}	3.24	the lowest temperature during charging of a cell or battery specified by the manufacturer
Upper limit discharging temperature T_{dm}	3.25	the highest temperature during discharging of a cell or battery specified by the manufacturer
Lower limit discharging temperature T_{dl}	3.26	the lowest temperature during discharging of a cell or battery specified by the manufacturer
Allowable maximum surface temperature T_{max}	3.27	the permissible maximum temperature on the surface of a cell or battery under normal operating conditions specified by the manufacturer.

* GB 31241-2022 clause number

Table 1: GB 31241 terms and definitions

Description	Specifications GB 31241-2022		Specifications IEC 62133-2:2017		Specifications UN 38.3		Applicability GB 31241-2022	
	Clause(s)	**Parameters**	**Clause**	**Parameters**	**Clause**	**Parameters**	**Cell**	**Battery**
Sample capacity Test	4.7.3	Charge fully, sit for 10 min., discharge and measure the capacity	-	-	-	-	X	X
Durability	5.3.3	Water 15 s, 75% alcohol 15 s	-	-	-	-	-	X
High temperature external short-circuit	6.1	57 °C ± 4 °C, 30 min; 80 mΩ ± 20 mΩ; 20% or 24 h	7.3.1	55 °C ± 5 °C, 1-4 h; 80 mΩ ± 20 mΩ. 55 °C ± 5 °C, 24 h or 20%.	38.3.4.5 (T5)	57 °C ± 4 °C, 6 or 12 h; < 0.1 Ω; 57 °C ± 4 °C, 1 h or ½ temp increase	X	-
Overcharge	6.2	I_{cm}; U_{cl} + 0.4, 4.65, or U_{cl} + 0.2; 7 h or charging time, or 20% of max temp	7.2.1	Charging current; standard voltage; 7 days	38.3.4.7 (T7)	2 x charging current; 2 x charging voltage or 22 V (≤ 18 V), or 1.2 x charging voltage (> 18 V); 24 h	X	-
Forced discharge	6.3	1 I_tA; -U_{up} ; 90 min.	7.3.7	1 I_tA; -U_{up} ; 90 min.	38.3.4.8 (T8)	Max. discharge current; rated capacity divided by the test current	X	-
Low pressure (altitude simulation)	7.1, 8.1	11.6 kPa, 20 °C ± 5 °C, 6 h	-	-	38.3.4.1 (T1)	11.6 kPa, 20 °C ± 5 °C, 6 h	X	X
Temperature cycling	7.2, 8.2	72 °C ± 2 °C, 6 h; -40 °C ± 2 °C, 6 h; 10 times. 20 °C ± 5 °C, 6 h	-	-	38.3.4.2 (T2)	72 °C ± 2 °C, 6 or 12 h; -40 °C ± 2 °C, 6 or 12 h; 10 cycles. 20 °C ± 5 °C, 24 h	X	X
Vibration	7.3, 8.3	Sinusoidal, 7-200-7 Hz, 15 min; 12 cycles; 3 h	7.3.8.1	Sinusoidal, 7-200-7 Hz, 15 min; 12 cycles; 3 h	38.3.4.3 (T3)	Sinusoidal, 7-200-7 Hz, 15 min; 12 times; 3 h	X	X
Acceleration impact (mechanical shock)	7.4, 8.4	150 g_n ± 25 g_n, 6 ms ± 1 ms; 3 shocks	7.3.8.2	150 g_n, 6 ms; 3 shocks	38.3.4.4 (T4)	150 g_n or 50 g_n; 6 ms or 11 ms; 3 shocks	X	X
Free fall	7.5, 8.5	1.5 m (user replaceable batteries only) or 1 m (all others)	7.3.3	1 m	-	-	X	X
Crush	7.6	13.0 kN ± 0.78 kN, Speed 0.1 mm/s	7.3.5	13 kN ± 0.78 kN	38.3.4.6 (T6)	13.0 kN ± 0.78 kN, Speed 1.5 cm/s	X	-
Heavy object impact	7.7	9.1 kg ± 0.1 kg, 610 mm ± 25 mm	-	-	38.3.4.6 (T6)	9.1 kg ± 0.1 kg, 61 ± 2.5 cm	X	-
Thermal abuse	7.8	130 °C ± 2 °C, 30 min	7.3.4	130 °C ± 2 °C, 30 min	-	-	X	-
Projectile (combustion jet)	7.9	Cell is heated until it explodes, completely burnt out, or 30 min	-	-	-	-	X	-
Stress relief	8.6	70 °C ± 2 °C, 7 h	7.2.2	70 °C ± 2 °C, 7 h	-	-	-	X
High temperature use	8.7	80 °C, 7 h	-	-	-	-	-	X
Washing	8.8	11.0 ± 0.1 (pH), 45 °C ± 2 °C	-	-	-	-	-	X
Overvoltage charging	9.2	I_{cm}; 6 V (n = 1) or (n x 6.0) V (n ≥ 2); 1 h or (C/I_{cm}) h, or until protection circuit activates	-	-	-	-	-	X
Overcurrent charging	9.3	1.5 I_{cp}; U_{up} or until protection circuit activates	-	-	-	-	-	X
Undervoltage discharging	9.4	I_{dm}; (n x 0.15) V or until protection circuit activates. 10 min	-	-	-	-	-	X
Overcurrent discharging	9.5	1.5 I_{dp}; U_{de} or until protection circuit activates.	-	-	-	-	-	X
External short-circuit	9.6	20 °C ± 5 °C , 80 mΩ ± 20 mΩ; 24 h or protection circuit activates	7.3.2	20 °C ± 5 °C, 80 mΩ ± 20 mΩ; 24 h or 20%.	-	-	-	X
Reverse charging	9.7	I_{cr}, -U_{up}; 90 min or until protection circuit activates	-	-	-	-	-	X

X: applicable, -: not applicable

Table 2: Type tests for cells and batteries

TYPE TESTS

Demonstrating compliance with the requirements of GB 31241 includes conducting certain tests listed in Table 2 and Table 3. The general acceptance criteria for each test are that the sample being tested does not generate a fire, explode, or leak as a result of testing.

Description	Specifications GB 31241-2022	
	Clause	Parameters
Overvoltage charge protection	10.1	I_{cm}, (n x 6.0) V. 1 min after protection circuit activates. 500 cycles.
Overcurrent charge protection	10.2	1.5 I_{cp}, U_{up}. 1 min after protection circuit activates. 500 cycles.
Undervoltage discharge protection	10.3	I_{dr}, (n x U_{do}) or U_{do} V. 1 min after protection circuit activates. 500 cycles.
Overcurrent discharge protection	10.4	1.5 I_{dp}. 1 min after protection circuit activates. 500 cycles.
Short circuit protection	10.5	80 mΩ ± 20 mΩ. 1 min after protection circuit activates. 500 cycles.

Table 3: Type tests for batteries with protection circuit (Note: "n" is the number of cells connected in series or blocks of cells connected in parallel in the battery)

Charging, Discharging, and Conditioning Procedures

Prior to testing, cells and batteries are subject to charging, discharging, and/or conditioning, as applicable. The manufacturer-specified charging procedure is preferred. An alternative charging procedure (which is new to this version) is to charge at 0.2 I_t A. When the terminal voltage reaches the limited charging voltage (U_{cl}), change to constant voltage charging until the charging current is less than or equal to 0.2 I_t A.

A cell or battery is discharged at a constant current of the recommendation discharging current (I_{cr}) down to the end of discharge voltage (U_{de}). This discharge procedure is new and replaces the manufacturer-specified procedure.

Cells and batteries are to be conditioned with two charge-discharge cycles. The interval between charge and discharge is 10 minutes. New to the 2022 version of GB 31241 is the introduction of an electrostatic discharge (ESD) test for batteries equipped with protection circuits. In such cases, the ESD test must be conducted after two charge-discharge cycles and being fully charged, using a ± 4 kV contact discharge and ± 8 kV air discharge.

Test Items

Table 2 lists required tests for cells and batteries. The same or similar tests found in 62133-2:2017 and in UN 38.3 (7^{th} Edition and 8^{th} Edition) are also included in the table for comparison.

For batteries incorporating a protection circuit, additional test items, as listed in Table 3, apply.

Sample Capacity Test

The sample is fully charged and is then left idle for 10 minutes. Then, the capacity is measured as the sample is being discharged.

Durability

This test applies only to user-replaceable batteries. The test is conducted by rubbing the marking for 15 seconds with a piece of cotton cloth soaked with water, then rubbing the marking for 15 seconds with a piece of cotton cloth soaked with 75% (alcohol by volume) medical use alcohol.

External Short Circuit

A test sample is deliberately short-circuited by connecting the positive and negative terminals 30 minutes after the surface temperature of the test sample reaching 57 ˚C ± 4 ˚C (for a cell) or room temperature (for a battery). The total external resistance shall be 80 mΩ ± 20 mΩ.

For cells, the test sample remains on test until the surface temperature declines by 20 % of the maximum temperature rise, or for a period of 24 hours, whichever is sooner. Batteries with the protection circuit removed remain on test for 24 hours, while batteries with a protection circuit remain on test until the protection circuit activates.

Overcharge

A fully discharged cell is charged at a constant current of the maximum charging current (I_{cm}) until reaching the voltage of U_{cl} + 0.4 (U_{cl} < 4.25), 4.65 (4.25 ≤ U_{cl} <4.35), or U_{cl} + 0.2 (U_{cl} ≥ 4.45), then followed by constant voltage charging. (Note that the charging current and voltage in the 2022 version of GB 31241 are different than those specified in the 2014 version.)

During testing, monitor the cell temperature change. Terminate testing after either:

a. The longer period of 7 hours or the charging time declared by the manufacturer, or
b. The cell's temperature declines by 20 % of the maximum temperature.

When there is a difference between the results of a) and b), those generated during the longer of the two options takes precedence.

Forced Discharge

A fully discharged cell is subjected to a forced-discharge at 1 I_tA to the negative value of the upper limit charging voltage (-U_{up}). The total duration for the forced discharge testing is 90 minutes.

Low Pressure (Altitude Simulation)

Fully charged cells are placed in a vacuum chamber with an ambient temperature of 20 °C ± 5 °C. The internal pressure of the vacuum chamber is gradually reduced to a pressure equal to 11.6 kPa (simulating an altitude of 15,240 m), and then remains under test for 6 hours.

Temperature Cycling (Thermal Cycling, Thermal Rest)

The fully-charged cells are placed in a programmable test chamber at 20 °C ± 5 °C. The test chamber's temperature is increased to 72 °C ± 2 °C and maintained at this temperature for 6 hours. Then the test chamber's temperature is reduced to - 40 °C ± 2 °C and maintained at this temperature for 6 hours. The transition time between different temperatures does not exceed 30 minutes. After repeating this cycle 10 times, the cells are stored for a minimum of 6 hours at a room temperature of 20 °C ± 5 °C.

Vibration

A fully charged test sample is subject to a vibration having a sinusoidal waveform with a logarithmic sweep between 7 Hz and 200 Hz and back to 7 Hz traversed in a 15-minute time span. This cycle is repeated 12 times for a total of three hours for each mounting position of the test sample. Cylindrical and button test samples are vibrated in both their axial and longitudinal directions. Prismatic and pouch samples are vibrated in three mutually-perpendicular directions.

Acceleration Impact (Mechanic Shock, Shock)

The fully charged cells or batteries are secured on the impact table for semi-sinusoidal pulse impact test. Within the first 3 ms, the minimum average acceleration is 75 g_n, the peak acceleration is 150 g_n ± 25 g_n, and the pulse duration is 6 ms ± 1 ms. Each test cell or battery is subjected to three acceleration impact tests in each direction.

Free Fall

Each fully charged cell or battery is dropped from a height of 1.0 m onto a flat concrete floor, except for user-replaceable batteries, which are dropped from a height of 1.5 m. Both terminal sides of the cylindrical and button cells and batteries are dropped once. The cylindrical side is dropped twice. There are four drop tests in total. Each side of the prismatic and pouch cells and batteries are dropped once. There are six drop tests in total.

Crush

Each fully charged cell is crushed, perpendicular to the direction of the flat surfaces, between two flat surfaces. The force for the crushing is applied by a device exerting a force of 13.0 kN ± 0.78 kN at a speed of 0.1 mm/s. Once the maximum force has been applied, or an abrupt voltage drop of one-third of the original voltage has been obtained, the force is released.

A cylindrical cell is crushed with its longitudinal axis parallel to the flat surfaces of the crushing apparatus. A button cell is crushed with its upper and lower sides parallel to the flat surfaces of the crushing apparatus. For prismatic cells (hard shell), pouch cells with a length less than 25 mm, and other types of cells, perform the crush test only on the wide surface of the cell.

For pouch cells with a length not less than 25 mm, place a steel semi-cylinder with a diameter of 25 mm on the wide surface of the cell for crushing. The longitudinal axis of the semi-cylinder body passes through the geometric center of the wide surface and is perpendicular to the direction of the electrode tab. The length must be greater than the size of the crushed cell. Release the force once the crush force reaches the force listed in Table 10 of the standard. This test procedure is new to this version.

Heavy Object Impact

A fully charged cell is placed on the surface of the platform. A metal bar of 15.8 mm ± 0.2 mm in diameter is placed horizontally on the upper surface of the geometric center of the cell. A weight with a mass of 9.1 kg ± 0.1 kg falls freely from a height of 610 mm ± 25 mm on to the cell. Each cell is to be subjected to only one single impact. This test does not apply to pouch cells. This is the same test as the impact test found in Clause 14 of UL 1642 5th Edition.

Thermal Abuse (Heating)

A fully charged cell is placed in a test chamber. The chamber's temperature is raised at a rate of 5 °C/min ± 2 °C/min to a temperature of 130 °C ± 2 °C. The cell remains at this temperature for 30 min before the test is terminated.

Projectile (Combustion Jet)

A fully charged cell is placed on a steel wire screen of a test apparatus shown in Figure C.2 of the standard, which is equivalent to Figure 20.1 of UL 1642 5th Edition. If the cell falls off the screen during test, a single metal wire can be used to secure the cell to the screen. A cell is heated and remains on the screen until it explodes, has completed burned out, or is heated for 30 minutes without explosion or catching fire.

Stress Relief (Case Stress at High Ambient Temperature)

The thermoplastic materials used in the molded or injection-molded enclosure or structure must not result in shrinkage or deformation that affects the safety of the cell when the internal stress generated by molding or injection molding is released. The fully charged battery is placed in an air circulating oven at a temperature of 70 °C ± 2 °C for 7 hours. The battery is then removed and allowed to return to room temperature.

High Temperature Use

Batteries shall be sufficiently safe when used under high temperature conditions. To ensure compliance with this requirement, a fully charged battery is placed in a high temperature test chamber with the temperature set to the maximum value of:

- The manufacturer-specified upper limit charging temperature and upper limit discharging temperature of the battery;
- The manufacturer-specified upper limit charging temperature and upper limit discharging temperature of the cell; or
- 80 °C.

After the surface temperature of the sample stabilizes, the battery remains under these test conditions for 7 hours.

Washing

This test applies to hand-held and pocket-sized portable electronic equipment containing lithium-ion batteries. The test apparatus for the washing test is shown in Figure C.3 of the standard. The washing solution has a pH value of 11.0 ± 0.1 (a NaOH solution with a mass fraction of 0.004 % can be used) and is maintained at a temperature of 45° C ± 2° C during the test.

The test is performed by the following steps: solution preparation, immersion, stirring, dehydration, and drying. If the sample can be charged and discharged following the washing, continue one discharge-charge cycle, and then end the test. If the sample cannot continue to charge and discharge, then end the test.

Overvoltage charging

A fully-charged battery is continuously charged at the constant current of the maximum charging current (I_{cm}) to the specified test voltage or the maximum bearable voltage (whichever is higher) and is then maintained at that voltage for constant-voltage charging. The specified test voltage is 6 V (when n = 1) or (n × 6.0) V (when n ≥ 2), with n representing the number of cells connected in series or blocks of cells connected in parallel in the battery.

For batteries with the protection circuit removed, charge for 1 hour or (C/ I_{cm}) hour, whichever is longer. For battery with protection circuit retained, charge until the protection circuit activates.

Overcurrent Charging

A fully discharged battery is charged at a constant current of 1.5 times the overcurrent charging protection current (1.5 I_{cp}). For batteries with the protection circuit removed, charge to the upper limited charging voltage U_{up}. For batteries with the protection circuit retained, charge until the protection circuit activates.

Undervoltage Discharging

A fully charged battery is discharged at the constant current of the maximum discharging current (I_{dm}). For batteries with the protection circuit removed, discharge to (n x 0.15) V, with n representing the number of cells connected in series or blocks of cells connected in parallel in the battery. For batteries with the protection circuit retained, discharge until the protection circuit activates.

Overcurrent Discharging

A fully charged battery is discharged at the constant current of 1.5 times the overcurrent discharging protection current (1.5 I_{dp}). For batteries with the protection circuit removed, discharge to the end-of discharge voltage. For batteries with the protection circuit retained, discharge until the protection circuit activates.

Reverse Charging

A fully charged battery is reverse charged to the negative upper limited charging voltage ($-U_{up}$) at the recommendation charging current I_{cr}. For batteries with the protection circuit removed, charge for 90 minutes. For batteries with the protection circuit retained, discharge until the protection circuit activates.

LABELING REQUIREMENTS

For lithium-ion cells and batteries, the following information, in Chinese, must appear on the product:

- Product name, model;
- Rated capacity, nominal energy, limited charging voltage, nominal voltage;
- Positive and negative polarities;
- Factory of manufacture; and
- Date of manufacture or batch number.

For CCC-regulated cells and batteries, the CCC mark shall be applied to the product. CCC mark requirements are stipulated in Attachment 2 of CNCA 2023 Notice No. 12.[6]

WARNING INSTRUCTIONS

Warning instructions in Chinese shall be placed on the batteries or on the smallest package. For user-replaceable batteries that can be placed in an ingestion gauge, warning instructions in Chinese shall also be provided on their smallest package.

CONCLUSION

GB 31241-2022 introduces important new and updated requirements. Compliance with this standard is mandatory for cells and batteries used in portable electronic equipment.

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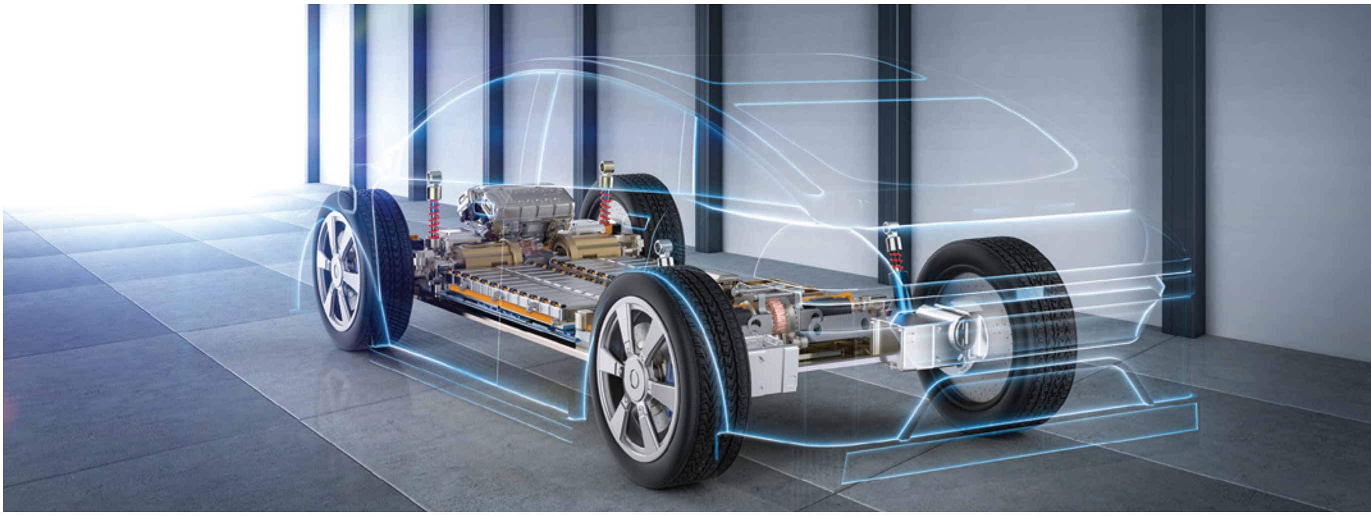
EMC TESTING OF E-MOTOR SYSTEMS

Technical Measures to Fulfill Practical and CISPR 25-Compliant EMC Tests on E-Axles



Electromagnetic compatibility (EMC) testing of e-drives and e-axles at the component level per CISPR 25 requires both technical measures and carefully developed implementation strategies to ensure that measurements accurately reflect real-world performance. Given the rising demands on performance classes, particularly for high-power electric axles, these tests require a setup that closely resembles the e-axle's actual in-vehicle installation conditions. Achieving this realistic test setup presents unique challenges, as the scale and complexity of the test object directly impact the design and setup of the test bench.

For realistic testing, it is essential to account for the mechanical and spatial demands of larger e-axle systems. This often necessitates a significantly larger test bench than those typically used for conventional automotive components. Such an expanded setup results in increased metal structures within the test environment, specifically in the anechoic chamber. This added metal

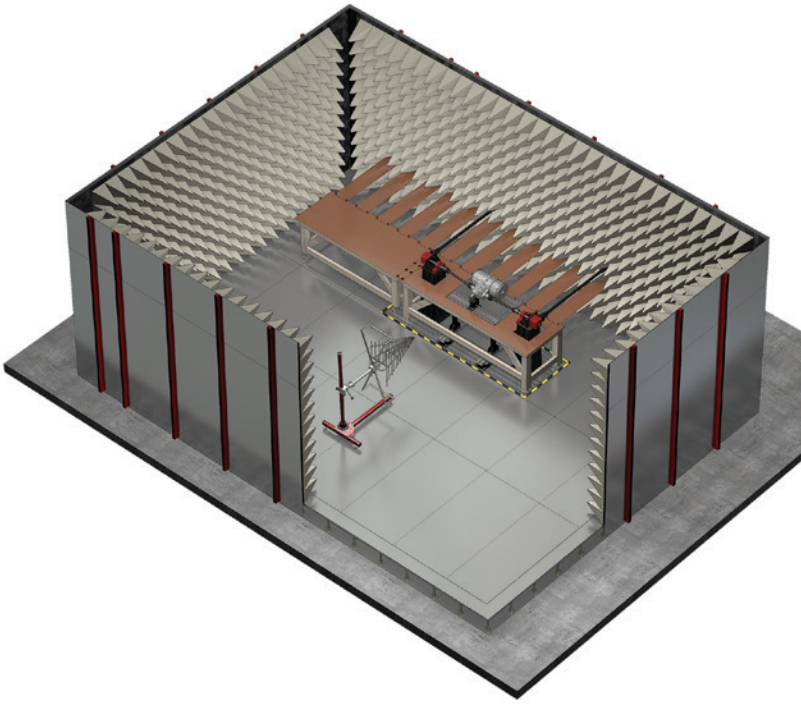


Figure 1: Rendering of EDTC-AX, with two outside load machines

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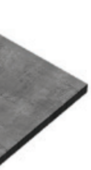
can influence the electromagnetic field distribution, potentially introducing reflections and resonances that affect measurement accuracy. Thus, ensuring that metallic elements do not interfere with the EMC results is a primary concern in the test bench design.

Another critical factor is the routing of cable harnesses. In many test benches, these cables must be routed near the metallic structures of the test setup. Ideally, they should be placed at the standardized length specified by CISPR 25 on the table's ground plane. However, this proximity to metal surfaces can lead to unintended electromagnetic coupling and alter the interference profile, creating additional challenges for measurement precision.

The long wire method has typically been used to assess the impact of these factors on the interference emission range of 150 kHz to 1 GHz. This method allows for testing multiple test setup variations, providing insights into how different configurations influence emissions. While the long wire approach can identify general trends, it may not fully replicate the actual setup of a complex e-axle system. Nevertheless, it serves as a useful basis for studying how elements such as metallic proximity, cable routing, and structure size impact emissions across various test configurations.



The findings from our investigation highlight the complexities and potential variabilities involved in EMC testing for electric drives and axles, particularly when different test benches yield slightly different results. Consequently, this study aims to initiate a broader discussion on the standardization and reproducibility of measurement results for electric drives and axles across diverse test environments. By sharing these findings, we hope to encourage further research into optimizing EMC test setups and, ultimately, to foster more standardized and comparable testing practices for e-drive systems.

NORMATIVE BASICS AND CRUCIAL ASPECTS FOR EMC TESTING

When performing EMC testing on automotive components according to CISPR 25, there are several crucial aspects to consider:

- *Test environment:* The test environment should be controlled and free from external electromagnetic interference. CISPR 25 tests are typically performed in shielded rooms or anechoic chambers to allow compliant testing and meet the ALSE verification in the defined frequency range.
- *Grounding and bonding:* Proper grounding and bonding are essential to ensure accurate testing results. Test setups must replicate the actual grounding conditions of the vehicle to achieve realistic results, especially for devices that are connected to the vehicle chassis or grounded to it.
- *Cable and harness layout:* The layout of cables and wiring harnesses used during testing should be as close as possible to the actual installation in the vehicle. This includes considerations like spacing, routing, and orientation of the cables to replicate in-vehicle conditions.
- *Frequency range and limits:* CISPR 25 specifies emission limits for various frequency bands (typically from 150 kHz to 2.5 GHz), which are relevant for automotive systems. It's crucial to know the frequency range required by the component and ensure compliance with specified limits.
- *Measurement equipment and probes:* Use CISPR 25-compliant measurement equipment, like

antennas, line impedance stabilization networks (LISNs), and RF probes, to ensure consistent and accurate results. Each piece of equipment must be calibrated to meet CISPR standards.

- *Radiated and conducted emissions:* CISPR 25 covers both radiated and conducted emissions. Radiated emissions testing focuses on the electromagnetic field emitted from the device, while conducted emissions testing measures noise on power or signal lines. Ensure that the test setup properly isolates and measures each type of emission as required.
- *Power supply considerations:* Use a stable and regulated power supply to replicate the vehicle's electrical environment. Automotive components are often tested at different voltages (e.g., 12V, 24V) to ensure they meet CISPR 25 standards under typical operating conditions.
- *Component mode of operation:* Test the component in all its possible modes of operation. The device should be tested in idle, active, and any special modes to ensure it meets standards across its entire functional range.
- *Compliance with test levels:* CISPR 25 defines various test levels for different types of devices and applications. Selecting the correct test level is crucial based on the component's placement in the vehicle and its susceptibility to or generation of electromagnetic interference.
- *Data logging and analysis:* Comprehensive logging of results, including peak, average, and quasi-peak values, is essential. Accurate data analysis will determine compliance with CISPR 25 standards and help identify any specific issues needing mitigation.

ADAPTATION OF CISPR 25 AND POSSIBLE SET-UP VARIANTS

Meeting the previously-referenced normative basics help to ensure that automotive components meet EMC requirements per CISPR 25, improving reliability and safety in the electromagnetic environment of a vehicle.

However, considering those crucial aspects of CISPR 25, testing can present a difficult challenge, especially when accounting for the component mode of operations that are required for e-motors or e-axles, as well as its correct and impact-free implementation into an EMC environment.

Furthermore, according to CISPR 25, a setup for e-axles is normatively not defined. Unlike conventional automotive components, e-axles can combine an electric motor, inverter, and transmission, which often create complex interactions between these subsystems in terms of electromagnetic emissions. The lack of a dedicated normative setup in CISPR 25 means that engineers must pay close attention to how the test bench is designed, as the setup itself can significantly influence test results.

Influencing parameters in the design of test benches for e-axle systems include the arrangement of high-voltage cables, grounding and bonding practices, motor positioning, and cooling systems, each of which can affect EMC performance. For instance, cable layouts and connections must realistically mimic in-vehicle conditions to ensure accurate emissions measurements, as real-world installations are influenced by the vehicle's metallic structure and shielding effects. Proper grounding and bonding of the e-axle and all associated components are also essential, as this can mitigate or amplify emissions depending on the test bench's design.

Considering these issues, e-axle EMC tests at the component level aim to replicate installation conditions as closely as possible. Yet, they often fall short of simulating the entire electromagnetic environment of a vehicle. To address this, system-level tests based on CISPR 12 (applicable to whole vehicles) may provide more realistic insights into how an e-axle will perform once installed. CISPR 12 considers radiated emissions for the entire vehicle and can reveal potential integration issues that might not be evident in isolated component testing. This broader testing approach may also highlight interactions between the e-axle and other on-board systems, such as power electronics, battery systems, and auxiliary electronics, each of which can contribute to the vehicle's overall electromagnetic emissions.

While conducting CISPR 12 tests at the vehicle level offers valuable insight into the real-world EMC behavior of e-axles, these tests are complex and resource-intensive. Therefore, engineers must carefully balance the thoroughness of the EMC testing process with the time and cost constraints typical of automotive development cycles.

INVESTIGATION OF TEST SETUPS AND RESULTS

In line with the requirements set forth in CISPR 25, we investigated several practical design variations to evaluate the setup, using the long wire method as a measurement basis. These variations included:

- Routing the cable harness close to metallic structures
- Using ferrites to minimize signal reflections
- Positioning the antenna near metallic structures
- Injecting a 120 dBµV signal within the 150 kHz to 1 GHz frequency range
- Measuring emissions, including consideration of the antenna factor
- Comparing the results to the CISPR 25 reference level to determine any deviations
- Ensuring compliance by achieving 90% of all measured points within a ±6 dB tolerance band

Case 1: Change in the Metal Structure Above the Table Ground Plane

Our testing verified that measurement results are negatively impacted when metal structures are placed directly on the test table, indicating that the presence of metal above the ground plane significantly affects these results. Metal structures introduce changes in the electromagnetic field distribution, which can create unwanted reflections and resonances, thereby influencing the accuracy and consistency of measurements.

Case 2: Influencing the Built-Up Metal Structure by Using Isolation Material and Ferrites

When the metal structures are positioned in isolation from the table's ground plane, the measurement results improve notably, especially below 130 MHz, with a potential improvement of up to 6 dB. However, this adjustment leads to a distinct resonance peak at 160 MHz, which must be considered in the overall assessment. The use of ferrites positioned in front of metal structures shows minimal improvement below 30 MHz but proves effective in reducing interference between 30 MHz and 170 MHz. However, beyond 170 MHz, the emission results increase, indicating that ferrites may have limitations in high-frequency ranges.

Case 3: Comparing a Regular Test Table to a Real EMC Load Machine (EMC-BlueBox)

In our third test scenario, we performed initial measurements on a real component setup utilizing our company's EMC-BlueBox, a specialized emission-free and mobile load machine capable of handling up to

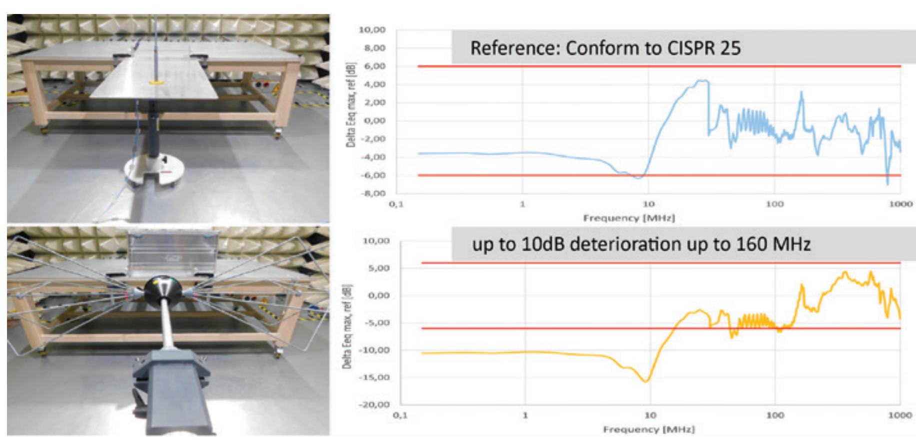


Figure 2: Measurement results on the change in metal structure over table ground

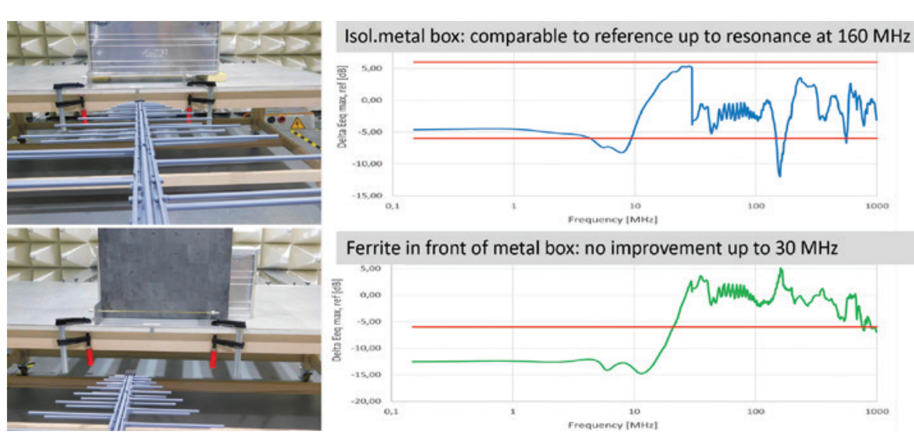


Figure 3: Measurement results on the change in isolation and absorption of metal structures over table ground plane

120 kW. This setup aimed to approximate in-vehicle conditions more closely and yielded results that show comparability to those obtained with the long wire method. Importantly, the results suggest that metallic structures located below the ground plane are less impactful; however, metal above the ground plane remains a significant influence on measurement accuracy, especially in certain frequency ranges.

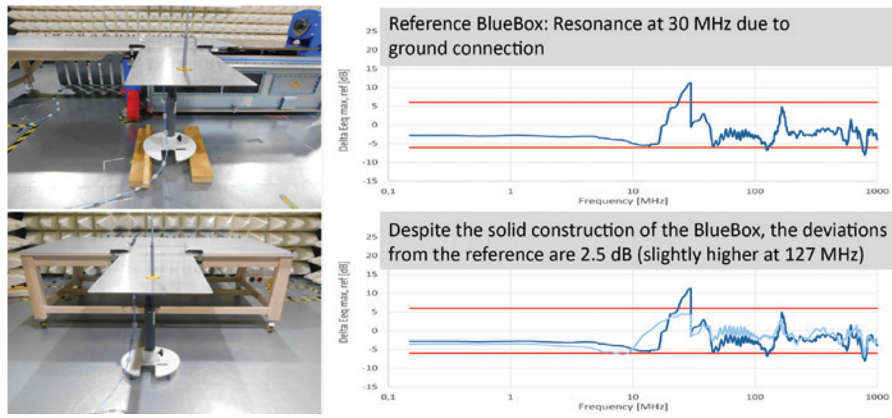


Figure 4: Measurement results comparing regular test table with EMC-BlueBox

REQUIREMENTS FOR A PROPER SET-UP AND REALISTIC MEASUREMENT

We conducted our investigations using the long wire method, which provides valuable insights but which cannot fully replicate the actual setup of a real component and its wiring harness. The long wire method is useful for identifying general trends but lacks the specificity needed for accurate component-level assessments.

These findings emphasize the need for additional investigations into the effects of metallic structures on EMC testing environments, particularly for e-drive and e-axle systems. It would be valuable to conduct broader studies across various EMC test benches used for e-drives and e-axles, considering that such systems often operate under high-power conditions and involve complex electromagnetic interactions. Such studies could lead to optimized test setups that better reflect real-world performance, improve measurement reliability, and support more accurate compliance assessments for automotive EMC standards.

For accurate and compliant EMC testing, certain critical factors should be considered:

- *Adherence to normative standards:* Ensure all relevant normative requirements are met to achieve international compliance and recognition.
- *Minimization of metallic structures:* Avoid large metallic structures, especially above the ground plane, as they can affect measurement accuracy.

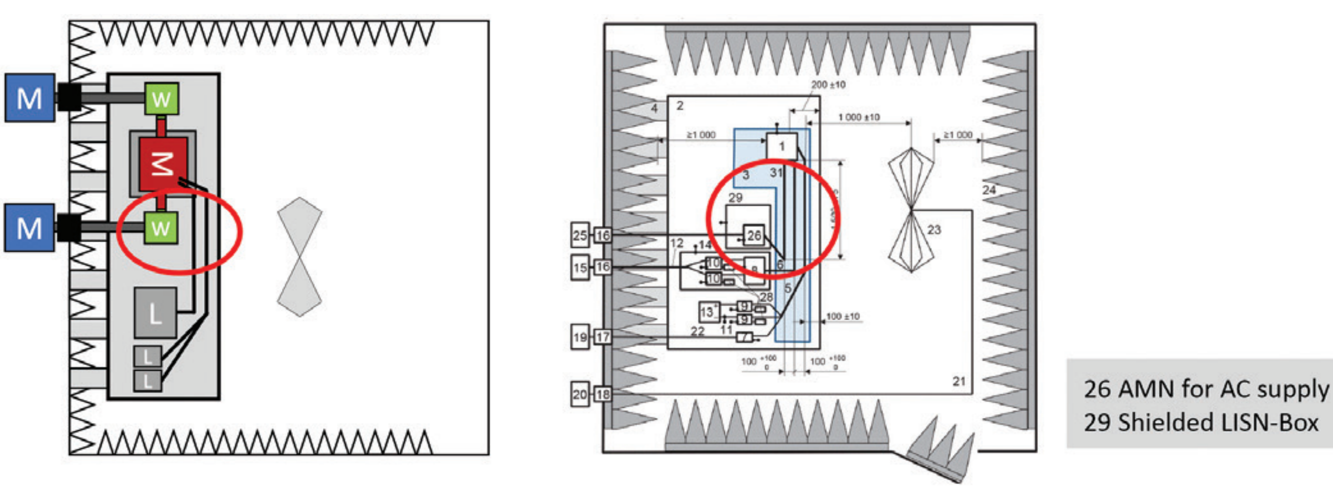


Figure 5: Proposal for the arrangement of load machines for e-axles, based on CISPR 25

- *Optimal cable harness placement:* Maximize the distance between the cable harness and metallic structures and avoid parallel routing to reduce electromagnetic interference.
- *Multi-directional measurements:* Conduct measurements from multiple directions around the test object to obtain a comprehensive understanding of emissions.

SETUP OF A DUAL LOAD MACHINE WITHIN AN EMC CHAMBER FOR TESTING E-AXLES

With reference to the investigation and with the need to test e-axles, a setup based on CISPR 25 with external load machines as a dual arrangement with 90° angle gears inside the EMC test environment is recommended. This configuration offers multiple advantages:

- *Minimal metal structure:* Keeping metal structures within the EMC system as compact as possible to reduce interference.
- *Shielded connections:* Using shielded shafts for connections between the external load machines and the anechoic chamber.
- *Optimized shaft length:* Keeping the shaft connection to the 90° angle gear short, while maintaining the required distances from absorbers per CISPR 25.
- *Flexible test table positioning:* Allowing the test table to be positioned laterally for e-axle testing or perpendicular to focus on the periphery and cable harness.
- *Integrated load machines:* Where possible, embedding load machines into the floor can further reduce structural interference.

KEY FINDINGS AND SUGGESTIONS FOR AN ADAPTED EMC TEST BENCH FOR E-AXLE TESTING

The findings of our investigation highlight the factors critical to developing a realistic and accurate EMC test bench for e-axle systems:

- *Impact of metallic structures on cable harnesses:* Metallic structures near the cable harness strongly influence emission results and can introduce errors.
- *Limited effectiveness of absorptive materials:* Using ferrite materials provides only partial compensation for metallic influence and is effective only up to 1 GHz.
- *Criticality of structures above the ground plane:* Metallic structures above the ground plane are particularly influential, creating resonance points that significantly alter results.
- *Reproducibility challenges:* Variations in size and placement of metallic structures above the ground plane can lead to major, often non-reproducible changes in results, highlighting the need for further investigation.

These insights are essential for refining EMC test setups, particularly for e-axle testing, to achieve reliable and repeatable measurements that accurately reflect real-world conditions. However, further investigations are required.

Although metallic structures are necessary in an EMC test site for setting up effective e-axle test benches, a CISPR 25-compliant environment can still be achieved by closely adhering to the considerations

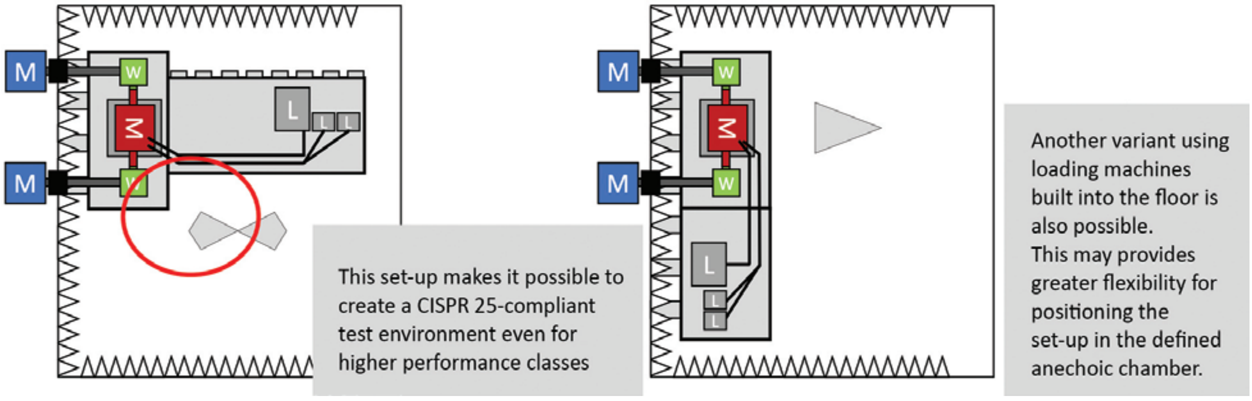


Figure 6: Proposal for the arrangement of the peripherals on an additional test table, depending on the focus of the EMC test

highlighted in this study. By strategically managing these metallic elements, the impact on electromagnetic measurements can be minimized. Test setups with high-performance capabilities have already been implemented in alignment with this approach. For instance, setups using dual 250 kW load machines, running at 3,000 RPM and capable of producing 3,000 Nm, reflect the high-performance requirements of electric axles designed by leading automotive manufacturers.

However, there is a need for further investigation and standardization. We advocate for updates to the CISPR 25 standard to address the unique challenges of testing electric axles, ensuring that consistent and reproducible testing methodologies are available to all OEMs and service providers globally. Establishing a unified approach to test procedures, equipment, and environmental conditions would improve test reliability and comparability, creating a standard that supports the rapid evolution of electric mobility.

Several additional factors should be considered for adapting CISPR 25 to better support e-axle testing. For example, the specific positioning of antennas is critical for accurately capturing emissions, while simulating dynamic driving conditions could provide more realistic insights into how these systems will behave under real-world operating conditions. Increased automation in test setups, both in terms of measurement and equipment handling, could improve efficiency and reproducibility.

Integrating e-axle test benches into an EMC testing environment requires detailed preparation of the anechoic chamber and careful selection of the medium used to simulate passive or active load on the test object. Depending on the setup, this could involve electrical, hydraulic, or pneumatic loading methods. Additionally, the spatial needs of the test setup, both within and outside of the EMC testing environment, should be considered, as e-axle testing equipment may require substantial space due to load machines, auxiliary systems, and ventilation requirements.

CONCLUSION

Achieving a CISPR 25-compliant environment for e-axle testing is feasible with careful design and planning. But a revision of the standard to accommodate these unique needs is essential to ensure repeatable, accurate, and internationally comparable EMC test results for electric axles.

Our investigation is based on the needs of OEMs or service providers who specialize in e-motor and e-axle EMC tests. We, in partnership with other industry colleagues, advocate for finding a practical investigation of a solution for testing electric axles, which can be implemented with various suppliers of load machines. The focus of the solution is on the correct implementation of the knowledge gained within an EMC test environment and on the reproducibility of EMC tests. The renderings presented in this article offer different expansion options. But, most importantly, they represent a realistic technical conception and offer practical implementation strategies.

PRODUCT Showcase

EMC EDUCATION

How Students Benefit from Collaboration Between Academia and Industry

By Bogdan Adamczyk

Each year, the January issue of *In Compliance Magazine* addresses EMC education. It is only fitting that this month "EMC Concepts Explained" [1] is also devoted to the topic of EMC education. Specifically, this column will describe a unique collaboration between academia and industry at Grand Valley State University (GVSU).

The EMC Center, located in Grand Rapids, Michigan, on the GVSU engineering campus, is an intersection between academia and industry that brings decades of EMC & High-Speed industry expertise, tools, and capabilities to the classroom and the student experience. E3 Compliance is an independently funded industrial group and a tenant within the GVSU Innovation & Design Center (IDC). They provide engineering students with industry experience in EMC & High-Speed electronic product development.

This unique collaboration between GVSU and E3 provides opportunities for undergraduate and graduate students to work on cutting-edge electronics technology in multiple industries such as automotive, aerospace, medical, defense, consumer, commercial and industrial.

This column starts with a description of the EMC & High-Speed laboratory, along with some of the capabilities and services offered to the industry. This is followed by examples of the unique student experiences that result from the collaboration between GVSU and E3 Compliance.

E3 COMPLIANCE AND INDUSTRY SUPPORT

E3 Compliance [2] is an ITAR-registered independent engineering consulting company located in downtown Grand Rapids, Michigan as a tenant within GVSU's Innovation Design Center (IDC).

Dr. Bogdan Adamczyk is professor and director of the EMC Center at Grand Valley State University (http://www.gvsu.edu/emccenter) where he performs EMC educational research and regularly teaches EM/EMC courses and EMC certificate courses for industry. He is an iNARTE-certified EMC Master Design Engineer. He is the author of two textbooks, "Foundations of Electromagnetic Compatibility with Practical Applications" (Wiley, 2017) and "Principles of Electromagnetic Compatibility: Laboratory Exercises and Lectures" (Wiley, 2024). He has been writing "EMC Concepts Explained" monthly since January 2017. He can be reached at adamczyb@gvsu.edu.

Scott Mee is a co-founder and owner at E3 Compliance, which specializes in EMC & SIPI design consulting, simulation, pre-compliance testing, and diagnostics. He has published and presented numerous articles and papers on EMC. He is an iNARTE-certified EMC Engineer and Master EMC Design Engineer. Scott participates in the industrial collaboration with GVSU at the EMC Center. He can be reached at scott@e3compliance.com.

E3 specializes in EMC and High-Speed design consulting, analysis and performs pre-compliance and diagnostic testing in a ~6000 sq ft lab. A birds-eye view of the lab and the 3-meter chamber are shown in Figure 1.

E3 COMPLIANCE AND GVSU COLLABORATION

E3 Compliance collaborates with GVSU to provide educational experiences for students in EMC and High-Speed electronic product development. The company's seasoned engineering team has over 100 years of combined experience in EMC & High-Speed which allows their team members to mentor and help educate

Figure 1: Birds-eye view of the EMC lab and a 3-meter chamber

students in challenging electrical engineering topics. E3 employs students, under non-disclosure, in a cooperative (co-op) undergraduate engineering program for 10 - 12 months that consists of three rotations where they alternate between taking classes and working full time in the company's lab.

During their first rotation, students are taught how to read and interpret regulatory and industry standards. They also perform high-speed signal and power integrity measurements as well as EMC pre-compliance tests such as radiated & conducted emissions, radiated & conducted immunity, electrostatic discharge and electrical disturbances. This experience gives students a great foundation of what EMC, Signal Integrity and Power Integrity are and how to perform measurements. It also exposes them to the latest product technologies and how they can exhibit EMC and High-Speed issues before they become ready for production.

During their second rotation, co-op students are exposed to product designs and are taught how to investigate EMC & High-Speed issues found through testing. This allows students to begin learning how to identify root-causes by understanding the physics using specialized tools while also mitigating problems by retrofitting devices in the lab. Students enjoy working hands-on in a lab environment to see the results on the bench or in the EMC chambers.

On their third rotation, students gain more independence and take on more responsibilities to work with industrial clients and help with industry course hardware demonstrations. They become capable of running a wide variety of different tests and measurements according to many different standards and engineering methods. The students are also capable of performing diagnostics to investigate and resolve EMC failures identified in testing.

The experience goes even further by allowing students to apply their knowledge to help industry clients prevent issues by participating in schematic, PCB layout and system design reviews before hardware is released. Students are able to see the full life-cycle of product development from concept to production releases. Eventually, they will have the rewarding experience of seeing products appear in the marketplace that they helped develop while obtaining their electrical engineering degrees. By the time the undergraduate students finish their degree they have one year of unique industrial experience. Figure 2 shows some of the GVSU co-op students at work.

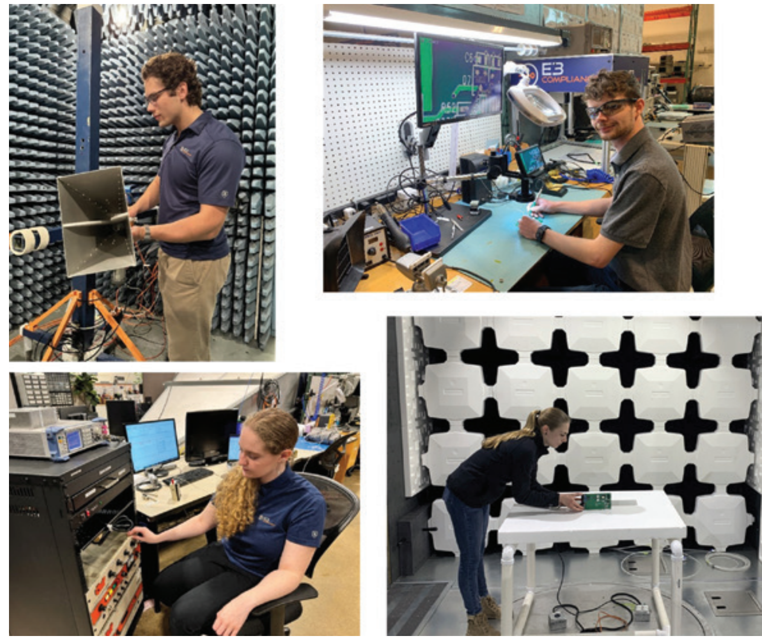


Figure 2: GUSV Co-op students at work

GRADUATE-LEVEL EDUCATION

In addition to employing co-op students, E3 Compliance also employs graduate students pursuing their master's degrees in part time roles. The company sponsors these students in what is called an industry sponsored graduate fellowship (IGF) program. This program allows them to be exposed to more advanced levels of engineering and physics within the same mentorship and lab environment as GVSU's co-op students.

Beyond the student employment experiences, E3 also sponsors multi-disciplinary senior design capstone projects that involve 5-6 students nearing the completion of their undergraduate degrees in engineering. Typically, the company sponsors one project each year that requires the students to design, build and test a system to enhance our EMC or High-Speed capabilities. One example is an automated EMC antenna mast which required mechanical, electrical, software and systems development and integration. This project supported the automation of radiated emissions testing in the company's EMC chambers.

Within the EMC industry, a large number of companies now seek the talent pool that graduates with this kind of experience coming out of college. The students gain hands-on experience that is hard to learn another way than by doing the work and being mentored by experts. The increased demand from industry supports the view that collaboration between academia and industry really does work.

OTHER COLLABORATIVE EFFORTS

There are several other ways that E3 Compliance supports student education with GVSU. Members of the company's engineer team collaborate with GVSU faculty to research EMC concepts and fundamentals by designing, fabricating and analyzing PCB designs with the university. Students or full-time employees design circuit boards in collaboration with GVSU, perform simulations and testing on the PCB assemblies and then co-author articles that are subsequently published showing what has been learned from the research.

All of the published information is non-proprietary and can be shared with the public. The designs are often showcased by students at the semi-annual Padnos College of Engineering (PCE) project day held in Spring and Fall each year on the GVSU downtown Grand Rapids, Michigan engineering campus. The recent project day presentations by GVSU/E3 co-op students are shown in Figure 3.

Some of the concepts studied include signal integrity, power integrity and EMC emissions and immunity topics. Several of the studies have also been used in lab experiments in GVSU's EMC engineering courses where students are expected to populate the boards and measure them in EMC chambers to evaluate performance and learn to fix non-compliances. This is an experience that most practicing electrical engineers wished they had while going through their undergraduate studies to better prepare them for industry.

E3 Compliance also supports GVSU's Amateur Radio Club (W8GVU). The university club has faculty and student members that learn about radio frequency communications and operate fixed and mobile radio gear. The company supports the club by designing and building "FOX" transmitter PCBs and step attenuator receiver boards (shown in Figure 4) to aid in the "Fox Hunts" in which students participate.

CONCLUSION

The collaboration between GVSU and E3 Compliance has profoundly affected the EMC education at the university. The joint research has led to the development of three new EMC courses, publication of two textbooks, [3,4], and over 100 publications. The content of the courses and the associated laboratories directly reflect the outcome of the collaboration.

The collaboration that has been established over the years between academia and industry at the GSVU EMC Center, has created an environment where students and industry both benefit and succeed. This program is unique and has resulted in many students graduating with EMC & High-Speed skills and experience that have allowed them to start their careers in reputable, global companies. Some of the students that go through the program have also been hired directly into the EMC Center as engineers who now play a lead role in the operations. The students have also had opportunities to co-author publications and present some of the findings from the EMC Center. Future plans include the establishment of an MSE program in Electromagnetic Compatibility combined with graduate assistantship and internship, currently under development.

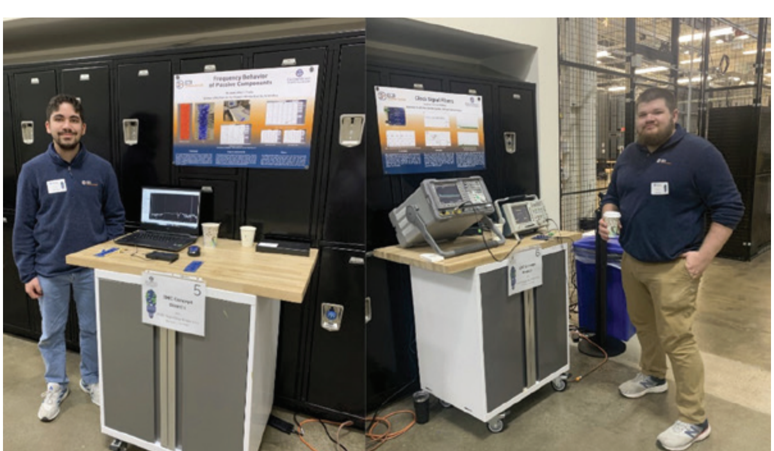


Figure 3: Project day presentations

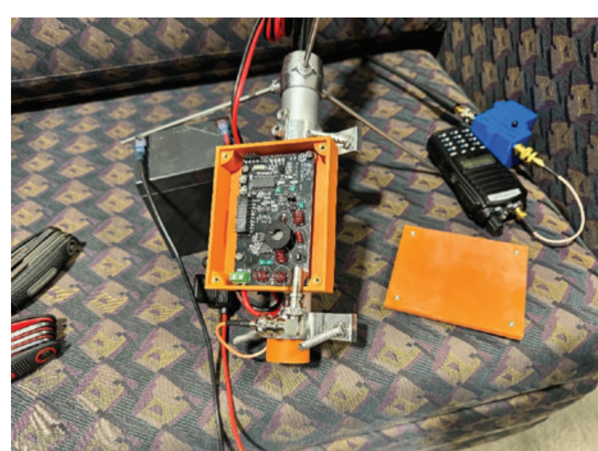


Figure 4: Amateur radio club FOX transmitter project

GAA TECHNOLOGY: NAVIGATING FUTURE ESD CHALLENGES IN MASS PRODUCTION

By Wen-Chieh Chen on behalf of EOS/ESD Association, Inc.

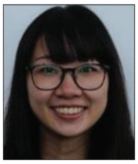
To continue Moore's law, transistor scaling needs to be enabled by geometry innovations. From the 22nm node, bulk FinFET, a multi-gate transistor built on a silicon substrate, has replaced planar FET and become mainstream for mobile SoC applications [1-3]. Beyond the 3nm nodes, bulk gate-all-around (GAA) technology has emerged as a promising transistor architecture, offering superior electrostatic and leakage control [4-8]. Vertically stacked horizontal nanosheets (NS) further enhance driving current per layout footprint [8-11]. CMOS technology scaling will no longer be limited at the transistor level to continue the roadmap further.

New scaling options in considerations of technology co-optimization (DTCO) and system-technology co-optimization (STCO) are being explored to achieve more tailored chip and enhanced system performance, such as a backside power delivery network (BS-PDN). This article examines the impact of double-sided connectivity with BS-PDN on ESD reliability.

BACKSIDE POWER DELIVERY NETWORK

BS-PDN was introduced as part of DTCO to enhance functional performance in logic scaling [12]. Metal routing is simplified by separating power and signal pathways, improving frontside (FS) signal integrity, and optimizing backside power delivery [13]. A high-density through silicon via (TSV) or power via is critical for double-sided connectivity between the silicon wafer's front and back sides. Thinning the wafer to just a few hundred nanometers is necessary to maintain TSV process quality by achieving a proper aspect ratio [14].

Figure 1 illustrates the simplified process flow for achieving a thinned silicon thickness of 300nm and double-sided connectivity with nano-TSV (nTSV) structures. However, reducing the silicon substrate thickness could challenge ESD robustness, as ESD protection devices rely on sufficient Si substrate volume for effective discharge and heat dissipation. Unlike fully depleted silicon-on-insulator (FD-SOI) technology, which allows an open buried oxide layer (BOX) to enhance ESD performance, this option is not viable for double-sided connectivity with BS-PDN [14].



Wen-Chieh Chen received the B.S. and M.S. degrees from National Chiao-Tung University, Hsinchu, Taiwan, in 2016 and 2018, respectively. She received the Ph.D. degree in electrical engineering from KU Leuven, Leuven, Belgium, in 2024. Wen-Chieh Chen is currently with imec as a resercher, Leuven, Belgium. Her research interests include mixed-voltage I/O circuit design and ESD device characterization in advanced sub-3-nm technologies and DTCO/STCO era.

IMPACT OF EXTREMELY THINNED SILICON SUBSTRATES ON ESD DIODE PERFORMANCE

Recent studies have examined the ESD performance of two typical protection diodes—shallow trench isolation (STI) and gated diodes—with extremely thinned silicon substrates [15]. Figure 2(a) on page 48 shows the simulation results of STI diodes with 300nm and 4.5µm substrate thicknesses. The diodes are stressed by a 100-ns TLP stress. The injected TLP current is 0.67A, corresponding to a 1-kV HBM event. The 4.5µm represents the conventional full Si wafer thickness because it is longer than the thermal diffusion length (~3µm) of

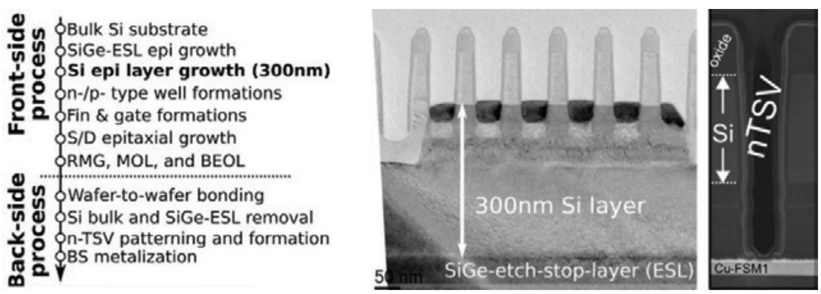


Figure 1

100-ns TLP stress [16]. The current density in the thinned STI diode is approximately twice as high as that of the thick diode. In Figures 2(b) and 2(c), the simulation results show that the thinned STI diode certainly fails at 0.67A TLP current, while the thick STI diode remains at a much lower temperature.

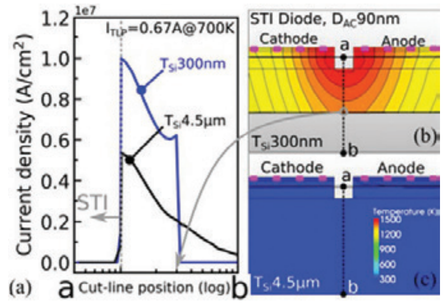


Figure 2

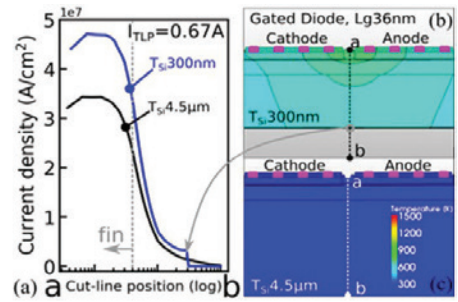


Figure 3

For gated diodes, the simulation results (Figure 3) indicate that current penetration beyond 300nm is minimal, suggesting smaller performance degradation compared to STI diodes. Furthermore, the lattice temperature in the thinned gated diode is much lower than in the thinned STI diode.

PROPOSED SOLUTION: ESD DIODES WITH ACTIVE BACKSIDE TECHNOLOGY

In response to these ESD challenges from substrate thinning and BS-PDN, active backside (BS) technology has been proposed by introducing a p+ epitaxial layer and BS contact patterning (Figure 4) [17]. The vertical diode can thus be enabled offering significant advantages, such as improved area efficiency and ESD current uniformity. Moreover, the vertical diode's design facilitates better thermal dissipation by incorporating backside metal layers (BSM) as heat sinks (Figure 5). This simulation decouples the impact of heat dissipation from the frontside metals (FSM).

Simulations show that the maximum temperature (Tmax) and normalized increased temperature (ΔTmax) of the vertical diode decrease with reduced silicon thickness, demonstrating substrate thinning is beneficial to vertical ESD diode, especially in extremely thinned Si substrate.

FUTURE ESD CHALLENGES IN DTCO AND STCO SCALING

Looking ahead, GAA technology is expected to evolve further. A recent proposal includes a fork-shaped transistor architecture to minimize spacing between p-type and n-type MOSFETs, offering superior scalability compared to current nanosheet architectures [12, 18]. Additionally, complementary FET (CFET) technology, which stacks n-type MOSFETs on top of p-type MOSFETs, eliminates the n-to-p separation bottleneck, significantly reducing the standard cell area footprint (Figure 6).

However, CFET technology presents two key challenges for ESD robustness. First, the thin nanosheet structure and absence of a body terminal limit ESD discharge through parasitic devices, forcing current to discharge through the active channel. Second, the complete isolation between n-type and p-type active regions complicates ESD diode implementation, requiring special process options that may not be compatible with standard flows.

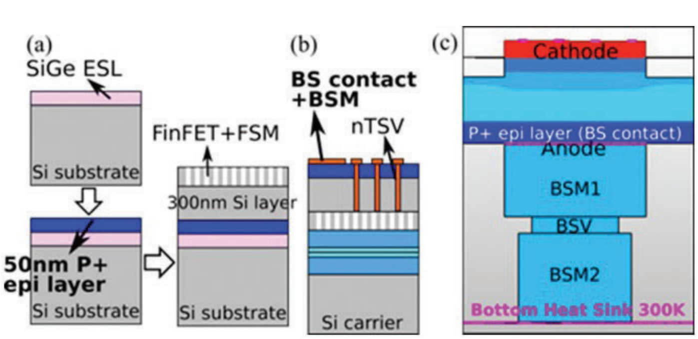


Figure 4

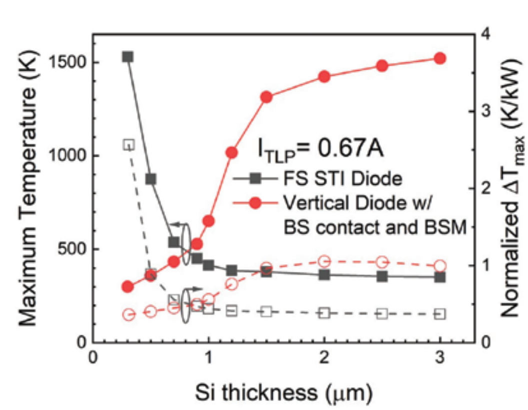


Figure 5

Figure 6

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