



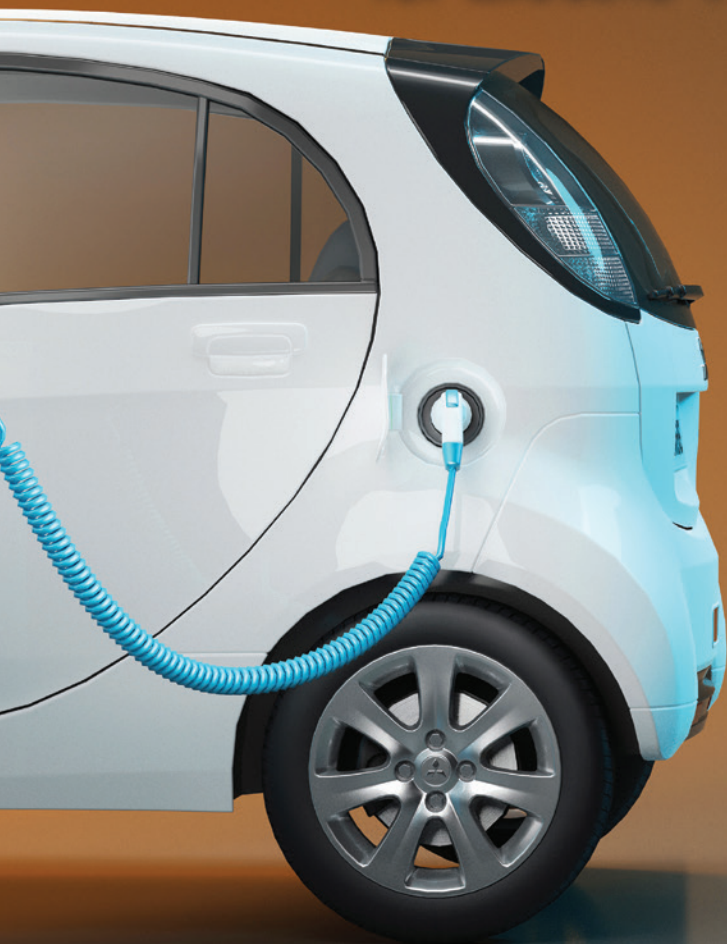
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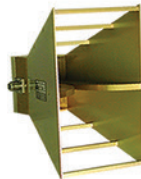
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8 EMC DESIGN TECHNIQUES FOR ELECTRIC VEHICLE POWERTRAIN MODULES *State-of-the-Art EMC Designs to Consider Before Your Next Module Project*

By Dr. Min Zhang

This article presents the EMC design techniques for electric vehicle powertrain modules. High voltage EMC regulations for powertrain modules are reviewed first to help understand associated design challenges. The design techniques are then demonstrated in detail to help engineers design a module that will pass the EMC requirements in the test chamber.



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By Christopher Semanson

Are you a new safety manager shopping power converters and wondering about the features listed under the functional safety section? Or are you a seasoned design and release engineer looking to start on a new ISO 26262 module? Either way, this article offers guidance in applying functional safety concepts to your next automotive design.



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This article discusses the legal and practical issues around the duty to warn and instruct and where to place safety information on the product and/or in the manual.



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FCC Implements New Penalties Under PIRATE Act

The U.S. Federal Communications Commission (FCC) can now penalize those parties that allow illegal radio broadcasting activities on their property.

According to the terms of an Order, the Commission is now authorized to propose fines of up to \$2 million to property owners and managers that house so-called pirate radio broadcasts on their premises or who knowingly

facilitate their operation. This authority falls under the scope of the recently enacted Preventing Illegal Radio Abuse Through Enforcement (PIRATE) Act.

Under this expanded authority, the FCC's Enforcement Bureau will first provide written notice to owners and managers that illegal broadcasts are believed to be originating from their properties, thereby giving them the opportunity to remedy the problem.

Depending on the response, the Commission has the discretion to take further actions, including levying financial penalties of up to \$100,000 per day with a maximum penalty of \$2 million.

In its Order, the Commission notes that this expanded enforcement authority is not an exercise of "administrative discretion" and therefore does not require a notice and public process to take place.

Material Found to Block Electromagnetic Waves

Researchers at Drexel University's Nanomaterials Institute have demonstrated that a class of thin, two-dimensional material has the potential to block electromagnetic radiation (EM), potentially laying the groundwork for a new generation of shielding materials.

According to a paper published in the scientific journal *Carbon*, the researchers found that one particular MXene, titanium carbonitride, provides an excellent shield against EM radiation. They determined that MXene not only blocks EM radiation but absorbs EM signals rather than merely reflecting them back. In their testing, samples of cotton and linen dipped into a MXene solution including titanium carbonitride blocked more than 99.9% of EM signals.

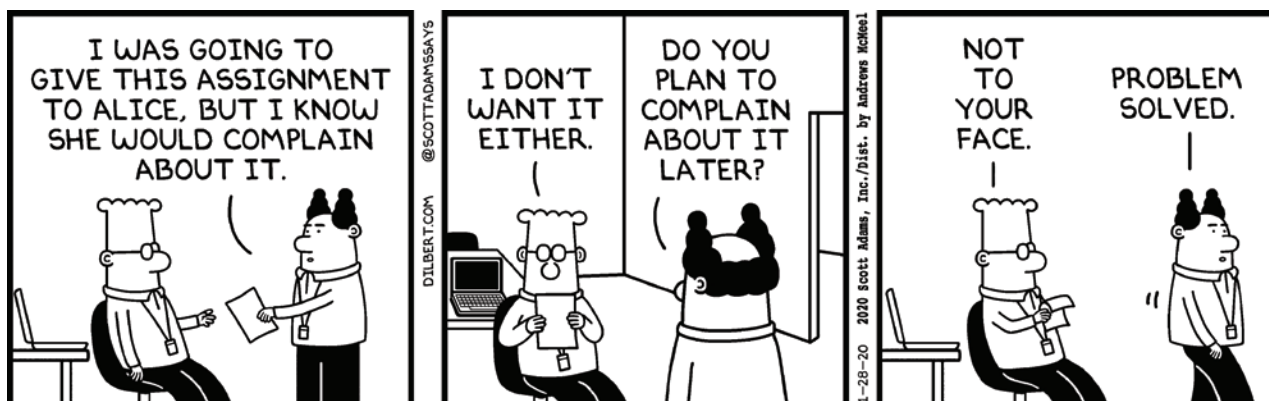
The Drexel University researchers also found that the MXene produces a durable coating that doesn't require chemical additives or other pre-treatment or post-treatment processing. Further, MXene-treated materials lose only small amounts of their shielding effectiveness over time.

EU Pushes for "Right to Repair" for Products

As part of the widespread effort to boost environmental sustainability efforts in the European Union (EU), the EU Parliament has passed a resolution calling on the EU Commission to grant consumers a "right to repair" a variety of products, including electrical and electronic devices.

The EU Parliament suggests a number of methods that manufacturers could adopt to extend the life of their products. The suggestions include extending product guarantee periods, offering guarantees for replacement parts, and giving consumers easier access to information on maintenance and repair options.

The Parliament also calls on the Commission to implement regulatory provisions that would support more sustainable production methods by product manufacturers, and a greater emphasis on reducing practices that shorten the effective life of a given product. The Parliament also recommends increased support for the deployment of more robust second-hand markets for used products.



FCC Denies Huawei's Appeal

The U.S. Federal Communications Commission (FCC) has denied an appeal from Huawei Technologies to reconsider its designation of the company as posing a national security threat to the safety of the U.S. communications network.

In a Memorandum Opinion and Order, the Commission defends its June 2020 action to officially ban the use of monies from the Commission's Universal Service Fund to purchase equipment or services from Huawei and other companies posing a threat to national security, noting the "overwhelming evidence of Huawei's close ties to the Chinese Communist Party and China's military and intelligence apparatus."

According to the FCC, "the Commission's review of the record found that Huawei is susceptible to Chinese government pressure to participate in espionage activities and that Huawei's close ties to the Chinese military present significant risk." The Commission also cites bans by other countries against the use of Huawei equipment as evidence of the potential threat.

According to the FCC, "the Commission's review of the record found that Huawei is susceptible to Chinese government pressure to participate in espionage activities and that Huawei's close ties to the Chinese military present significant risk."

Huawei filed an Application for Review in late July, challenging the FCC's June Designation Order and arguing that the Commission lacked the authority to do so and that the Commission's Public Safety and Homeland Security Bureau violated provisions of the Administrative Procedures Act in making its decision. However, in its Memorandum and Order, the Commission concludes that its decision to ban Huawei was based on a thorough assessment of the threat potential and that it acted within the full scope of its authority.

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State-of-the-Art EMC Designs to Consider Before Your Next Module Project

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By Dr. Min Zhang

Powertrain modules are one of the key differentiators in the EV industry. Both vehicle manufacturers and Tier-1 suppliers have been spending considerable resources researching and developing state-of-the-art technologies for EVs. The current trend is to achieve a more compact module design with higher power density and system efficiency. For instance, the Nissan LEAF has achieved a very compact e-powertrain module design by integrating an on-board charger (OBC), a DC-DC converter, and a junction box with the electric drive unit (EDU) [2].

This article presents the EMC design of a powertrain module, which consists of an electric motor, an inverter, and a mechanical gearbox. The electric system diagram of an EV powertrain module is illustrated in Figure 1.

The importance of design engineers taking a system-level overview of an EV powertrain module was presented in my previous work, “Demystifying EMC in an Electric Vehicle’s Drive Unit” [3]. It is critical to factor in EMC design considerations at an early stage so as to achieve the overall system design goal. The high voltage (HV) EMC regulations and requirements present a daunting task for not only new entrants but also for well-established companies in the automotive industry. Therefore, we’ll first review in this article the HV standards and regulations that apply to electric powertrain modules. Then, we’ll highlight EMC challenges in the powertrain module design and demonstrate design techniques to address potential EMC issues. Engineers will then have a better understanding of how to design a

module that will pass the EMC requirements in the EMC test chamber.

HV EMC STANDARDS AND REGULATIONS FOR EV POWERTRAIN MODULES

CISPR 25:2016 [4] serves as a general EMC guideline for automotive developers, although vehicle manufacturers often have their own proprietary EMC specifications [5]. Annex I of CISPR 25 defines test methods for shielded power supply systems for high voltages in electric and hybrid vehicles. CISPR 36:2020 [6] was released recently, and it defines the test methods for electromagnetic field emission on a vehicle level. A component-level electromagnetic field emission test to reflect this standard is expected to be available soon from vehicle manufacturers.

(Note that on-board chargers (OBCs) require a different set of test methods that are related to charging and are not covered in this article. Also not included here is a discussion of low voltage (LV)-associated EMC tests, electrical tests, or electrostatic discharge (ESD) tests.)

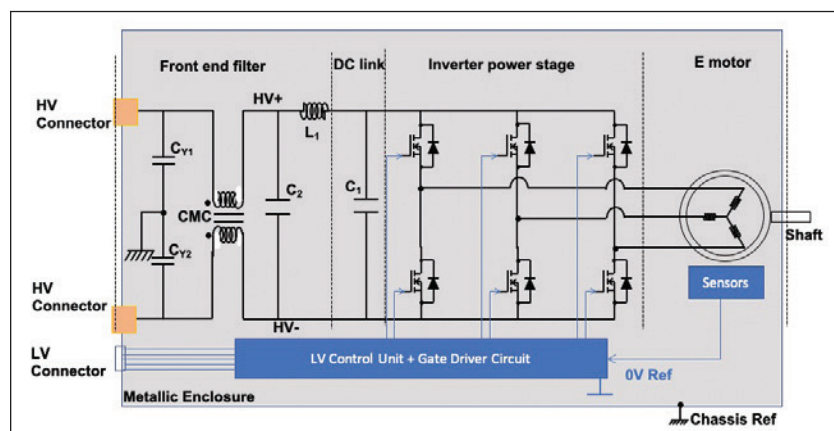


Figure 1: System diagram of an EV electric powertrain module

HV Component Emission, Immunity, and Transients

Annex I of CISPR 25 defines both conducted and radiated emission limits for shielded HV systems, and unshielded systems shall comply with the same limits as shielded systems. Annex I of CISPR 25 also introduces the HV/LV coupling attenuation test. This test is performed while the equipment under test (EUT) is unpowered. Essentially the test result is the $-S_{21}$ plot of the EUT by an impedance analyzer. For good system decoupling behavior, the Class A1 or A2 in requirements for minimum coupling attenuation given in [4] need to be achieved.

For RF-immunity, the ISO 11452 series is relevant for vehicle component tests. The newest revisions of subparts under ISO 11452, such as ISO 11452-4:2020, include HV component test setups and high voltage artificial networks (HV-ANs). Other subparts are expected to adopt these HV component requirements accordingly.

ISO/TS 7637-4:2020 deals with transient emissions and transient immunity on HV lines.

Electric and Magnetic Field Strength

The standards SAE J551-5 [7] and GB/T 18387-2017 [8] define limits and test methods in the U.S. and China, respectively, for the magnetic and electric field emissions from electric vehicles. CISPR 36:2020 [6] deals with electromagnetic field emissions. A recent comparison study between GB/T 18387-2017 and CISPR 36:2020 on the magnetic field radiated disturbance test requirements has found that GB/T 18387-2017 is more stringent [9].

Magnetic field exposure will be the most critical aspect for electrical vehicles because of the high

currents associated with their electric drives. To cover this aspect also on the component level, test methods have to be defined.

Human exposure to magnetic fields is tested in accordance with a Guideline issued by the International Commission on Non-Ionizing Radiation Protection (ICNIRP). IEC TS 62764-1 defines the measurement procedures for magnetic field levels generated by electronic and electrical equipment in the automotive environment with respect to human exposure.

A summary of the HV EMC test is listed in Table 1.

EMC CHALLENGES

A more compact, larger power rating, and higher efficiency powertrain module generally means more EMC challenges.

High Voltage

Currently, the most common HV rating adopted by modern automotive manufacturers is 400V (Audi e-tron, Tesla, Nissan Leaf, etc.). The Porsche Taycan is the first EV in the market to have adopted an 800V power system [10]. For the same power rating, increasing the voltage reduces the current in the system, resulting in reduced copper loss (I^2R loss). Therefore, higher voltages correlate with an increased system efficiency. However, the HV rating of a powertrain module is limited by factors such as the voltage ratings of commercially available power electronics devices, the insulation breakdown of HV cables, worse EMC performance, and so on.

The roadmap for the next generation of power electronics devices for powertrain modules has

HV EMC Test	Reference
RF Conducted & Radiated Emission	Annex I, CISPR 25:2016 Edition 4
Electric and Magnetic Field Strength	Component test plan shall reflect vehicle test requirements GB/T 18387/2017 or CISPR 36:2020
HV Transient Emission and Immunity	ISO/TS 7637-4:2020
Human exposure to Magnetic Field	ICNIRP Guideline
RF Conducted & Radiated Immunity	ISO 11452 Series
HV LV coupling	Annex I, CISPR 25:2016 Edition 4

List only consists of HV EMC tests, LV, electrical and ESD tests are not included

Table 1: List of HV EMC tests for powertrain module [1]



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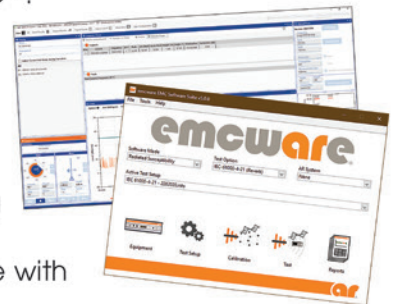
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indicated a breakdown voltage level beyond 1000V. It won't be long before most of the automotive design houses to move to 800V (and above) systems for the benefit of achieving higher efficiency. This predictable trend also poses great challenges for EMC design. As voltage level doubles (from 400V to 800V, for instance), and assuming the same parasitic characteristics of a design, noise levels associated with electric field will increase because of the high dV/dt characteristics.

Another great challenge associated with high voltage systems is safety. EMC and safety cannot be discussed separately in an HV system. Global Technical Regulation on Electrical Vehicle Safety (EVS) [11] defines the maximum capacitor energy that may be stored in the Y-capacitors to be 0.2J. This hard limit has a profound impact of front-end input filter design of all HV modules because Y-capacitors are very effective filters for broad band noise attenuation, particularly in the lower frequency range (starting from 300kHz).

This means that when voltage level doubles, the available

Y-capacitance value drops by 75% according to Equation 1:

$$E = 0.5 \cdot C_Y V^2 \tag{Eq. 1}$$

where E is the total energy stored in the Y-capacitor, C_Y is the available Y-class capacitance, and V is the upper band of HV system nominal voltage.

The relationship between noise level (as represented by common-mode current) and available Y-capacitance is illustrated in Figure 2.

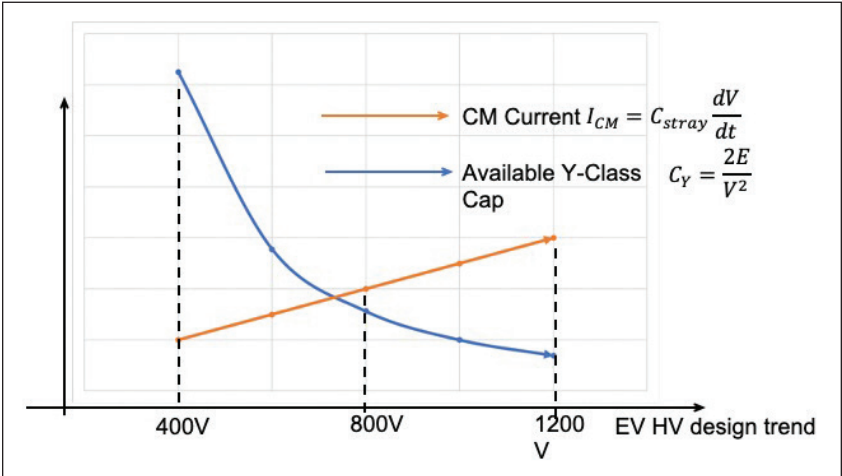


Figure 2: As voltage level increases, common-mode noise increases proportionally while the available Y capacitance reduces in an inverse square trend

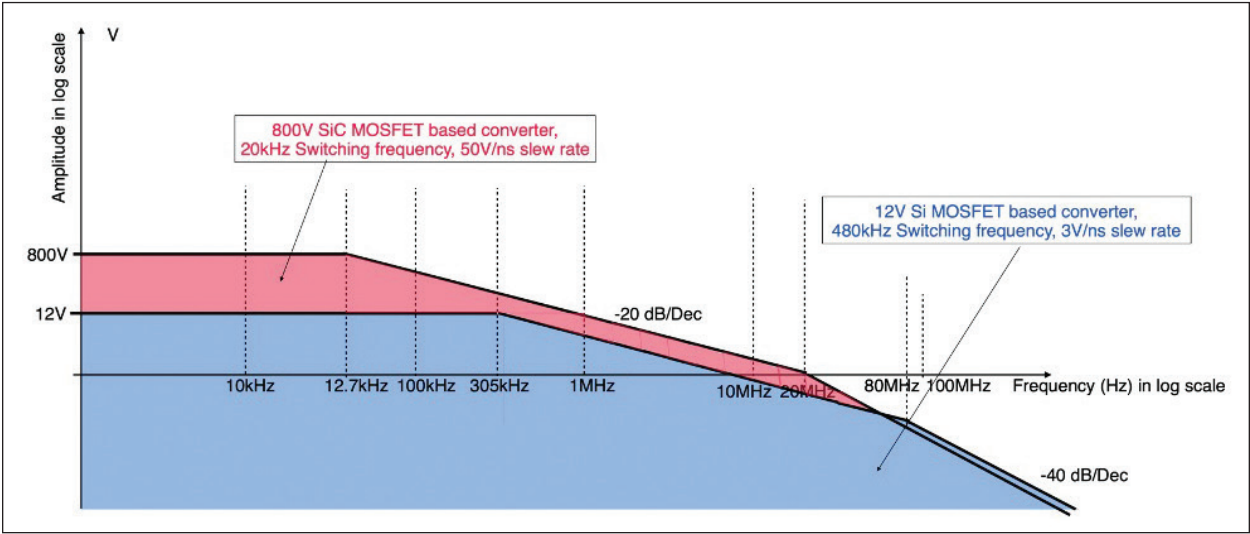


Figure 3: Switching device noise profile comparison

High Power/Current

Since the powertrain module is the performance unit of a vehicle, its power rating directly determines the acceleration rate, the horsepower, and the torque of a vehicle. Given a defined voltage rating of a powertrain module, higher power means higher current. As current is directly related to the magnetic field, higher power also means an increased magnetic field for a vehicle.

As the electric motor and inductors in the inverter are both inductive, higher current also means higher transient behavior caused by sudden state change. The back electromotive force (EMF) or kickback voltage caused by $L \cdot di/dt$ can stress or destroy components if not contained and send huge voltage spikes propagating on the HV bus line.

Fast Switching Power Electronics Devices

Insulated-gate bipolar transistors (IGBTs) were adopted in the early days of powertrain modules (such as the one in an earlier version of the Tesla Model S). The switching frequency of an IGBT-based power system is theoretically limited to 20kHz. The thermal concern of an IGBT often limits its switching frequency below its theoretical value. Wide-band-gap devices such as SiC MOSFETs have recently started replacing IGBTs as the device of choice thanks to their fast switching speeds (hence low switching losses) and better thermal characteristics.

Switching frequencies of 20 kHz and above could be comfortably achieved with SiC MOSFET-based powertrain module.

The downside of adopting wide-band-gap devices is the increase in electromagnetic interference (EMI)-related issues caused by their faster switching events. The rise time of a SiC MOSFET can be as small as a few nanoseconds, leading to a slew rate of 50-200V/ns [12]. To enable such fast speed characteristics, gate drivers are equipped with short high peak pulse current features, which could also pose EMI issues.

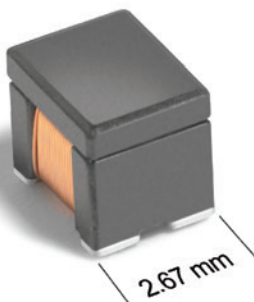
More SMPS and ICs

To provide power to microprocessors, gate drivers, and analog and digital integrated circuits (ICs), multiple power suppliers are often integrated into the design of the control unit board, with switched-mode power supply (SMPS) units the most common.

SMPS units such as buck and boost converters in the automotive application often have a switching frequency range between 150kHz and 500 kHz. The rise and fall time of the switches can be as short as a few nanoseconds. The noise spectrum shows less energy compared with power switching devices but covers a much wider frequency range. Figure 3 demonstrates the switching noise profile between an LV buck converter and an HV inverter.

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Bearing Current

Bearing currents are mainly caused by electrostatic discharges, magnetic asymmetries (caused by unbalanced three-phase windings), and common-mode voltages paired with high switching rates [13].

Bearings in an electric motor have moving metal balls or rollers in fixed metal shells. Very thin layers of lubricant sit between the two parts which therefore have a high capacitance and can carry high displacement currents. Because the lubricant is so thin, and because the bearings are not perfect, there can be an occasional electrical breakdown and even direct touching of the two metal parts. Therefore, the bearing current is partly capacitive, which gives a pulse of current during every switching transition and partly random high current spike [3]. This random breakdown can cause very high random peak currents that can give high quasi-peak noise in the EMI scan.

Bearing current can cause an electric motor’s bearings to deteriorate, hence reducing the lifetime of the powertrain. Bearing currents that circulate in the powertrain also cause conducted and radiated emissions, as shown in Figure 4.

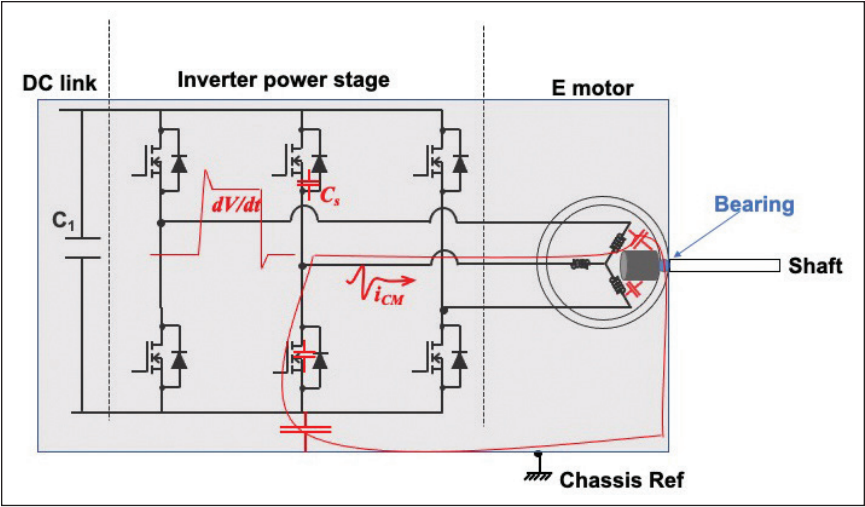


Figure 4: Bearing current caused by fast switching circulates through parasitic capacitance

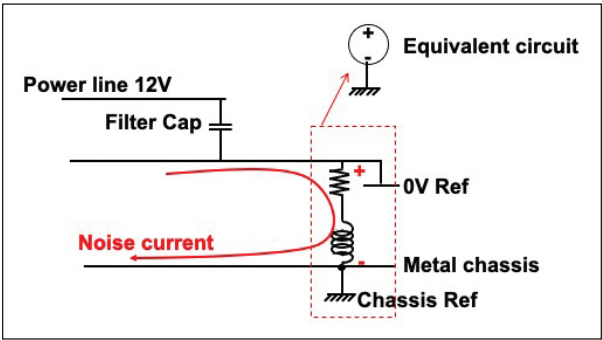


Figure 5: Connection between 0V Ref and Chassis Ref creates impedance for RF noise currents

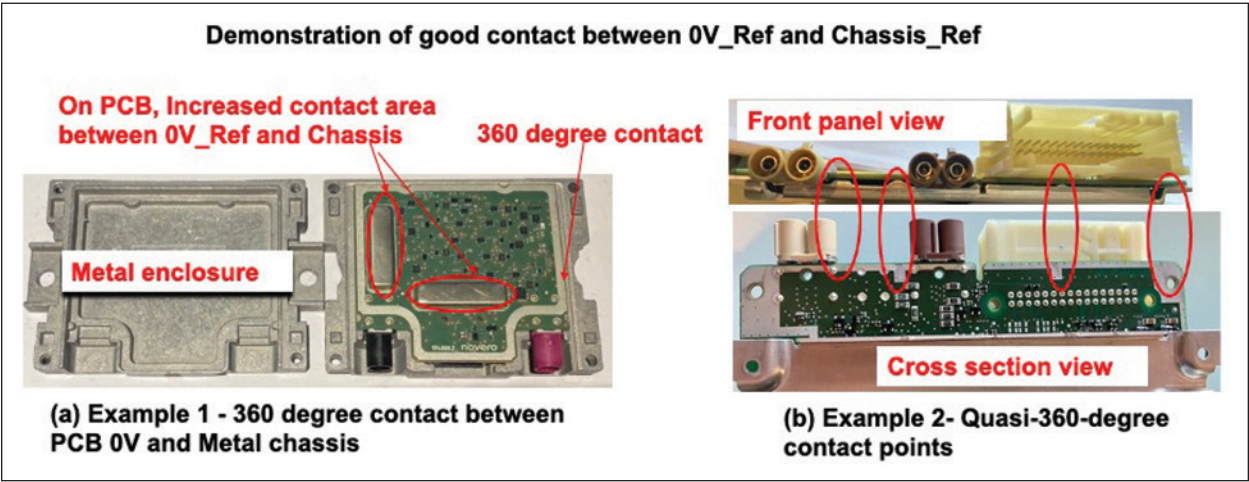


Figure 6: Demonstration of good contact between PCB 0V ref and chassis reference to reduce inductance

EMC DESIGN TECHNIQUES IN ELECTRIC POWERTRAIN MODULE

Grounding Design

It is not uncommon to see many ground symbols in one module design, even though the point of clarifying the use of the term “ground” has been stressed by many EMC experts [14] [15]. One recent project that I’ve reviewed had more than 5 ground symbols in one schematic. It is very confusing to see all these symbols in the first place, not to mention how the grounds are connected.

In Figure 1, the term “reference” is used rather than the term “ground.” It should be noted that circuit grounds are not necessarily the same as EMC grounds. To keep it simple and clear, there can only be one EMC ground, which is the metal chassis of the unit, or what we call the RF reference. The metal enclosure of a module has contact points to the vehicle chassis (either through direct bonding or mechanical fixtures); therefore, we treat the metal enclosure as a chassis reference.

The HV-line is the HV design reference, and it should be isolated from the vehicle chassis reference (either by dielectrics or by Y-capacitors). LV designs should have 0V as the reference points, and that should be the only design reference point. The idea of splitting analog and digital ground points is based on misconceptions and is not a good design approach [16].

The connection between the 0V reference (either on a PCB or a connector pin) and the chassis reference will introduce inductance [16]. The RF currents will inevitably flow in those inductances, leading to noise voltages that will help drive emissions. This is shown in Figure 5. As a result, efforts to minimize the inductance of the connection should be made in the module design. Among the schemes that reduce inductances between two reference points, the most effective way is to increase direct contact areas between the 0V Ref and Chassis Ref. This is demonstrated in Figure 6. Most of the time, multiple contact points along the edges and around corners of a PCB create a quasi-360-degree contact.

Connector Design

HV cables of a powertrain module are usually shielded, and shielding terminations have closely-spaced



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The future is here! With the increasingly sophisticated technology in our homes and industry — as evident in modern personal electronics, mobile devices, medical equipment, and automobiles — the potential for electromagnetic interference has accelerated significantly. Today's cars are essentially computers on wheels with varying degrees of automated control and “infotainment” capabilities. Testing of these emerging technologies to ensure safety and reliability has never been more important — or challenging. ETS-Lindgren's ability to provide turnkey systems, create real-world test scenarios, troubleshoot potential failures, and maximize the chance of passing standards within the allotted time and budget helps our customers bring life-changing products to market — faster. With decades of experience in compliance testing and measurement, ETS-Lindgren boldly addresses the future of EMC performance — Beyond Measure.

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contacts (360 degrees) to the module enclosure [17]. The reason for having a low impedance bond is the same as what we explained in the previous section. However, the mechanical quality of the contactor design needs to be considered very carefully because high temperatures, aging, vibration, and chemical ingress can damage the bonding configuration over time. An example of a failed shielding connector is shown in Figure 7.

Front-end Filter Design

The front-end filter design is crucial for electric powertrain modules as it helps to block the noise from the inverter power switches. It also suppresses the noise traveling from outside of the module enclosure via the HV DC wirings.

There are many types of front-end filters, including the two-stage filter shown in Figure 1. In Figure 1, the L_1 and C_2 configuration forms the first-stage low-pass filter. The second-stage filter consists of a CMC and Y-capacitors. Notice that, together with the DC link capacitor C_1 , the first-stage filter effectively acts as a p (C-L-C) filter.

Nanocrystalline Core

Due to its high voltage and high current characteristics, the saturation of the magnetic core needs to be accounted for when designing HV inductive components. Nanocrystalline materials enjoy a very high saturation magnetization. Because windings that carry such high currents

will inevitably increase the size and the weight of a module, toroid or oval shape nanocrystalline cores are typically used in common-mode suppression chokes in automotive applications. They are effective in the frequency region between 150kHz and 120MHz.

For powertrain applications, cores can be either used on a single power line (HV+) as an inductor or on both power lines as a CMC. It should be noted here that the designers might find CMCs such as nanocrystalline cores are not needed due to other good EMC practices in place. However, it is best to allow for Murphy’s law and to design properly from the start so that the cores can be added later if necessary [18].

Y-capacitors

Compared with the use of CMCs, the benefits of using Y-capacitors include great high-frequency conducted emission attenuation (generally effective starting from 5 MHz), smaller sizes, lighter weight, and no saturation concerns. The connection of

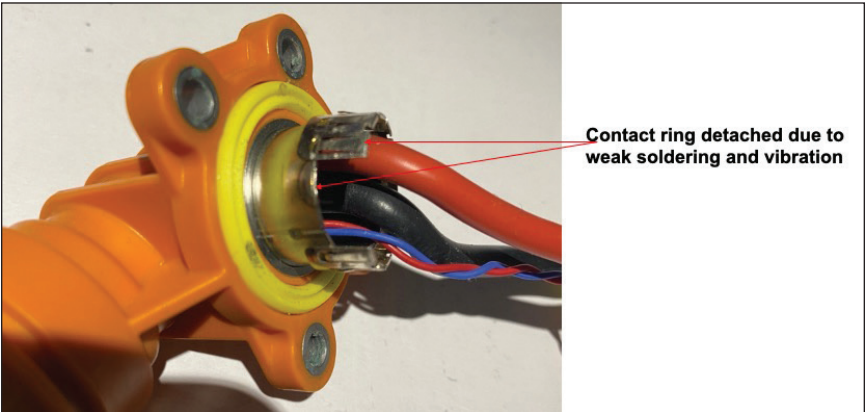


Figure 7: An example of weak contact of shielding connector

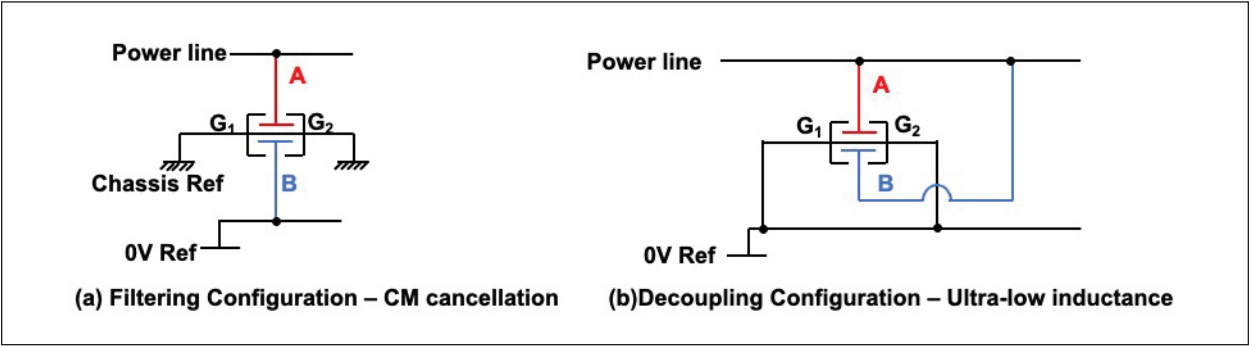


Figure 8: X2Y capacitor connections in an electric system, (a) filtering configuration; (b) decoupling configuration [19]

Y-capacitors to the chassis reference should also be designed to achieve very low impedances. The internal equivalent series resistance (ESR) and equivalent series inductance (ESL) are the main factors that affect the effectiveness of Y-capacitors. The imbalance of the impedance of two Y-capacitors also affects the common-mode filtering performance. These drawbacks can be compensated by layout or by using alternative parts such as X2Y capacitors.

X2Y capacitors

X2Y capacitors (see Figure 8) [19] provide great EMI filtering and can be used to replace CMCs (Figure 8(a)) in applications where size, weight, and cost are design constraints. Two capacitors are balanced shunt so as to create a cancellation of the mutual inductance. The X2Y capacitors also provide a shielding effect. Alternatively, as Figure 8 (b) shows, the X2Y capacitors can be configured as decoupling capacitors with ultra-low inductance. Currently, 500V X2Y parts are not automotive qualified, but it is worth paying attention to this component as manufacturers will probably upgrade the high voltage parts so they are AEC-Q200 qualified.

DC Link Design

The DC link includes the HV DC bus bars and DC link capacitors. The DC bus bars should be designed as short as possible and in close proximity to each other to reduce the loop area between them. DC link capacitors should be designed to cope with high voltage, high-frequency switching ripples, and high temperatures. The capacitance value should be large enough for the full power operation of a powertrain module. Low ESR and ESL film capacitors and electrolytic capacitors are often used in powertrain modules.

Film Capacitors

Film capacitors are widely seen in powertrain module design due to their high performance and reliability. The “brick” size of film capacitors limits the design freedom; therefore, it is important for design engineers to engage film capacitor suppliers early in the design stage. Parameters such as ESL and ESR are crucial for EMC, as self-inductance of the capacitor is caused by geometry of the component (such as capacitor wrapping, upper conductor rail, and lower conductor rail).

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Electrolytic Capacitors

In some cases, manufacturers use a high-performance electrolytic capacitor bank as the DC link. The current flowing in the self-inductance of a capacitor creates a magnetic field. The smaller the self-inductance, the smaller the magnetic field for a given current, and vice-versa. Connecting a number of capacitors in parallel connects their self-inductances in parallel. But, if they are too close together, their magnetic fields will interact since the overall inductance is not reduced when the magnetic fields are all in the same direction. As a result, the overall inductance is not reduced to $1/N$ (as we might expect from circuit theory or SPICE simulations).

But if we arrange N -paralleled capacitors closely together, and so that they are alternately reversed or so that the self-inductance of the capacitors are in perpendicular position to each other, their magnetic fields will tend to oppose each other, canceling them out to some extent (as now mutual inductance is kept at a minimum). Since weaker fields mean lower inductances, we may be able to achieve greater than a $1/N$ reduction in overall self-inductance [20].

Figure 9 demonstrates the magnetic field coupling due to mutual inductance between capacitors. Examples are given to show how layouts of arrays of capacitors can achieve lower overall inductances by their magnetic fields and cancel each other out, to some extent.

Inverter Power Electronics Devices Design

The EMC design consideration of using wide-band-gap devices such as SiC MOSFETs was introduced in [3]. The subject itself could easily inspire a few dedicated articles. Therefore, we only summarize here some of the best design practices.

Because the common-mode current I_{CM} can be calculated by Equation 2:

$$I_{CM} = C_{stray} \cdot dV/dt \quad \text{Eq. 2}$$

where dV/dt is the slew rate of the switching device, C_{stray} is the stray (parasitic) capacitance and can be calculated by Equation 3:

$$C_{stray} = C_{FET} + C_D + C_L \quad \text{Eq. 3}$$

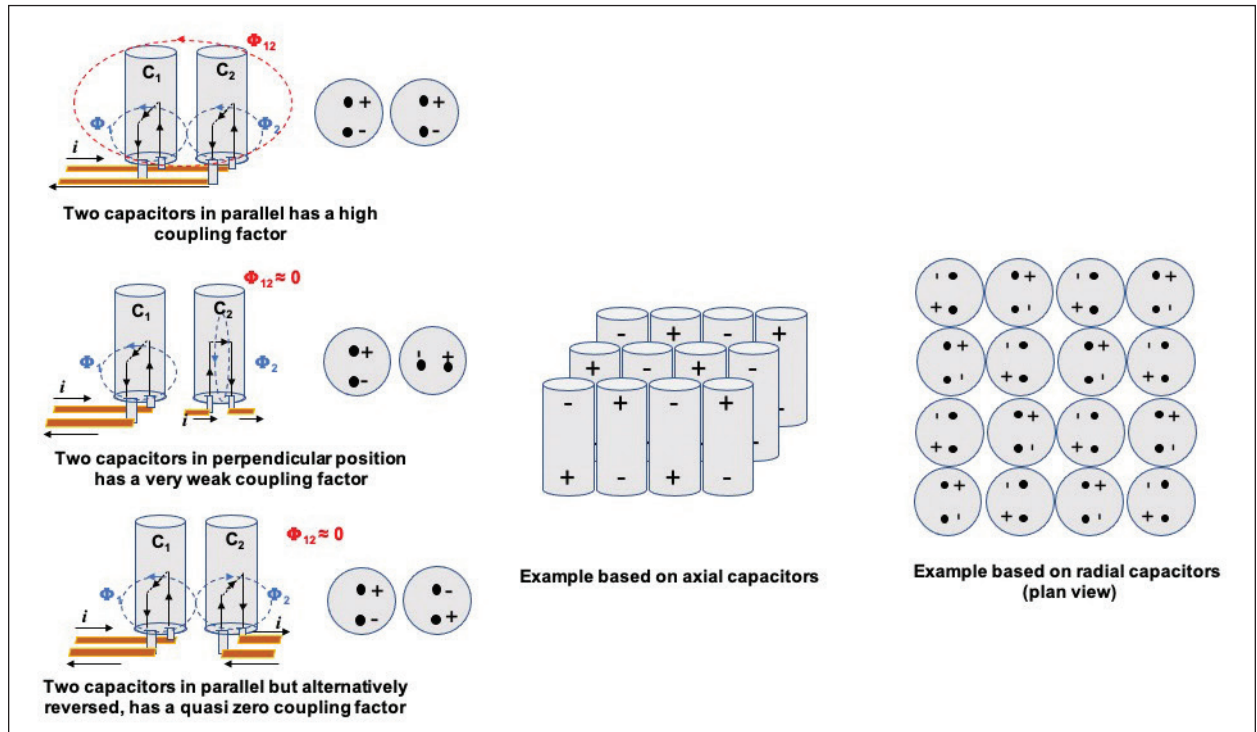


Figure 9: Layout rules for a number of electrolytic capacitors

where C_{FET} is the SiC MOSFET parasitic capacitance (predominantly drain to source capacitance C_{DS}), C_D is the free-wheeling diode capacitance, and C_L is the parasitic capacitance caused by layout (for instance, the capacitance between the device and a heatsink).

Reducing the slew rate helps to mitigate spikes or ringing, but at the cost of increased switching loss. Reducing C_{stray} can be achieved by selecting optimized packaging and applying good layout practice. The ringing of the switching is caused by the L - C circuit resonance, and good layout practice to achieve lower stray inductance (e.g., device connections to the bus bar) helps reduce the ringing.

To share the large current, N SiC MOSFETs are placed in parallel. This configuration results in $1/N$ $R_{DS(ON)}$, allowing very low conduction loss. The total ESL of the devices might not be as low as $1/N$ for the same reason we explained when we talked about multi capacitors in parallel. However, ways of shortening the connections, such as connections between the devices and bus bars and the connections between the devices and motor windings, can minimize the inductance.

Figure 10 on page 20 demonstrates the SiC MOSFETs layout in the powertrain module of a Tesla Model 3. Four MOSFETs are put in parallel to form one switching block. Altogether, there are 24 switching devices in a very tight package space, with short connections to minimize the parasitic inductance. Direct sintering of the SiC MOSFET to the bottom of the heat sink helps remove the heat efficiently.

Techniques such as using SiC Schottky diodes in parallel to SiC MOSFETs to eliminate the reverse recovery charge effect were presented in [3]. But more manufacturers are integrating very fast and robust intrinsic body diode into the device package; hence separate antiparallel diodes are not required. Generally, locating decoupling capacitor arrays close to the switching devices is also crucial to reduce the ringing effect of the switching events.

Inverter Control Unit Design

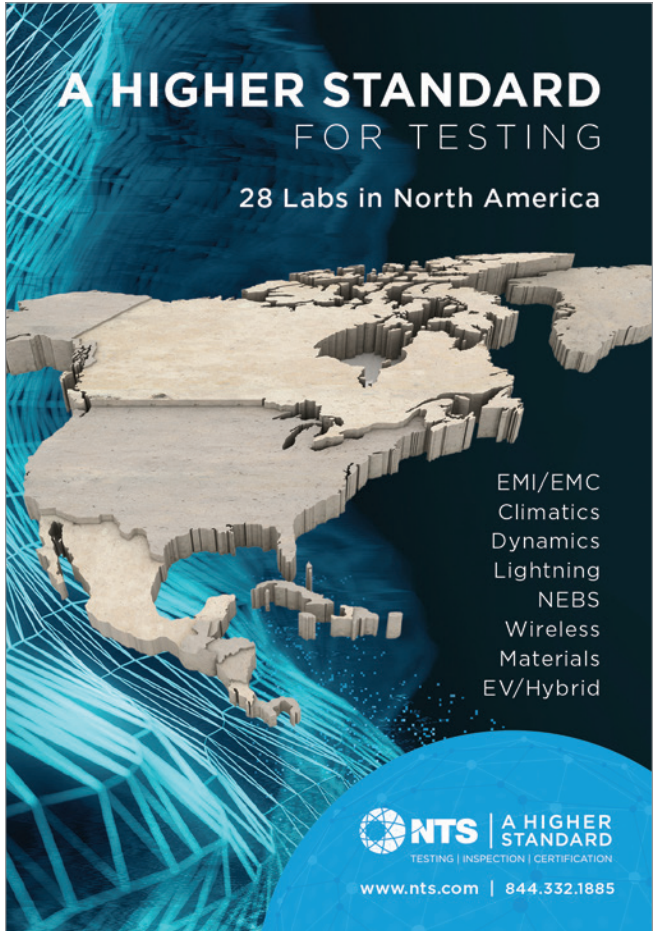
Compared with the power stage, the low voltage control unit often has various high-frequency noise sources. The noise spectrum of a control unit covers a much wider range, as listed in Table 2 on page 20.

The EMC design follows guidelines similar to those we previously discussed, which is to apply good layout practice, design front-end and output filters on both power and signal lines, and apply sufficient global and local decoupling capacitors.

CMCs are often seen in the LV power system design, and the X2Y balanced capacitor was introduced previously in this article. Although the HV (above 400V) X2Y part is not automotive qualified, there are plenty of AEC-Q200 qualified parts [19] that can be used in the control unit of a powertrain module. [21] introduced X2Y capacitor in an SMPS design.

Bearing Current Mitigation

At the design stage, there are two approaches one can apply to mitigate the bearing current, as described in the following paragraphs.



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Hardware Mitigation Schemes

Ceramic bearings or hybrid bearings (a combination of steel rings matched with ceramic) are good candidates for an electric motor because of their mechanical characteristics. Because ceramic is an electric insulator, it can reduce the bearing currents and mitigate the electrical arcing [22]. Alternatively, the rotor of an electric motor can be directly grounded with a small thrust bearing that can easily be changed [13] [23]. This grounding also helps prevent the motor shaft from radiating due to the stray RF currents induced into it.

Other methods of mitigating the common-mode noise, which contributes to the shaft voltage and bearing current, are to add the common-mode filter along the motor windings. Shielded cables also help [13]. But for a compact module design, these methods are generally not considered.

Software Mitigation Schemes

Apart from using the hardware approach, certain switching schemes can be adopted to reduce the common-mode voltage of an electric motor, therefore reducing the bearing current. The method proposed in [24] proved to achieve both high performance and low common-mode voltage and current but unfortunately does not include a spectrum analyzer evaluation of the results as compared with normal PWM schemes. The

implementation of the proposed method also requires an in-depth understanding of the motor drive system.

CONCLUSION

In this article, we reviewed the HV-related EMC regulations for powertrain modules in EV applications. We then discussed the design challenges they present and demonstrated the EMC design techniques that can be implemented at the design stage.

Most of the techniques introduced in this article follow EMC design principles, such as reducing parasitic parameters, 360-degree shielding, and bonding. New passive components (such as nanocrystalline core and X2Y capacitors) can also be considered, as well as software schemes to mitigate the common-mode noise. By adopting these design techniques, engineers can be more confident that the powertrain module they design will pass the EMC tests, potentially even the first time around! 🇨🇳

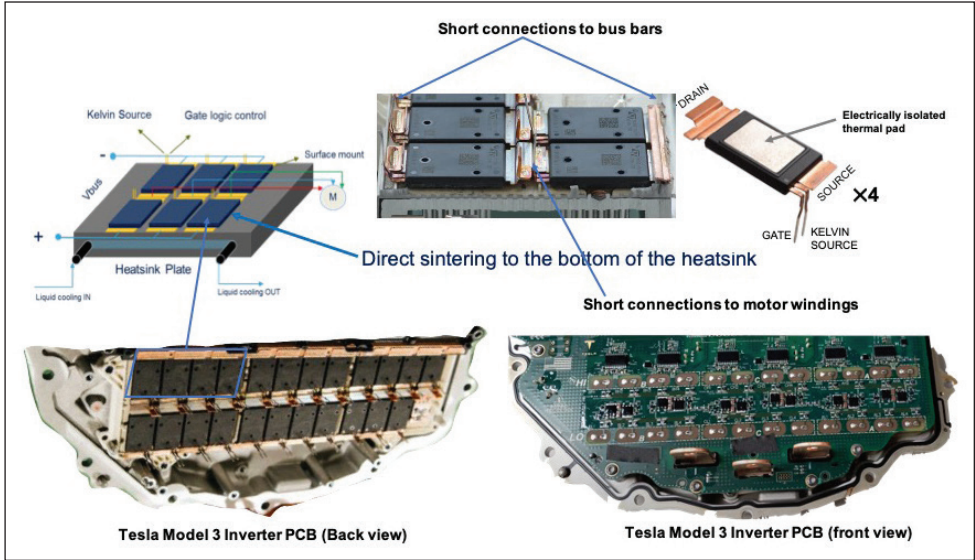


Figure 10: SiC MOSFETs layout in Tesla Model 3 powertrain inverter

LV Electronics	Frequency Range
Switched Mode Power Supply (SMPS)	150 kHz – 2 MHz
Communication Lines (LIN, CAN, FlexRay, etc)	10 kHz – 2.5 MHz
Microcontroller/DSP	200 MHz – 600 MHz
Digital Isolator	200 kHz – 10s of MHz

Table 2: List of LV electronics frequency range in powertrain module

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APPLYING ISO 26262 TO POWER MANAGEMENT IN ADVANCED DRIVER ASSISTANCE SYSTEMS

Understanding the Tools and Methods Used to Develop Functionally Safe Power Systems for ADAS Applications

Over the last decade, automotive original equipment manufacturers (OEMs) like Ford, GM, and Tesla have been at the forefront of mobility and advanced driver assistance systems (ADAS), jockeying for a leadership position in this hotly contested, quickly developing field. As these systems advance, with them comes an increase in the number of semiconductor components in the vehicle to support devices like cameras, radars, and modules used to make decisions based on their information.

This has provided an opportunity for semiconductor manufacturers to increase their market share, allowing them to pivot from their traditional base microcontroller (MCU) offerings to highly integrated system on chip (SoC) processors, memory, and power devices. However, as the industry evolves, the question remains for both consumers and OEMs alike: "How can we standardize the development and design of these components across the industry, such that we can satisfy the risk that comes along with these components, while confidently claiming the part functionally safe?"

Enter the first edition of ISO 26262, Road vehicles—Functional Safety, which was the industry's attempt at standardizing the development of the components of these large systems to minimize both:

- Systematic risk, errors generated in the design process through a missed requirement cascade or an incomplete analysis; and
- Random hardware faults specific to the malfunction of the device in question.

For roughly the last decade, automotive OEMs have been relying on part 5 of this standard to help them address hardware malfunction at the component level and to establish what the industry considers "safe" design practices. The result of this analysis has led the industry to focus mostly on the core of each electronic module, the microcontroller, in addition to adopting the failure mode effects and diagnostic analysis report, dependent failure analysis, and their peer reviews.

And this is how engine, gateway, and body controllers coalesced around what is considered mostly common



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By Christopher Semanson

for functionally safe electronic control units (ECUs). They employ things like dual core lockstep processors, double stored variables, and other safety mechanisms that enhance their coverage metrics to achieve the all-important Automotive Safety Integration Level (ASIL) rating. Building upon part 5 of the standard, and the level of complexity to which automotive systems have ascended, ISO 26262 has expanded its coverage to include part 11, which focuses on semiconductor components, with the goal of simplifying the automotive system by both:

- Combining multiple functions into one large system on chip, thereby creating large SoC devices with multiple power domains, and
- Wanting to simplify wiring such that only one low voltage bus runs throughout the vehicle.

An example of this integration is shown in Figure 1.

This leads automotive system designers to adopt multi-rail, high power, power management devices (PMICs) that have traditionally been reserved for

high-end server systems and other highly integrated consumer devices. These devices are capable of splitting one voltage rail into multiple lower voltage rails via integrated switching and linear regulators, in addition to being able to monitor each output. But semiconductor manufacturers who've normally prioritized speed in development to get into a next-generation server socket and are now tasked with applying part 11 to their products, with customers left to determine how to implement them.

To help automotive designers understand what to look for when shopping for PMICs and other power devices, we'll use an analysis containing a hypothetical situation that starts with a simple quality managed (QM) switching architecture for a basic DC/DC converter, then apply the tools ISO 26262 gives us to analyze the possible failures and, finally, present an architecture that attempts to address dependent and random hardware failures. It's important to note that many solutions to the "what makes this device safe?" question exist, so the analysis and mechanisms discussed here are common.

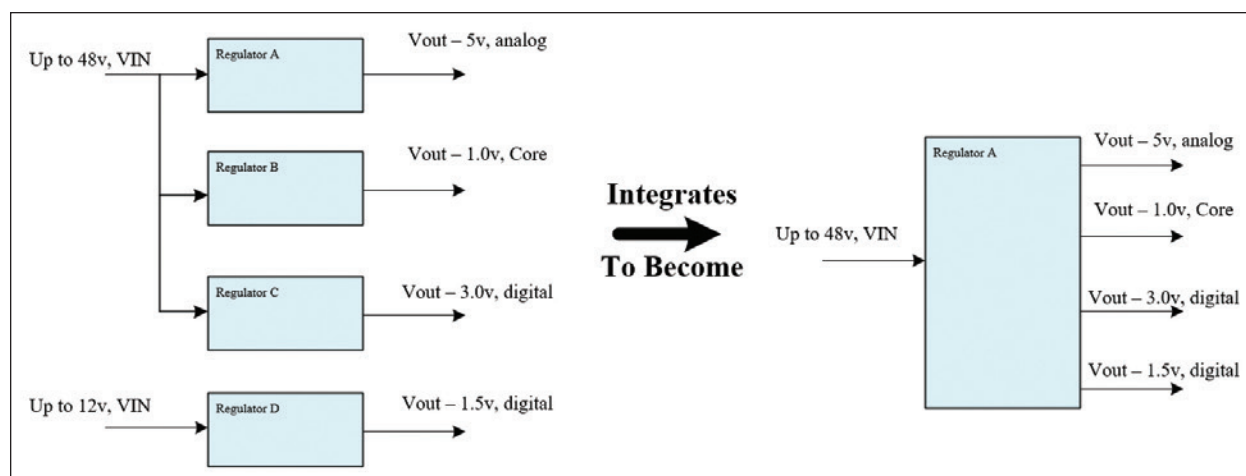


Figure 1: Integrating individual regulators into a PMIC

This article isn't meant to be conclusive, and a lot depends on what extra functions are required of the device by the system integrator. But this article will allow you, the automotive module designer or safety manager, to recognize what to look for when shopping for your next power device for your module.

ISO 26262 ANALYSIS TOOLS

In reading through ISO 26262, the standard suggests three widely accepted analysis tools that help the safety manager lead the design team to an understanding of how to create a functionally safe product. These tools are:

- The block diagram;
- The dependent failure analysis (DFA); and
- The failure mode effects and diagnostic analysis (FMEDA).

These tools are suggested for their ability to reduce complexity and allow the team performing the analysis to confidently arrive at a functionally safe design. In this article, we'll review each technique, give examples of how they're used, and then apply them in the safety analysis.

The Block Diagram

Reading through ISO 26262's specification, it's very clear that the authors valued one thing: *avoid needless complexity in the design process*. And, if you notice, you'll see that the standard identifies a standard design practice of creating a block diagram to help:

- Abstract the design to ensure that each block has a dedicated function, eliminating the need for needless (and often confusing) mixing of functions, and forcing the designer to plan their design prior to implementing it; and
- Allow the conceptual safety analysis to easily understand information flow and determine where mechanisms need to be implemented, and the design

decisions that need to be made in order to create a design free from dependency.

A simple example of such a diagram is shown in Figure 4.

When establishing a hierarchy, it's important to remember. *Abstraction!* Without it, the diagram loses context and becomes a burden to maintain and develop. A recommended rule of thumb is to create a hierarchy not more than three to four sublevels deep, with the goal being to be able to have enough detail such that the box being described becomes self-describing.

Failure Analysis

Before we start performing the analysis that will lead to a summary of commonly implemented safety

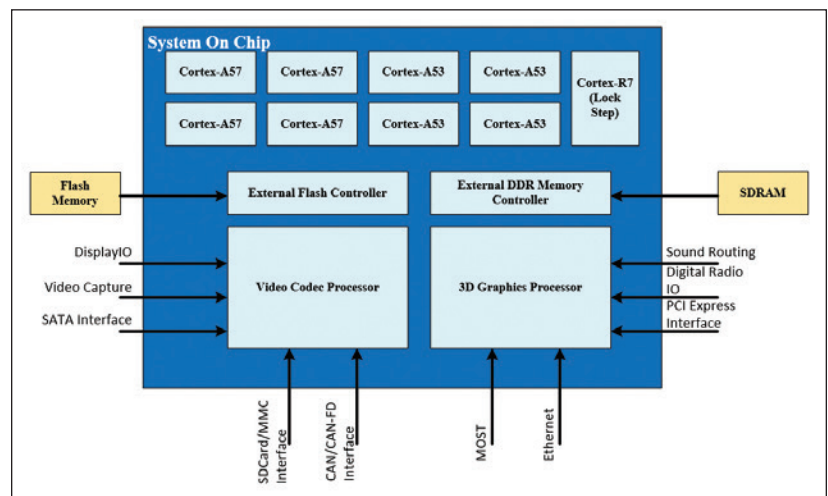


Figure 2: Integrating discrete HW components into a SoC

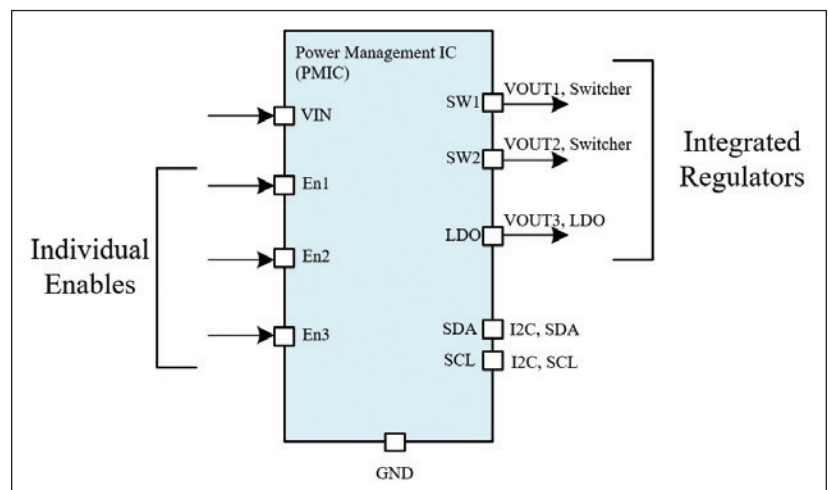


Figure 3: Basic PMIC with 3 outputs

mechanisms, we first need to review the tools that the specification expects us to employ in the analysis. These tools help the design team identify dependencies between safety mechanisms and the sections each safety mechanism protects, and how to apply commonly accepted failure modes in order to come up with a robust design.

- *The dependent failure analysis:* This analysis tool is designed to help identify dependent failures between safety mechanisms and the components they're meant to protect.
- *The failure mode effects and diagnostic analysis:* This analysis tool takes into account commonly accepted

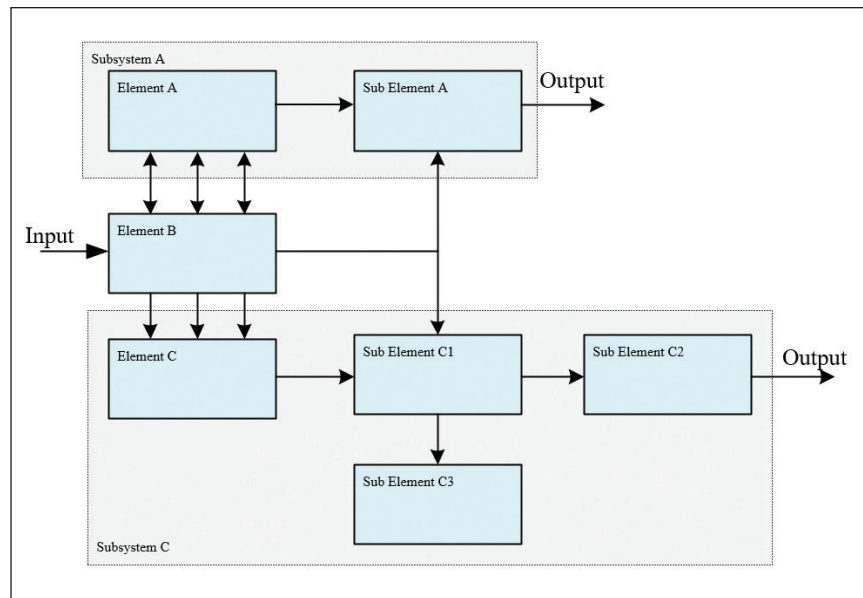


Figure 4: Example system diagram



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failure modes such as broken resistor strings and component drift and determines the impact on function of the device. It is also used as a calculator, justifying your safety coverage for an ASIL rating.

These dependencies and failure modes are analyzed within the context of the stated safety goal of the device. The safety goal is the primary high-level safety-related function that the device is designed to support. In most power management devices, this goal relates to output power monitoring; in other more complex devices, you may see this expanded to include other functions.

In this article, our example safety goal is to monitor the output for any voltage irregularities and provide a means to notify the system when we're unable to provide this support properly such that they can suspend any safety-related decisions that might be impacted by an output failure.

For the safety manager evaluating devices for potential use in their module, they're mostly concerned with voltage drift, spikes, and oscillations of the output rail, while maintaining the ability to warn the system if any of these occur.

Dependent Failure Analysis

The DFA is an analysis tool that examines the relationship between a safety mechanism and the circuit it is assigned to protect. The analysis starts out by identifying failures that are commonly known to impact more than one system. These include:

- *VCC and ground circuits:* Where drifts, noise, or failures of circuits powering the safety mechanism and the device it powers could adversely impact both.

- *Temperature:* Where an increase or decrease in temperature could impact a mechanism's monitoring accuracy while at the same time decreasing its ability to control something.
- *Shared components:* Where the failure of components like memory buses and other shared devices could impact both a monitor and regulator function.

The DFA helps a design to become free from interference by obtaining dependence, as shown in Figure 5, by addressing cascading faults and common cause faults (CCF).

Companies that have implemented a culture of safety in their design process have defined initiators that are meant to help guide the design and safety teams in their analysis.

Failure Mode Effects and (Diagnostic) Analysis

While the DFA is used to determine independence to help create a design that is free from CCF and cascading failures, the FMEDA is implemented as a straightforward approach meant to analyze the failures of each component in the design. The goal of the FMEDA is to systematically go through the hierarchy of the design and apply ISO 26262-recognized failure modes to each component to determine the output. Failures covered here were initially introduced in part 5 of ISO 26262 and then expanded in Part 11 in the Second Edition. They include, but are not limited to:

- Resistor failures and component drift
- Soft error rate in memory, and stuck at faults in digital logic circuits
- Data transmission failures, including loss of message, corrupted messages, and unintended message

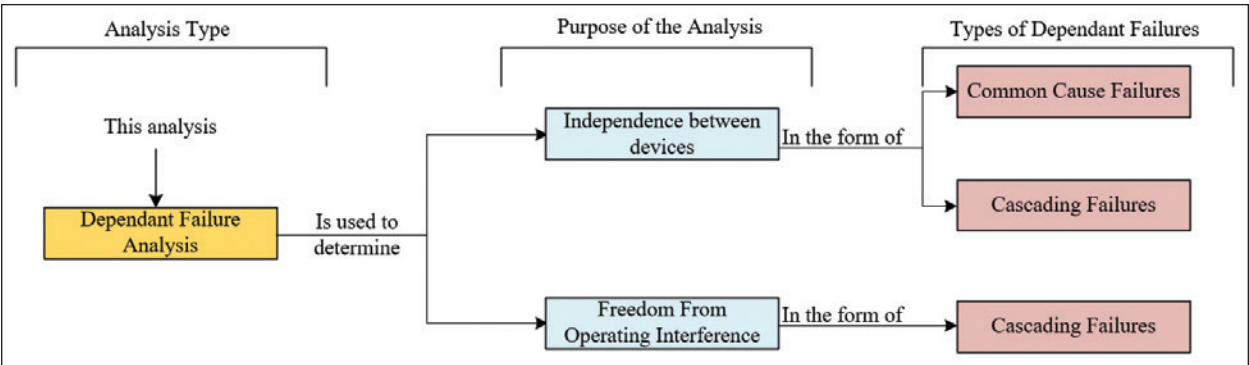


Figure 5: Types of dependent failures

In the conceptual phase, these faults are applied to the design, mechanisms are created to address the failure modes, and then a quantitative analysis is conducted to determine exactly how well the mechanism addresses the failure mode. The DFA is conducted to ensure that the device addresses dependencies.

The FMEDA considers faults into multiple classes, two of which include:

- **Single point failure mode (SPFM)**, where the failure of the circuit or device directly impacts the ability for the device to perform a task related to the stated safety goals. An example would be a feedback control loop opening leading to oscillatory behavior.
- **Latent fault (LF)** failure mode, where the failure of the circuit or device indirectly impacts the ability for the device to perform a task related to the stated safety goal. An example would be a monitor that only outputs “no fault” due to a short circuit failure; it requires a fault to be impactful to the system.

Latent faults are more nuanced, as their failures require the presence of more than one fault to exist at the same time to impact the design, versus a single point fault which will directly impact the device. A more complete fault classification is contained in Table 1/Figure 6.

The challenges of a FMEDA stem from the fact that it’s meant to be an exhaustive analysis. In devices that implement a large number of discrete components (e.g., millions of transistors) it can be a daunting task, which is why it’s often paired with a DFA for an exhaustive analysis. The effectiveness of the DFA and FMEDA all depend on how well the design is understood at the time of analysis, which is even more reason for a disciplined design group to have a well thought out design.

Next, we’ll use these three tools in analyzing, and creating a functionally safe power management device.

INTRODUCING THE BASIC DC/DC CONVERTER ARCHITECTURE

To design and analyze our conceptual DC/DC converter, we first create a block diagram to set an architecture and establish a hierarchy. By understanding how information flows between major blocks, it will help to dissect the design. A typical power management devices’ circuit architecture includes:

- **Voltage reference generation:** This normally includes the bandgap, and a digital to analog converter that provides references to switching converter, monitors, and any other devices that need a bias current or voltage.
- **Internal rail generation:** The internal power domain that provides power to the internal components of the device and sets the voltage input/output (VIO) level.

Type of Fault	Description
SAFE FAULT	Not in safety relevant parts of the logic, or in safety relevant logic but unable to impact the design function
SINGLE POINT FAULT	Dangerous, failure can result in the violation of the safety goal of the device; no safety mechanism to detect this fault.
RESIDUAL FAULT	Dangerous, can violate the safety goal of the system. They are single point faults partially detected by a safety mechanism.
MULTIPOINT FAULT (LATENT)	Faults that do not directly violate the safety goal, but only do so if another fault occurs; for example, in a safety mechanism.
PERCEIVED MULTIPOINT FAULT (LATENT)	Multipoint faults detected by a safety mechanism.

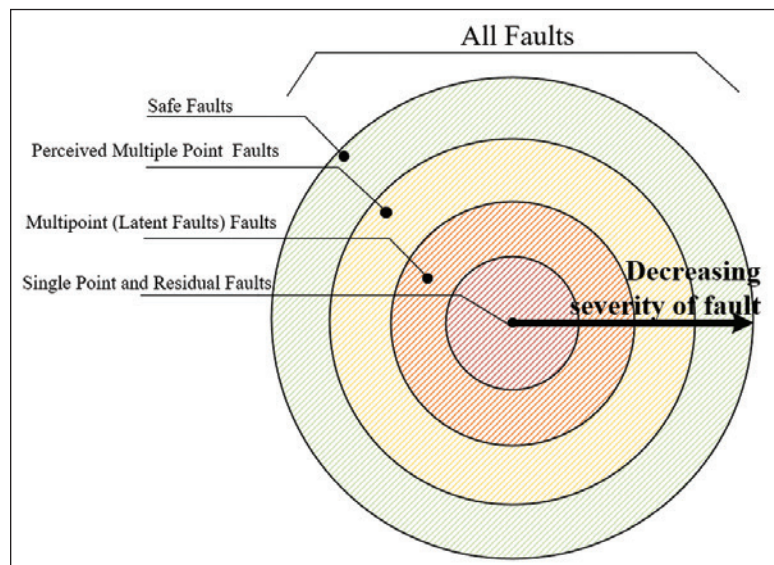


Table 1/Figure 6: Types of faults

- *The switches:* These devices span the range of implementation, but in general, this includes the pre-driver and driver circuitry that provide the switching from the input voltage.
- *The PWM control circuitry:* This comprises the entirety of the control loop, which is generally made up of an error amplifier, compensation, and the feedback (either internal or external)
- *Regulator enabling:* In general, these are things that enable or disable regulation such as a power on reset device, over current, over voltage, or over temperature setting, and an external enable.
- *Digital core:* The glue that ties the above together, allowing the flexibility to the marketing manager to option the part out such that it can be programmed to fit multiple different applications.

Together, these systems work to form the basics of a power management device, which is shown in Figure 7.

The full design and implementation of each of these circuits depends upon a wide variety of factors specific to the application. In the following sections, we'll discuss some high-level circuits that make up these blocks, which will allow us to facilitate the completion of our conceptual analysis.

THE SAFETY ANALYSIS

Combining the dependent and failure mode analysis, we can conceptually analyze our architecture and come up with mechanisms and additional architecture enhancements to improve our robustness to hardware failures. While this analysis is not considered to be exhaustive, it will provide some context for a safety manager or product designer evaluating datasheets to compare capabilities.

INTERNAL RAIL AND BIAS GENERATION

In our hierarchy, we start by creating a powertrain used to help generate bias voltages, currents, and an internal rail to power all of our onboard devices. Part of this powertrain will be a voltage DAC that will provide tap voltages for various references around the device.

We define the fault models from the DFA, and come up with the following.

- *Common cause faults:* Where a singular fault leads to two faults in two separate elements (Figure 8).
- *Cascading faults:* Where a fault in one element, leads to the fault in another element (Figure 9).

Taking these two fault models into context against Figure 7 (the basic regulation architecture), we see

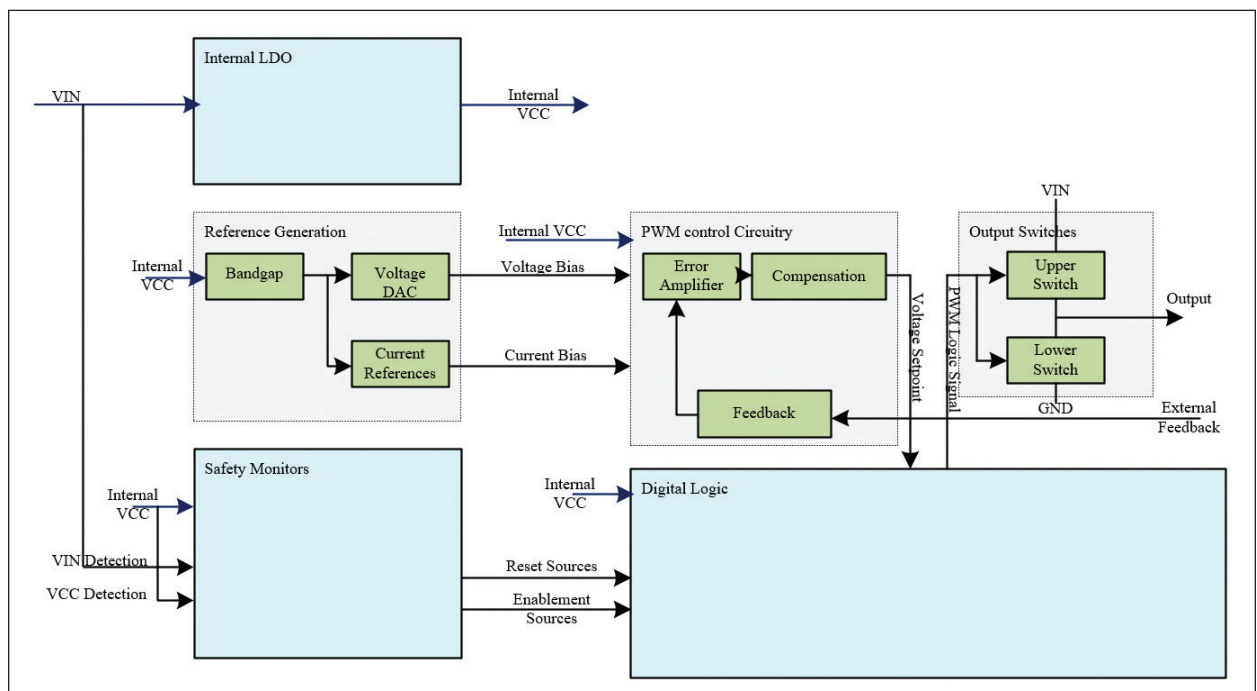


Figure 7: Basic regulation architecture

that there is only one source of bias and VCC for the entire chip, if that source were to experience a failure mode of either:

- Drift, due to either component failure or temperature; or
- Oscillation, due to loss of feedback in the voltage generation circuit.

Then that common cause fault would impact both the voltage monitor accuracy as well as regulation targets. To address this, the original architecture is modified to be more independent.

Figure 10 illustrates just one way to address this dependency, in which there are separate bias circuits (bandgaps) and voltage DACs to create separate bias points. This reduces the dependency between circuits

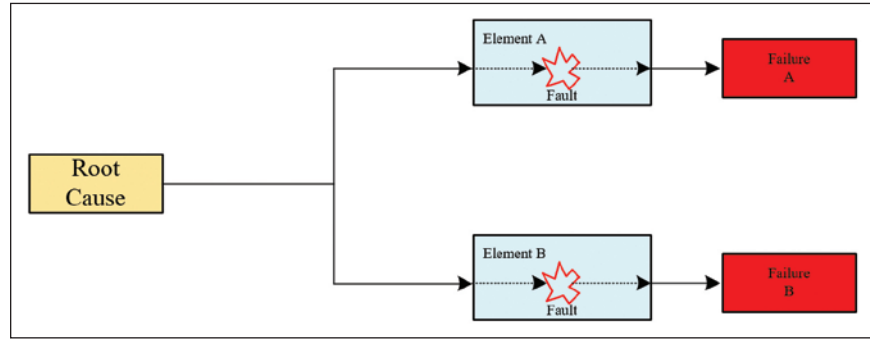


Figure 8: Common cause failure model

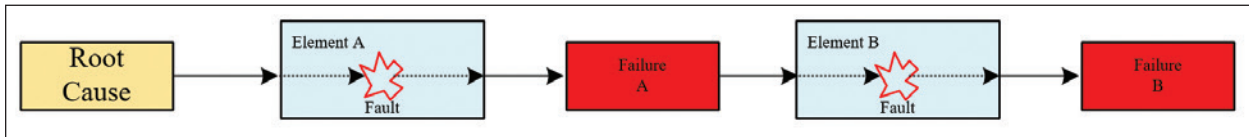


Figure 9: Cascading failure model

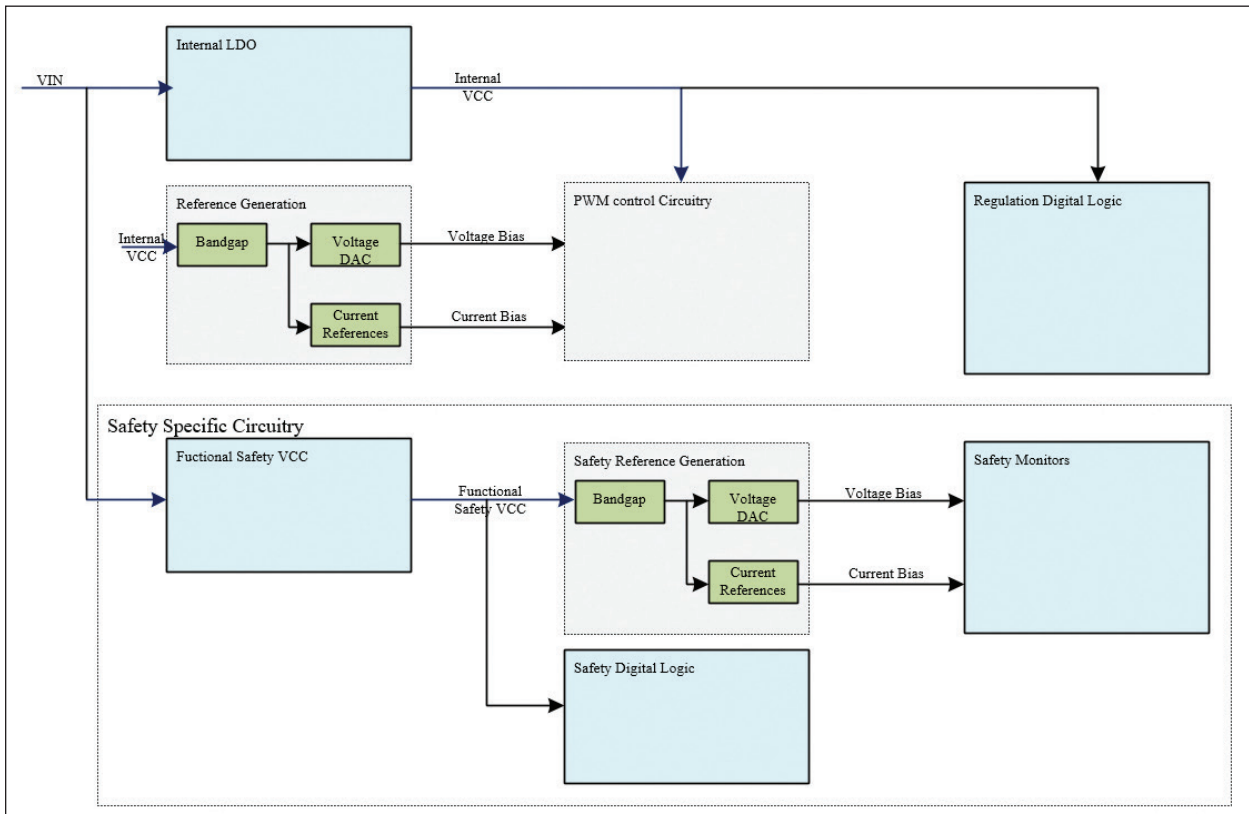


Figure 10: An improved biasing structure, with separate power delivery

and is often why datasheets feature a separate “safety” bandgap or a different voltage domain for their safety devices. Other examples include:

- Distinctly designed bandgaps to prevent both from experiencing the same failure.
- In addition to architectural changes, it is not uncommon to monitor each bandgap against one another, as well as to monitor the source of VCC against a reference over which it has no influence.

The more rigid the safety requirements, the more complex the solution becomes. Now that we’ve addressed dependencies and discussed the implementation of safety mechanisms in the internal bias and power generation section, we turn our attention to the voltage control loop and output switches.

PWM CONTROL CIRCUIT & OUTPUT SWITCHES AND DRIVERS

Arguably the most important part of a power management device, the feedback loop design is critical since the choice in architecture denotes what type of safety mechanisms are necessary as well as performance. There are a wide variety of control architectures, but in this conceptual design, we’ll be employing:

- A voltage control outer loop that utilizes an error amplifier, compensation, reference, and feedback to control the output to a setpoint. In our conceptual architecture, we’ll be utilizing external feedback.
- An inner current loop controller that acts as a quick modifier to the setpoint to compensate for load changes. In our conceptual architecture, we’ll be sensing current through the (integrated) output switches in terms of high and low side current sensing.

The basic architecture is found in Figure 11.

While the fully exhaustive analysis would take quite some time, some pronounced examples include the compensation circuit, output switches, and references. The failure modes analyzed are shown below:

- *Failure of the output switches by being stuck high or low:* This would lead to an irregularity in switching and would cause either an output overvoltage, under voltage, over current, and/or over temperature event due to shoot through or directly connecting the output to either ground or VIN.

- *Compensation, which damps the response of the control loop to prevent excessive deviations from the setpoint during a load change, and oscillatory behavior:* A potential failure here would be an overvoltage event or oscillatory behavior if the bandwidth of the controller drastically changes.

First, taking these three failure modes into consideration, we can easily develop two different failure mode protection mechanisms:

- A window comparator which measures for over and under voltage on the output; or
- An over current monitor which senses the current through either the high side or low side switch.

For this reason, the hallmarks of most power management devices are output current and voltage monitoring, and are often done via comparators instead of an onboard analog to digital (A/D) converter. And, taking lessons from our previous section, these output monitors will be referenced with a uniquely powered and referenced bandgap.

Next, we continue with the DFA and automatically clue into the feedback node, which is shared between the regulation and output monitor. If we lose the resistor due to a failure in the resistor divider or if the pin shorts, the device’s regulation will malfunction as the target becomes incorrect, and the monitor runs the risk of not catching it. A DFA leads to the following two criteria:

- The device needs to implement two independent sources of feedback to address the dependent failure of the feedback node shorting to another pin or another voltage on the board; and
- This independent source of feedback needs a redundant resistor divider to address the failure mode of any part of the resistor feedback network shorting.

Again, for this reason, it is not uncommon to see a feedback pin and another pin that is used for monitoring. If the feedback resistor is instead internal, then that is redundant and often through a different path. With these additions, we can expand our definition to include an example of what a safety manager or module engineer might see when shopping power parts.

For the last two sections, the design turns its focus to things that are often under the category as monitors instead of the control loop.

MONITORS AND CONTROLS

The monitors and enabling controls are arguably some of the most important circuits in the device. They are comprised of a series of comparators and measurement circuits that make up:

- Over current monitors.
- Power on reset detectors.
- Output voltage (over and under voltage) monitoring.
- Internal clock monitoring

Each of these monitors often have the ability to reset/alert downstream components when an irregularity has occurred. Applying our DFA theory again, we notice that the same situation continues to come up, that is, dependencies in the feedback loop and in how we reference the thresholds for the monitors.

Next, conducting the FMEDA, we apply ISO 26262-recognized failure modes only to the comparator. The faults models here are comparator output stuck at faults (stuck high and low). Of these two faults, stuck low is the more impactful of the two when it comes to monitoring, as the fault occurrence would be missed. In order to increase the device's ability to detect these stuck low faults, which would cause the device to miss a fault in the event of one occurring, you will often see a term ABIST, an acronym for analog built-in self-test.

The process outlined in Figure 13 allows a brief moment in time for the digital part of the device to take control of the comparator input and force the input above

or below the trigger voltage in order to see if the comparator circuit works.

After successful determination, the input control is given back, and it becomes a nominal sensing circuit again. This process takes a moment during startup and is why many datasheets mention some sort of ABIST

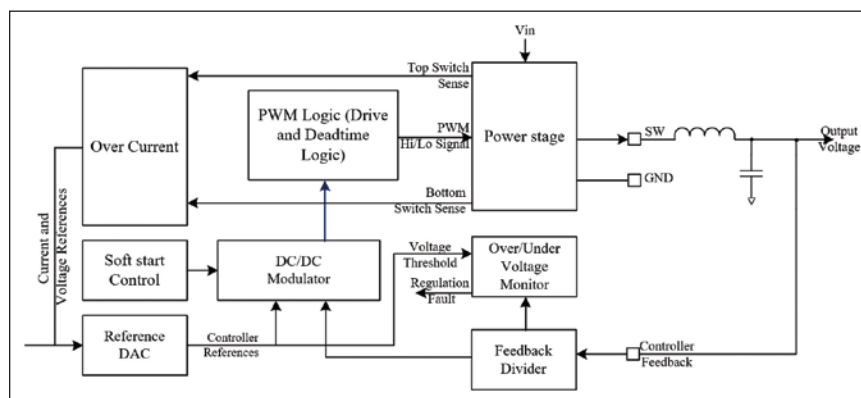


Figure 11: Basic DC/DC modulator, with dependencies in the monitor

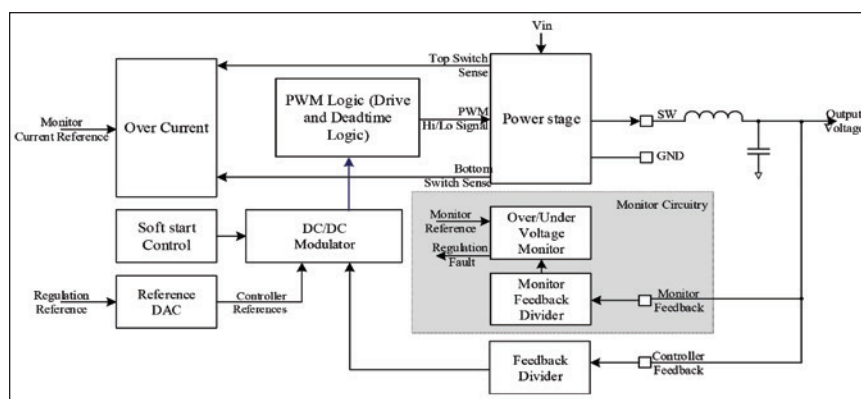


Figure 12: Basic DC/DC modulator, without dependencies in the monitor

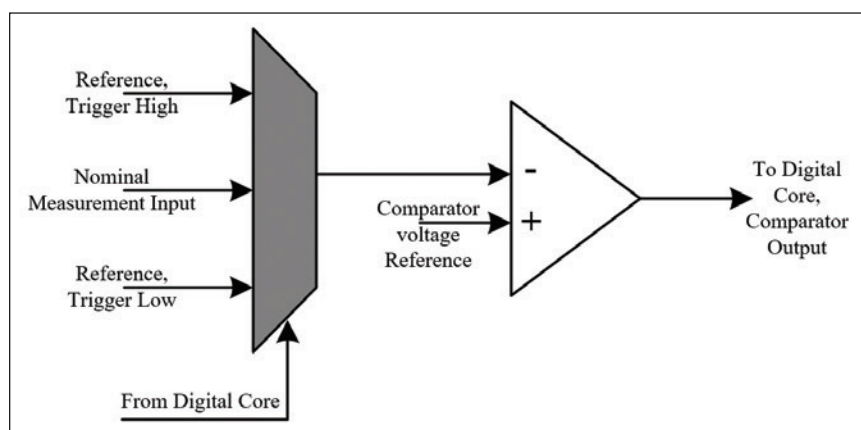


Figure 13: Comparator BIST architecture example

in their feature section as it is a low impact way of checking for stuck faults.

Lastly, we'll examine the brains, the digital core of a mixed-signal regulator.

DIGITAL CORE

The digital core is most likely the closest thing power management devices have to flash memory in terms of implementing configurability. Power management devices often contain the following elements as part of the digital core:

- A wide variety of configurations held in fuses and registers;
- A main high-speed oscillator; and
- A serial communications interface- usually I2C or SPI.

The digital core sits next to the analog parts, as shown in Figure 14, and is often broken up between a section of digital logic that makes functionally safe decisions and a section responsible for startup and control of the regulator.

This architecture is often preferred to mitigate the possibility of dependencies found through a DFA analysis. In order to better understand the breakup of the digital core, see Figure 14, where the main functions consist of:

- Configuration, often in the terms of runtime configuration registers and one time programmable (OTP) fuses;
- Functional safety decision making, often realized as a state machine; and
- Communication, either implemented as a I2C or SPI controller.

Here, the fault modes defined by ISO 26262 are more aligned to what you would see in a microcontroller setting. We first realize this by applying our FMEDA criteria in terms of bit corruption at the one-time

programmable (OTP) fuse array and configuration registers. A failure here could misconfigure the chip, either at startup and during runtime. In order to protect against this issue, an n-bit cyclic redundancy calculation (CRC) is often executed both at startup and periodically on the configuration of the device to ensure integrity. This is also extended to the communication interface, where a CRC is performed on each communication transaction.

While the list of digital safety mechanisms and design options is vast, it is normal to see the following among the top listed as safety mechanisms in addition to the CRC:

- Redundant logic where necessary;
- Clock monitoring; and
- Logic BISTing (LBIST) which, like the ABIST, checks the digital logic for critical stuck faults.

After addressing each main function of our basic DC/DC buck converter and the random hardware failures associated with these sections, our focus turns on how to evaluate metrics and grade the effectiveness.

ASIL FAULT METRICS

The analysis done was qualitative. The process starts with a diagram of interconnections for our

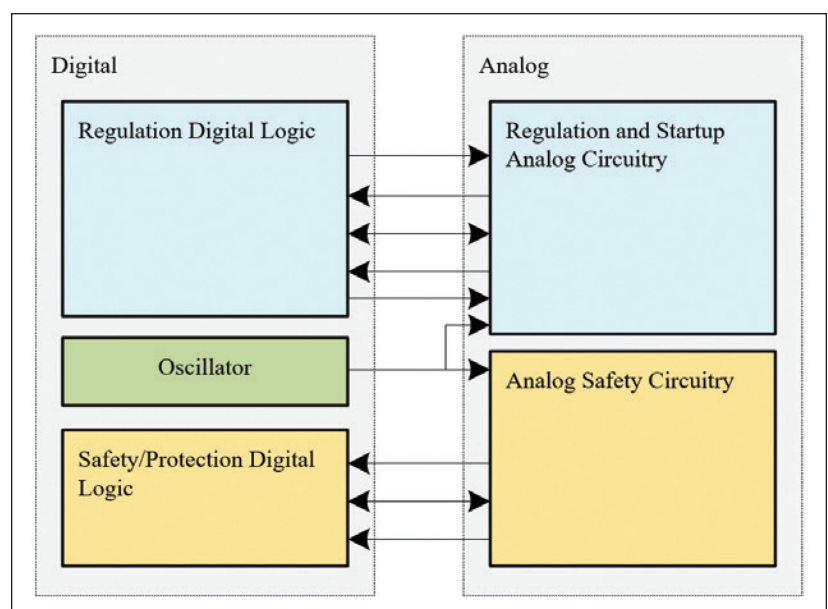


Figure 14: Analog and digital partitioning

power converter and continues by applying industry standard failure modes to each block and reviewing their effects. It continues with the DFA that allows the design team to address dependencies in the architecture, and also allow the device to showcase various safety mechanisms and architectural enhancements that allow for a certain ASIL.

We define the coverage metric as a means for standardizing analysis in a quantitative way across the industry from part to part and manufacturer to manufacturer. This means that if the target for our power converter is an ASIL B system, that would require a specific level of coverage, as opposed to an ASIL D system which requires a higher single point, and latent fault detection coverage. The summary is shown below in Table 2.


And often, you will see comments in the datasheet like “supports applications up to,” which often means that during the analysis, certain assumptions were made that, if followed, would allow for the system to make up for the lack of detection.

Before you begin reviewing your supplier datasheets or before you begin designing, I recommend that you review ISO 26262 as the specification provides

an overview of common ways of dealing with faults and provides strategies for low, medium, and high coverage which the industry recognizes. An example is shown in Table 3, but as always, refer to your copy of ISO 26262 for a comprehensive list.

CONCLUSION

Functional safety is an evolving area of automotive and industrial design, and the right device can be difficult to find since each semiconductor manufacturer presents their product in the best possible way. With each new design comes a new set of safety mechanisms implemented by the design and safety teams, which the marketing team then uses as saleable features. But, without some basic background, this can lead to confusion.

The conceptual analysis presented in this article is meant to give you, the reader, some tools to understanding why ASIL-rated power management devices have the “safety” features listed in their hardware datasheet. And, in preparing for your next ADAS design, remember that ISO 26262 outlines the tools needed to address both random hardware and systematic design faults, not just high-level digital components but of standard mixed-signal analog/digital designs as well! 

Metric	ASIL B	ASIL C	ASIL D
Single Point Fault Metric	≥ 90%	≥ 97%	≥ 99%
Latent Fault Metric	≥ 60%	≥ 80%	≥ 90%
Probabilistic Metric for Random Hardware Faults (in FIT)	100 FIT	100 FIT	10 FIT

Table 2: ASIL metrics

Safety Mechanism	What the safety mechanism protects	Typical Diagnostic Coverage Considered Achievable	Note
Ram Pattern Test	Volatile Memory	Medium	High Coverage for stuck
Voltage Monitoring	Power Supply	High	Depends upon the quality of monitor
Majority Voter	General System Measure	High	Depends upon the quality of voting
Comparators	General System Measure	High	Depends upon the quality of comparison

Table 3: Safety mechanism and coverage

LOCATION OF SAFETY WARNINGS

On the Product or in the Manual?



An important issue to be considered in trying to meet the duty to warn and instruct is for the manufacturer to decide where to place safety warnings – on the product, in the manual, or on the product and in the manual. Generally speaking, all warning labels on the product should be shown in the manual. But the converse is not true. Not all warnings in the manual need to be placed on the product.

Since our first goal is to communicate the warning to the user, we need to figure out where best to place them to maximize the possibility of that happening. In the event of an accident, the plaintiff will always claim that they did not see the warning and, therefore, the manufacturer may need to present evidence as to why they placed it where they did.

This article will discuss the basic duty to warn and instruct, and then examine the law and standards as they pertain to this issue. Then it will discuss recommendations about how to decide where to place this information and what to say.

BASIC LEGAL DUTY TO WARN AND INSTRUCT

Product sellers must provide “reasonable warnings and instructions” about their product’s risks. The law differentiates between warnings and instructions as follows: “Warnings alert users and consumers to the existence and nature of product risks so that they can prevent harm either by appropriate conduct during use or consumption or by choosing not to use or consume.” Instructions “inform persons how to use and consume products safely.”¹

Therefore, when the law talks about the “duty to warn,” it includes warning labels on products, safety information in instruction manuals, and safety information in other communications such as company websites, social media, advertising, and catalogs.

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By Kenneth Ross

The law says that a manufacturer has a duty to warn where: 1) the product is dangerous; 2) the danger is or should be known by the manufacturer; 3) the danger is present when the product is used in the usual and expected manner, and 4) the danger is not obvious or well known to the user.²

Once the decision has been made to warn, the manufacturer needs to determine whether the content of the warning is adequate. Generally, the adequacy of a warning in a particular situation is a question of fact to be decided by the jury. However, various courts and commentators have described a list of requirements and goals of an adequate warning. One court said:

*"If warning of the danger is given and this warning is of a character reasonably calculated to bring home to the reasonably prudent person the nature and extent of the danger, it is sufficient to shift the risk of harm from the manufacturer to the user. To be of such character the warning must embody two characteristics: first, it must be in such form that it could reasonably be expected to catch the attention of the reasonably prudent man in the circumstances of its use; secondly, the content of the warning must be of such a nature as to be comprehensible to the average user and to convey a fair indication of the nature and extent of the danger to the mind of a reasonably prudent person."*³

Other courts have said that an adequate warning does the following:

- Alert the consumer or user to the severity of the hazard (severity being defined as the magnitude of the hazard and the likelihood of it being encountered);
- Clearly state the nature of the hazard;
- Clearly state the consequences of the hazard; and
- Provide instructions on how to avoid the hazard.

And the *Restatement Third, Torts: Products Liability* says that a court must focus on a warning's "content and comprehensibility, intensity of expression, and the characteristics of expected user groups" to determine its adequacy.

Case law treats the duty to warn and instruct separately. So, including adequate warnings in the manual may not be enough to meet the duty to instruct. And adequate instructions in the manual may not fulfill the duty to warn. There are very few cases that discuss the adequacy of instruction manuals as instructions and not warnings. And the case law is not particularly illuminating. The cases only say that manuals should be "adequate, accurate, and effective," and "clear, complete, and adequately communicated."

WARNINGS STANDARDS

On the issue of location, which is certainly related to adequacy, let us first look at what the standards in the U.S. and elsewhere say. Except for some product specific standards, general warning label standards do not talk about when the warning should also be placed in the manual and, more important, when you can just place warnings in the manual and not on the product.

Product specific standards promulgated by ANSI, ASTM, UL, CSA, etc., generally talk about what warnings have to be attached to the product and what information, including warnings, have to go in the manual. But not all product specific standards deal with the content of instructions and some do not deal with warnings or instructions at all. And, of course, compliance with these standards is not a defense. Therefore, manufacturers cannot completely rely on them to answer this question.

INSTRUCTION STANDARDS AND GUIDELINES

There is one general standard that talks about instructions. ANSI Z535.6 is a standard published in

late 2006 dealing with instructions. The purpose of the standard is, in part, to “establish a uniform and consistent visual layout for safety information in collateral materials for a wide variety of products and establish a national uniform system for the recognition of potential personal injury hazards for those persons using products.”

The standard applies to all “collateral material” that accompanies a product but does not deal with safety information communicated through company websites, social media, advertising, and promotional material, or stated in audio/visual material such as safety videos.

This standard says nothing about when a warning is sufficient when placed only in the manual and when it must also be attached to the product. In addition, this standard only deals with safety instructions in a hardcopy format.

There are some product specific standards that have detailed requirements about the safety information that need to go in the manual and on a label placed on the product. Such standards do answer the question on where this information goes. Unfortunately, as stated above, compliance with such standards is not a defense in a product liability case. Therefore, an injured party can still argue that the warning should have been placed on a label on the product and not just in the manual.

On this question, Steve Hall of Applied Safety and Ergonomics and current chair of the ANSI Z535 committee said to me in an email dated August 2, 2012:

“There is no hard and fast rule, but generally you want to try to provide messages in a way that gives people a reasonable chance to read them at an appropriate time. So, for tasks that are expected to involve referring to the manual (e.g., assembly, troubleshooting, maintenance, etc.), it is generally reasonable to provide safety messages in the relevant part of the manual, and not on a label. Conversely, for scenarios where the target audience is not reasonably expected to have access to a manual, a label may be more appropriate.”

In addition, there are a few governmental guidelines or guidances on instructions, but these generally provide no rules on where to place safety information. One of these is the U.S. Consumer Product Safety Commission’s *Manufacturer’s Guide to Developing*

Consumer Product Instructions.⁴ In the European Union, there are product specific directives that discuss labels and instructions. For example, the Guide to the European Union’s Machinery Directive (2006/42/EC) says:

“The manufacturer is not expected to mark on the machinery all the information for safe use provided in the instructions. However information concerning essential aspects of safe use must be marked on the machinery, such as, for example, the maximum dimensions of workpieces, the maximum dimensions of the tools to be used, the maximum slope on which the machinery is stable, the maximum wind speed and so on. The information to be marked on the machinery is usually specified in the relevant harmonized standards”⁵

In addition, the International Organization for Standardization (ISO) has issued several standards on instructions.

COMMON LAW ON WARNING LOCATION

On the issue of the location of the warning on the product, case law requires the warning be in a position so that it can be seen before the user encounters the hazard. This is also required in ANSI Z535.4. There are also a few cases where a warning was deemed inadequate because it was in the wrong location on the product, and a few cases where the warning was only in the manual and not on the product.

On the issue of how to analyze whether to place a warning only in the manual, Professor David Owen, in his products liability hornbook, says:

“Whether adequacy requires in any given case that warnings be placed directly on the product involves a balance of the significance of the hazard, the user’s need for the information, the availability of a feasible means to place the warnings on the product, and other factors in the calculus of risk.”

If feasible, reason normally suggests that important warnings of serious hazards be placed on the product itself rather than in a pamphlet, booklet, or information sheet that can be damaged, lost, discarded, destroyed or stuffed in a drawer. Depending on the circumstances, however, a warning may still be adequate even if it is provided off the product in a manual or other writing.”⁶

Professor Owen cited just a few cases for the above proposition. One of the cases, *Broussard v. Continental Oil Co.*⁷ illustrates one basis for putting warnings in the manual and not on the product – a lack of space on the product.

Black & Decker sold a hand drill with one warning on the product, “CAUTION: For Safe Operation See Owner’s Manual.” In the manual, there was a section devoted to safety. And item #18 in that section dealt with a safety precaution that was not followed and resulted in injury to the plaintiff.

The court dealt specifically with the question of whether Black & Decker met its duty to warn by placing the warning in the manual and not on the product. Plaintiff’s counsel submitted a proposed warning label for the hand drill that included 10 of the 18 warning messages in the manual. The court felt that the proposed language concerning the hazard involved in this accident was inadequate. In addition, the proposed warning showed how difficult it is to adequately warn of multiple hazards in a small space.

The court felt that putting even 10 warning messages on the drill decreased the effectiveness of all the warnings and that, given the clutter, a consumer might not read any of them. Thus, the court held that Black & Decker met its duty to warn by including a warning referring to the manual on the product and including the specific warning which was deemed adequate in content in the manual.

Another case from Louisiana held that a warning in the manual was sufficient because a warning on the product would not have been readable given the corrosion and wear to which the product and label would be subjected.⁸

In another case cited by Professor Owen involving a snowmobile, the court said of the instruction manual:

“However, among a list of fifty warnings, the manual contained warnings against standing behind the snowmobile while the engine was running and against lifting the rear of the snowmobile while the engine was running. The machine itself contained a printed sticker, near the front windshield, warning users to read the owner’s manual before using the machine and offering other advice. But the sticker did not warn against

standing behind the machine or lifting it while the engine was running.”

The plaintiff argued that there should have been a warning on the back of the snowmobile and not just in the manual. The court agreed and said:

“Given that the snowmobile had a handle attached to the back to facilitate lifting; the danger posed by lifting up a running snowmobile; Yamaha’s admitted knowledge that “tracks could fail when the rear [of the snowmobile] was lifted and the track was accelerated”; the foreseeability of users engaging in that maneuver; and the expert testimony about the frequency with which consumers fail to read owner’s manuals, it is not surprising that the jury found that Yamaha provided an inadequate warning.”

WHAT TO DO

This issue illustrates the importance of creating or revising instruction manuals and warning labels at the same time. They are inextricably intertwined. They form all or part of a safety communications system and will be viewed as such by the plaintiff and a jury.

With this in mind, I suggest that the manual be developed first, followed by the warning labels. Here are a few suggestions to consider for incorporating safety information into the manual. Some but not all of these suggestions are in ANSI Z535.6.

- The cover of the manual should have a boxed warning saying something like “Read this manual and all warning labels on the product before using this product. Failure to follow these instructions and safety precautions can result in serious injury or death.” It should also say, “Keep this manual nearby in a safe location for future reference.”
- A Safety Section should be placed at the beginning of the manual, before or after the table of contents, that describes the risks involved in the use of the product and how to minimize or avoid them. This section should include definitions of the signal words—such as “danger,” “warning,” and “caution”—that are used on labels and in the manual, as well as reproductions of the labels showing where they are attached to the product. If the product has symbol-only labels, the manual should describe the meaning of all symbols.

- Depending on the length of the Safety Section, it could be separated into subsections to make the precautions easier to read and find. The subsections can be devoted to the type of activity (e.g., assembly, installation, operation, maintenance) or type of hazard (e.g., fire, electrocution, crush) or even type of avoidance procedure (e.g., avoid open flames, wear protective gear, stay away from power lines, keep hands out of moving parts, etc.).
- Not all safety messages in the Safety Section need to be repeated in the text, especially if they are general and apply to many activities. In addition, not all safety messages in the instructional sections need to be repeated in the Safety Section. For example, lower level messages, such as those using “Caution” and “Notice” as signal words, may not need to be in the Safety Section.
- General safety messages should be included at the beginning of a chapter (e.g., maintenance, installation, or operation) or within a chapter. They should include general references to the Safety Section and other safety messages such as “Do not operate equipment without first reading this chapter and the Safety Section at the beginning of this manual” and “Failure to follow safety precautions in this chapter could result in serious injury or death.”
- Embedded safety messages should be contained within a specific procedure. For example, “To prevent burns, wear protective gloves when performing this procedure.” As stated above, not all of these messages need to be in the Safety Section.

As described above, the cover of the manual should tell the user to read the manual before using the product and then to keep the manual nearby for future reference. In addition to that, the manufacturer should include a label on the product saying the same things and telling the user how to get another manual if the original manual is missing or illegible.

With the message on the cover of the manual and this label on the product, the manufacturer can argue that all of the warnings in the manual but not on the product should have been read before using the product and that they can assume this will be done. Basically, that is what won the case for Black & Decker in the *Broussard* case. However, that was not enough for the court in the *Mohr v. Yamaha* case.

Now you need to figure out what safety messages in the manual should also go on the product. Based on the previous quote in this article by Professor Owen, it sounds somewhat like the factors in a negligence test: 1) the level of hazard (considering probability and severity); 2) the “user’s need for the information” on the product and not just in the manual (considering obviousness and the user’s need to see this precaution each time they use the product), and 3) “the availability of a feasible means to place the warnings on the product” (considering available space and the environment in which the label would be placed).

So, the higher the risk, the more the label should be accessible during each product use. And, the easier it is to place a warning on the product, the more likely it is that you should do so. So, for example, lower level hazards, hazards that only exist during unlikely uses, and maintenance hazards where maintenance personnel are professionals are some of the kinds of hazards where a label may not be necessary.


That being said, add the label when in doubt and where there is room. While there is a possibility that over warning could be used to argue that the warnings are inadequate, I think the risk of liability for under warning is far more likely.¹⁰

If making a final decision is problematic or if the manufacturer truly doesn’t know, it is possible for the manufacturer to do a formal or informal focus group study to try to determine what information would be best to place on the product versus the manual. In other words, they can find out from actual product users what information in the manual these users think should be visible to them each time they use the product.

CONCLUSION

No matter what a manufacturer does in the area of warnings and instructions, a plaintiff will argue that the manufacturer should have done something different and that doing so would have prevented the accident. Given the wide variety of options and analyses that can be done and the lack of clear guidance on this issue concerning most products, the manufacturer should use the factors described above and develop a rationale as to why certain messages are on the product and why some are only in the manual.


PRODUCT showcase

This should lessen the chances of a plaintiff using the location of warnings against the manufacturer and hopefully will provide some defense if such an argument is raised. 

ENDNOTES

1. Restatement Third, Torts: Products Liability, §2 (c), cmt. I
2. *Billiar v. Minnesota Mining and Manufacturing Co.*, 623 F.2d 240, 243 (2d Cir. 1980)
3. *Spruill v. Boyle-Midway, Inc.*, 308 F.2d 79, 85 (4th Cir. 1962)
4. See <https://www.cpsc.gov/s3fs-public/pdfs/guide.pdf> (visited December 1, 2020)
5. Guide to application of the Machinery Directive, section 252 (October 2019)
6. Owen, Products Liability: Third Edition, page 570 (West 2015)
7. *Broussard v. Continental Oil, Co.*, 433 So. 2d 354 (La. App), cert. denied, 440 So. 2d 726 (La. 1983)
8. *Williams v. Super Trucks, Inc.*, La. Ct. App. 2003
9. *Mohr v. Yamaha Motor Co.*, N.J. Super. Ct. App. Div., July 19, 2013
10. See "Is There a Risk to Overwarning?" *In Compliance Magazine*, September 2019

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EMC RESONANCE

PART I: NON-IDEAL PASSIVE COMPONENTS

By Bogdan Adamczyk

This article is part of a two-article series devoted to the concept of resonance in EMC. In Part I the fundamental circuit background is presented and illustrated by the resonance phenomenon in the non-ideal models of passive circuit components: capacitors, ferrite beads, resistors, and inductors. Part II (to appear in the next issue) describes the resonance in the decoupling capacitor circuits.

RESONANCE IN RLC CIRCUITS

In circuit courses, the study of resonance is usually limited to the two classical 2nd-order circuits, series and parallel *RLC* configurations. These circuits, shown in Figure 1, contain a single lumped capacitor and a single lumped inductor connected either “purely” in series or “purely” in parallel.

Actual circuits differ from these classical configurations; in addition to the intentional discrete reactive components, they contain distributed parasitic inductances and capacitances. Nevertheless, the study of these basic *RLC* configurations provides an insight into the more complex topologies and their behavior. Let’s begin with a series *RLC* circuit.

1. “Pure” Series Resonance – Non-Ideal Capacitor Model

Consider the series *RLC* resonant circuit shown in Figure 2.

Since the study of resonance is performed in the sinusoidal steady-state, the voltage and current, in Figure 2, are shown in the phasor forms, and the component values are replaced by their impedances [1].

In order to introduce the concept of resonance, let’s calculate the input impedance to the circuit.

$$\hat{Z}_{IN} = \frac{\hat{V}_S}{\hat{I}_S} = R + j\omega L + \frac{1}{j\omega C} \quad (1.1)$$

or

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$$\hat{Z}_{IN} = R + j\omega L - j\frac{1}{\omega C} = R + j\left(\omega L - \frac{1}{\omega C}\right) \quad (1.2)$$

When

$$\omega L - \frac{1}{\omega C} = 0 \quad (1.3)$$

the input impedance is purely real

$$\hat{Z}_{IN} = R \quad (1.4)$$

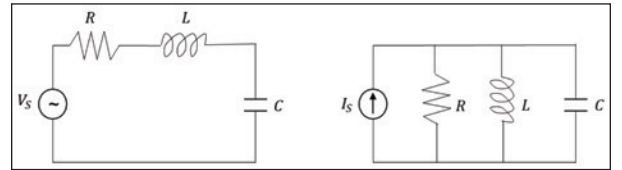


Figure 1: The “classical” series and parallel *RLC* resonant circuits

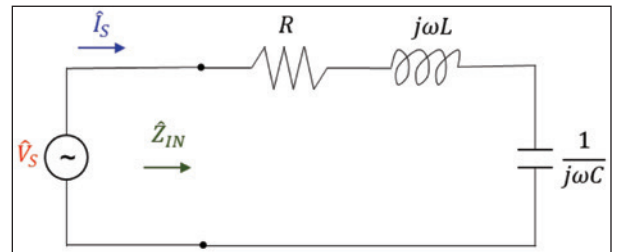


Figure 2: The series *RLC* resonant circuit

This happens at the frequency

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (1.5)$$

From the circuit theory, we recognize this frequency as the undamped natural frequency. Let's look at the consequences of the fact that the input impedance is purely real at that frequency. The voltage and current phasors can be expressed in terms of their magnitudes and angles as

$$\hat{V}_S = V_S \angle \theta_v \quad (1.6a)$$

$$\hat{I}_S = I_S \angle \theta_i \quad (1.6b)$$

Consequently, the input impedance in Eq. (1.1) can be written as

$$\hat{Z}_{IN} = \frac{\hat{V}_S}{\hat{I}_S} = \frac{V_S \angle \theta_v}{I_S \angle \theta_i} = \frac{V_S}{I_S} \angle (\theta_v - \theta_i) \quad (1.7)$$

Since, at ω_0 , the input impedance is purely real, it follows that

$$\theta_v - \theta_i = 0 \quad (1.8a)$$

or

$$\theta_v = \theta_i \quad (1.8b)$$

That is, at ω_0 , the voltage and current are in phase! We have arrived at the definition of the resonant frequency:

The resonant frequency, ω_r , is a frequency at which the voltage and current phasors are in phase (with respect to the same two terminals of the circuit).

Thus, for the series RLC circuit, the resonant frequency is the same as the undamped natural frequency.

$$\omega_r = \omega_0 = \frac{1}{\sqrt{LC}} \quad (1.9)$$

Note: 1) Not every RLC circuit is resonant. 2) When the circuit is resonant, its resonant frequency, in general, is different from ω_0 . 3) The “classical” series

and parallel circuit configurations are always resonant, and their resonant frequency is the same as ω_0 .

At resonant frequency, the magnitude of the input impedance is minimum. Let's illustrate this using a circuit model of a nonideal capacitor [2] and plotting its input impedance. This is shown in Figure 3.

2. “Pure” Parallel Resonance – Ferrite Bead Model

Consider the parallel RLC resonant circuit shown in Figure 4.

Let's calculate the input impedance to this circuit.

$$\frac{1}{\hat{Z}_{IN}} = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C \quad (2.1)$$

Thus

$$\hat{Z}_{IN} = \frac{1}{\frac{1}{R} + \frac{1}{j\omega L} + j\omega C} = \frac{1}{\frac{1}{R} - j\frac{1}{\omega L} + j\omega C} = \frac{1}{\frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right)} \quad (2.2)$$

When

$$\omega C - \frac{1}{\omega L} = 0 \quad (2.3)$$

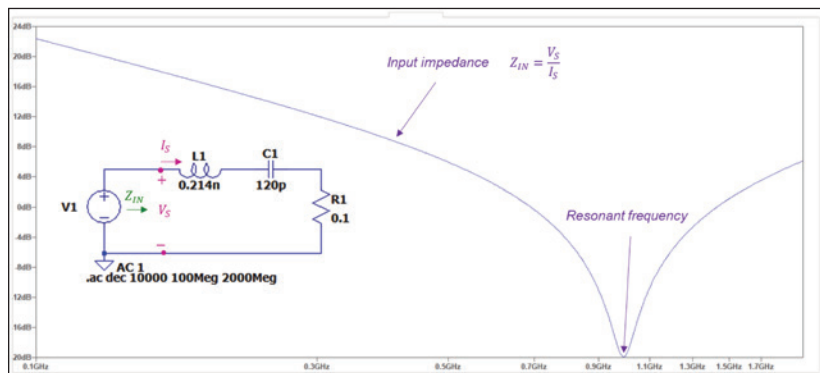


Figure 3: Series RLC circuit – Input impedance is minimal at the resonant frequency

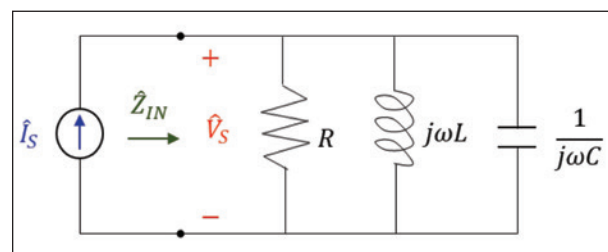


Figure 4: The parallel RLC resonant circuit

the input impedance is purely real (voltage and current are in phase) and equal to

$$\hat{Z}_{IN} = R \quad (2.4)$$

This happens at the resonant frequency of

$$\omega_r = \omega_0 = \frac{1}{\sqrt{LC}} \quad (2.5)$$

Thus, at resonant frequency, the magnitude of the input impedance is maximum. Let's illustrate this by using a circuit model of ferrite bead [3] and plotting its input impedance. This is shown in Figure 5.

3. "Hybrid" Series Resonance – Non-Ideal Resistor Model

Consider a variation of the series RLC resonant circuit, shown in Figure 6.

This circuit corresponds to a non-ideal model of a resistor [2]. Let's calculate the input impedance to the circuit.

$$\hat{Z}_{IN} = j\omega L + R \parallel C = j\omega L + \frac{R}{R + j\omega C} = j\omega L + \frac{R}{j\omega RC + 1} \quad (3.1)$$

or

$$\hat{Z}_{IN} = \frac{j\omega L(j\omega RC + 1) + R}{j\omega RC + 1} = \frac{R - \omega^2 LRC + j\omega L}{j\omega RC + 1} \quad (3.2)$$

Multiplying the numerator and denominator by the complex conjugate of the denominator, and separating the real and imaginary parts, results in

$$\hat{Z}_{IN} = \frac{R}{1 + \omega^2 R^2 C^2} + j \frac{\omega^3 L R^2 C^2 + \omega L - \omega R^2 C}{1 + \omega^2 R^2 C^2} \quad (3.3)$$

The input impedance is purely real (voltage and current are in phase) when the imaginary part of the impedance is zero, or

$$\omega_r^3 L R^2 C^2 + \omega_r L - \omega_r R^2 C = 0 \quad (3.4)$$

Leading to

$$\omega_r^2 = \frac{R^2 C - L}{L R^2 C^2} \quad (3.5)$$

and resulting in a resonant frequency of

$$\omega_r = \frac{1}{\sqrt{LC}} \sqrt{\frac{R^2 C - L}{R^2 C}} = \omega_0 \sqrt{1 - \frac{L}{R^2 C}} \quad (3.6)$$

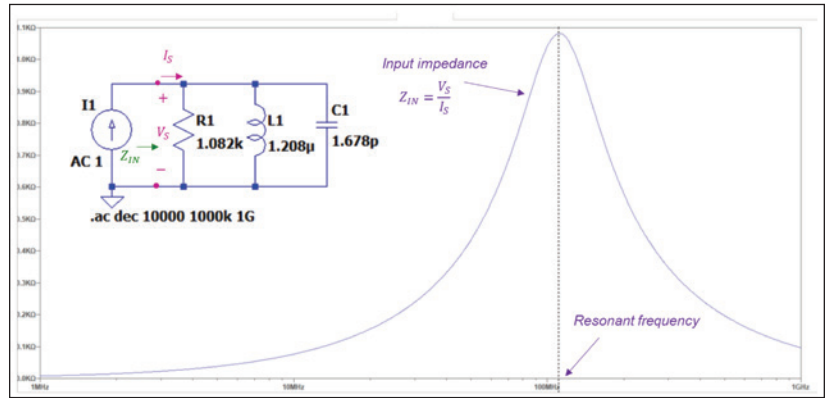


Figure 5: Parallel RLC circuit – Input impedance is maximal at the resonant frequency

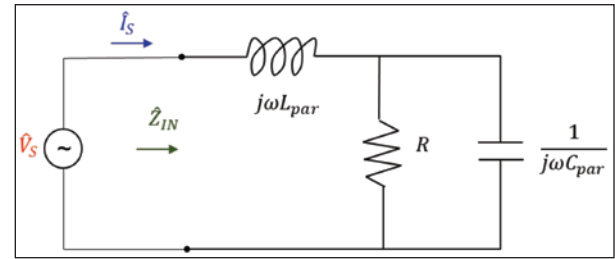


Figure 6: "Hybrid" series RLC resonant circuit

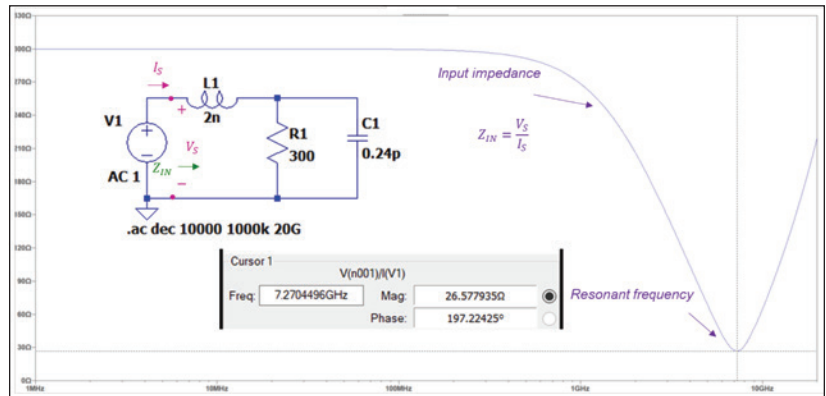


Figure 7: "Hybrid" series RLC circuit – Input impedance of a non-ideal resistor

When

$$\frac{L}{R^2 C} < 1 \quad (3.7)$$

The circuit is resonant, and its resonant frequency is different from the undamped natural frequency. To illustrate the circuit behavior at resonance, let's look at the input impedance of a non-ideal resistor. This is shown in Figure 7.

Note: the simulation model in Figure 7 is used only to show that the hybrid series RLC circuit *with the component values shown* is indeed resonant. This simple model is not valid beyond 2 GHz frequency, and thus, beyond 2 GHz, the simulated impedance plot and the value of the resonant frequency do not reflect the results that would be obtained from the laboratory measurements.

4. "Hybrid" Parallel Resonance – Non-Ideal Inductor Model

Consider the variation of the parallel RLC resonant circuit, shown in Figure 8.

This circuit corresponds to a non-ideal model of an inductor [2]. Let's calculate the input admittance to the circuit.

$$\hat{Y}_{IN} = \frac{1}{-\frac{j}{\omega C}} + \frac{1}{R + j\omega L} = j\omega C + \frac{1}{R + j\omega L} = j\omega C + \frac{R - j\omega L}{R^2 + (\omega L)^2} \quad (4.1)$$

Resonance occurs when the admittance is real, or

$$\omega_r C - \frac{\omega_r L}{R^2 + (\omega_r L)^2} = 0 \quad (4.2)$$

and thus

$$\omega_r C [R^2 + (\omega_r L)^2] - \omega_r L = 0 \quad (4.3)$$

From Eq. (4.3), we get


$$\omega_r^2 = \frac{L - R^2 C}{L^2 C} \quad (4.4)$$

Resulting in a resonant frequency of

$$\omega_r = \frac{1}{\sqrt{LC}} \sqrt{\frac{L - R^2 C}{L}} = \omega_0 \sqrt{1 - \frac{R^2 C}{L}} \quad (4.5)$$

When

$$\frac{R^2 C}{L} < 1 \quad (4.6)$$

The circuit is resonant, and its resonant frequency is again different from the undamped natural frequency. To illustrate the circuit behavior at resonance, let's look at the input impedance of a non-ideal inductor. This is shown in Figure 9. 

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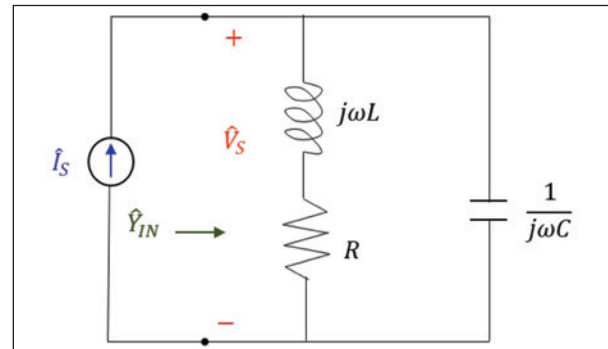


Figure 8: "Hybrid" parallel RLC resonant circuit

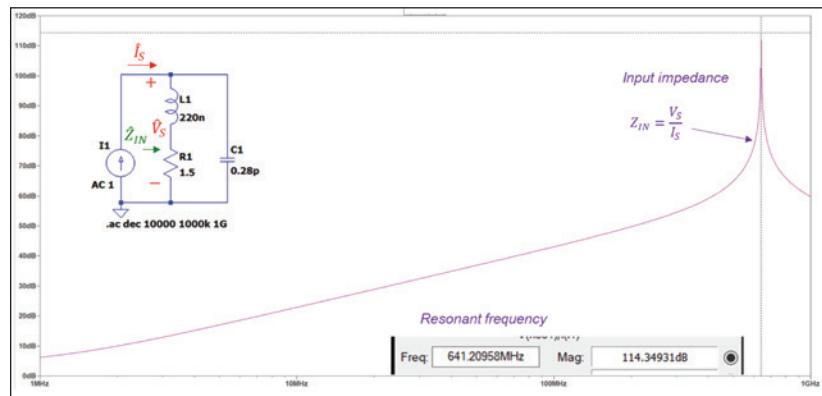


Figure 9: "Hybrid series RLC circuit – Input impedance of a non-ideal inductor

ESD ISSUES FOR FLAT PANEL DISPLAYS

By Joshua Yoo for EOS/ESD Association, Inc.

INTRODUCTION TO FLAT PANEL DISPLAYS AND THE CURRENT STATE OF THE ART

Electronic displays have been widely adopted around the world, and information displays have become an essential part of human life. Flat Panel Displays (FPD) products like smartphones, tablets, televisions, and wearable displays use LCD and organic light-emitting diode (OLED) technologies for most current display devices. As innovation comes from many sources, it is difficult to predict or accurately forecast future display technology development. Curved and flexible displays were introduced as the most innovative display technology achievement along with OLEDs in the last ten years. Flexible displays are a different segment from traditional FPDs, using plastic base material instead of glass, or extremely thin glass, which can change shape without breaking. As in these results, we are recently seeing newly introduced foldable smartphones from several manufacturers and widely adopted by users.

The obvious changing trends in display technology are products getting thinner and lighter and flexible display devices. There is a common trend for higher resolution and pixels per inch (PPI) and increasing screen sizes for new display devices. Also, there are continuous developments for brighter, lower reflectance displays for better visibility under high ambient light conditions. Future display trends will continue to be introduced at industry trade shows including Internationale Funkausstellung (IFA) and International Consumer Electronics Show (CES). Some of the newer technologies and finished products are Quantum Dots, curved and flexible displays with higher resolution and higher pixels per inch, Low-temperature polycrystalline silicon (LTPS) and Indium gallium zinc oxide (IGZO) technology, OLED, and transparent display technologies.

Joshua (Yong Hoon) Yoo is a president of Core Insight, Inc. He served on the EOS/ESD Association, Inc. Board of Directors during 2016 – 2018. He is an active member of standard working groups for Process Assessment, EOS Best Practices, High Reliability, Ionization and was a chair of the Flat Panel Display (FPD) working group. He is an expert and technical support for micro contamination and ESD issues in the FPD industry with 25+ years of experience in the static control industry. He holds certification as a Professional ESD Program Manager and iNarte ESD Engineer.



Founded in 1982, EOS/ESD Association, Inc. is a not for profit, professional organization, dedicated to education and furthering the technology Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, tutorials, and foster the exchange of technical information among its members and others.



Q. What are the FPD manufacturing details that can be a potential problem for ESD (like defects, glass material properties, etc.)?

Initially, ESD problems were not an issue until a few years ago, but ESD has now become a more significant reason for yield loss due to changes in panel technology, such as higher definitions, fast refresh rates, narrow bezel, and adopting thinner glass substrates, etc. FPD manufacturing processes are similar to semiconductor wafer processes and much simpler. But for economic reasons, the industry has adopted extremely large glass substrates that have greater capacitance and generate more energy compared with 300mm wafers.

During FPD fabrication processes, a variety of charge generation elements can cause static related issues. For example, friction from photoresist coated glass substrate and deionized water spray rinses in the cleaning process causes charge generation. There is also charge generation when glass substrates transfer through conveyor rollers between processes. Most ESD damage on glass substrates resembles CDM

damage after semiconductor device testing. A major difference between legacy CDM and ESD discharge on glass substrates is the discharge energy path to ground. ESD phenomena on glass substrates have no ground path and limited current flowing; thus breakdown events occur between metal structures or between thin films that are at different potentials.

Q ■ How is ESD in the FPD production process controlled? Are there any gaps between ESDA standards?


Most FPD manufacturers have requirements from the Original Equipment Manufacturers (OEM) to follow ANSI/ESD S20.20 or IEC 61340-5-1 standard as factory ESD control guidelines. This is an obvious dilemma for them because their devices aren't wafer-based semiconductor ICs, but glass or plastic substrate-based. Glass substrates can't drain their charge to ground through static dissipative materials as wafers do. Their operating personnel does not touch any items during the manufacturing process. The process is a fully automated in-line system that automatically transfers substrates between processes. ANSI/ESD S20.20 does not address FPD and automated handling equipment within ESD protected areas (EPA).

The FPD manufacturers control their processes based on their own failure and control experiences, not published standard documents. There is no published standard document to describe how to test FPD panels or completed display panel modules that have repeatable results. There is no published standard for requirements for the fabrication process. There are technical gaps and communication issues between FPD manufacturers and OEMs about correct control methods.

Q ■ What challenges remain?

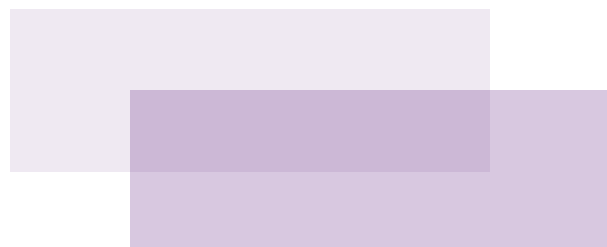
For semiconductor device qualification, HBM and CDM testing standards are globally accepted and have repeatable results for the electronics industry. IEC 61000-4-2 is a test methodology for completed electronic systems for ESD EMC compliance. For FPD, ESD damage occurs on panels only during

fabrication, panels with ICs as sub-system level (module), and completed systems through various ports. None of these failure modes have a detailed explanation or can be tested with methods in technical documents. WG21 – FPD is trying to publish a second Technical Report (TR) that addresses these issues. The first WG21 TR introduced basic ESD issues on FPD. FPD damage mechanisms, testing issues, and factory control documents need to be created based on the ANSI/ESD S20.20 standard. Some of the elements in S20.20 may remain unaddressed, and there may be some additional requirement for display panels, which are glass or plastic substrates.

To create these documents and make them technically correct, the EOS/ESD Association, Inc. invites volunteers and experts who are working in FPD manufacturing organizations and interested in ESD damage on FPD devices. 

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PRODUCT SAFETY AND THE PANDEMIC

By Erin Earley

Considerations for Your Warnings and Instructions in the COVID-19 Landscape

The pandemic has brought many changes in the way we do business. For equipment manufacturers, that may equate to big picture shifts related to your supply chain, vendors, and production. At the time of writing, COVID-19 continues to surge; even once the virus is better contained, though, its impact in areas like those will likely have a lingering effect for some time to come. Here, let's explore key considerations to keep in mind for your product safety strategy, warnings, and instructions.

OUR COVID-19 WORLD AND PRODUCT MANUFACTURING

Safety and risk reduction is a key component of pandemic business continuity plans.

"Over the past months, a common trend we've seen with product manufacturers is the need to reevaluate their supply chains to ensure they're well-positioned to continue business despite hurdles with the current environment – everything from vendor shutdowns to issues with fulfilling orders," says Angela Lambert, who consults with product safety teams on a regular basis through her role heading standards compliance at Clarion Safety Systems.

When changes occur to global supply chains and production capabilities it may, in turn, bring shifts to your product safety strategy, including warnings and instructions. That can range from evaluating the quality and on-time delivery of new vendors, or on a wider level, the actual warnings and instructions used, based on shifts to your audience.

Erin Earley, head of communications at Clarion Safety Systems, shares her company's passion for safer products and workplaces. She's written extensively about best practices for product safety labels and facility safety signs. Clarion is a member of the ANSI Z535 Committee for Safety Signs and Colors, the U.S. ANSI TAG to ISO/TC 145, and the U.S. ANSI TAG to ISO 45001. Erin can be reached at earley@clarionsafety.com.



KEY CONSIDERATIONS FOR LABEL FORMATS AND SYMBOL USE

When it comes specifically to keeping your warnings and instructions up to date with the times, one initial benchmark is to look at your product's intended audience to see if any recent changes have occurred. The intended audience is made up of those who should be warned because they may come into contact with potential hazards during any phase of the equipment or machinery's lifecycle.

"Pay special consideration to their location and any changes from that standpoint," says Lambert, who is also involved at the leadership level in the development of the ANSI and ISO standards for product safety, including as the chair of ANSI Z535.1 Safety Colors. "Depending on whether your audience is primarily U.S. or internationally-based will help you to decide if your focus is on adhering to the ANSI or ISO product safety label standards."

That's because these two main standards for product safety label and symbol choice are based on audience location: the *ANSI Z535.4 Standard for Product Safety Signs and Labels* is for domestic use while *ISO 3864-2 Graphical symbols – Safety colours and safety signs* –

Part 2: Design principles for product safety labels is for international use.

You have several main choices to be aware of, contingent on whether your products are shipped and used within the U.S. or internationally – and whether you choose to focus on the ANSI or ISO standards:

- **Use of internationally-recognized symbols:**

While ANSI doesn't mandate symbol use, symbols are highly encouraged. Follow best practice by using ISO 7010 symbols – or ones created with ISO design principles. The ISO 7010 standards establish one consistent, worldwide library of symbols – continuously refreshed.

- **Use of the right safety alert symbol:**

On your hazard alerting labels, per ANSI Z535.4, you have the option to use several different types of safety alert symbols. See Figure 1. Versions D and E are provided to allow for consistency with ISO standards; one of these two versions is needed to align with both the ANSI and ISO standards.

- **Use of at least one symbol within an ISO colored surround shape:** If your goal is to comply with the ISO standards, an ISO-formatted surround shape must be used around at least one safety symbol in your warning (keep in mind that excludes the safety alert symbol). See Figure 2. Symbols without an ISO colored surround shape can be used in addition to one or more ISO formatted symbols (called a “supplementary safety symbol” by ISO).

EFFECTIVE SAFETY LABELING: AN ONGOING DECISION-MAKING PROCESS

Our world, and our individual businesses, will continue to be shaped and forced to evolve in


light of the pandemic. One constant when it comes to labeling is that thoughtful decisions need to be made concerning how to warn effectively. That includes reevaluating your product safety strategy on a continuous basis, performing routine risk assessments (fundamental for product safety and warnings), and designing your labels to meet identified needs using standards-based best practices. With those areas prioritized, you're on the right path to doing everything possible so people can take the steps necessary to avoid harm. 



Figure 1: Safety alert symbol variations listed in ANSI Z535.4.



Figure 2: Examples of label formats that fail to comply (top) and comply (middle and bottom) with ISO 3864-2:2016. Per the standard, labels must use at least one ISO-formatted safety symbol in addition to the safety alert symbol in the label's severity level panel.

Banana Skins

Banana Skins numbered 316–317 describe interference events that we might not be too surprised to hear about in or after 2015.

316 2015: Vacuum cleaner interferes with space station navigation

A number of people who had been enjoying weightless activities in the non-spinning central hub of Virgin Space Ltd's newest hotel "Arthur C Clarke III" found themselves trapped on the 'ceiling' for 15 minutes, unable to reach the doors that were now 6 metres 'up' a smooth wall. The cause was a new cleaning droid. When it plugged itself into the wall sockets in the corridor in the engineering section a 0.5g acceleration occurred. It was later found that the corridor power sockets were on the same branch of the power bus as the navigation computer, and conducted interference from the new droid caused the asteroid-avoidance emergency thrusters to fire. The droid has refused to comment.

(Possibly from the Sunday Times News Review section, one week in 2015.)

317 2015: Intelligent cruise control interferes with latest silicon chips

The 30nm silicon fabrication process is now well-established and helping create many products and provide services that even ten years ago would have been considered science fiction. But investigations by York University into claims of unstable personalities in the latest models of robotic personal companions has revealed that ICs made with 30nm silicon features are very susceptible to the 76GHz radars used by the car-train systems required by automated highway systems. 76GHz automotive radar technology first appeared in the early years of this century as 'intelligent cruise control' or 'automatic emergency braking' systems for luxury vehicles, and is now ubiquitous. York University is now

seeking sponsors for a programme of investigation into low-cost techniques for shielding and filtering at 76GHz.

(Possibly from the News section of The EMC Journal in 2015.)

318 New battery pack significantly reduces RF immunity of life vest, causes malfunctions

An example of a subtle change in hardware configuration to the original design concept can be found in a life vest. The life vest was fielded with a bridgewire EID that could be fired by a salt-water activated battery pack that had been hardened and certified for HERO. After introduction into the fleet, an engineering change proposal was developed, and approved, to modify the type of battery used in the battery pack. The change was not submitted for HERO consideration. When the life vests were equipped with the new battery pack and used on board Navy ships, there were reports of uncommanded activation of the vests during flight operations and on the flight deck. The subsequent investigation found that the new battery pack made the EID subsystem resonant to a ship radar system; thereby creating susceptibility problems.

(Taken from MIL-STD-464A, Appendix A.5.9 "Life cycle, E3 hardness". 'HERO' stands for Hazards of Electromagnetic Radiation to Ordnance.)

319 Most ESD test generators do not simulate real-life ESD events

Even though all the (*ESD test*) generators have peak current values and risetimes very similar to the ones specified in the standard, some of the generators fail the equipment under test (EUT) at vastly different voltage levels from the others. A range of 1:5 is shown in the second part of this two-paper series. This indicates that even

though all the generators are made in accordance with IEC 61000-4-2 they produce different ESD events leading to a serious repeatability problem when the same EUT is tested with different brand generators. The problems have been well documented although the connection between parameters and EUT failures has been speculative so far.

As the fraction of devices that use fast CMOS is increasing, and going to continue to increase in the future, changes in the ESD standard are needed. Without such changes, the growing fraction of devices that can respond to pulses having widths of tens to hundreds of picoseconds will lead to an increasing dependency of the test result on the model of ESD generator selected.

For an EUT that reacts to the lower frequency (<1GHz) current components, the effect of changing the ESD generator model should not be larger than 1:3. In fact, we have not observed any ratio of EUT failure voltages above 1:2. In contrast, modern CMOS circuits with less than 0.15µm technology can react to pulses as narrow as 50ps. These circuits will respond to the fast-changing (unintended) components of the induced voltage. The effect (*on such fast devices – Editor*) of changing the ESD generator model may be as large as 1:10, as the spectral density varies by more than 20dB, as shown in our Fig. 3. Our observations showed a 1:5 variation.

With the introduction of more and faster CMOS circuits, the large influence of the ESD generator model, shown in Fig. 4, will occur more often if the ESD standard is not improved.

How many of the ESDs will have a larger severity than the reference event? Due to the strong dependence on factors like humidity, personal activity, clothing, etc, there is no final answer. Generally, for lower voltages the typical rise times are much shorter

and the rate of occurrence of ESD is larger, but fast rising ESD having less than 300ps rise time can also occur under dry conditions and fast approach speeds at voltages as high as 15kV.

These low-voltage ESDs and higher voltage ESDs having short arc-lengths show short rise times, as low as 50ps, thus their high-frequency content is much stronger. Up to now some widely used ESD generators not only covered the spectral content of the proposed reference event, but also tested for fast rising ESDs. They did not do so intentionally, but as a result of their design, which was based on incomplete understanding of the failure mechanisms in fast electronic systems and insufficient specifications.

In our opinion, the ESD standards IEC 61000-4-2 should be revised such that ESD generator performance is as similar to the reference events as possible in all their parameters. But manufacturers and users need to be aware that the standard does not cover all possible ESD events. For example, medical equipment might need to be tested using a shorter rise time to cover a larger portion of the real ESDs, notwithstanding furniture ESD or other ESD types. The standard needs to be understood as a minimum requirement, passing it does not protect against ESD related field failures.

(The above are some paragraphs taken from "Characterization of Human Metal ESD Reference Discharge Event and Correlation of Generator Parameters to Failure Levels — Part I: Reference Event" and "— Part II: Correlation of Generator Parameters to Failure Levels" by K Wang, D Pommerneke, R Chundru, T Van Doren, F P Centola, and J S Huang, IEEE Transactions on EMC Vol. 46 No. 4 November 2004, pages 498-511.)

The regular "Banana Skins" column was published in the EMC Journal, starting in January 1998. Alan E. Hutley, a prominent member of the electronics community, distinguished publisher of the EMC Journal, founder of the EMCIA EMC Industry Association and the EMCUK Exhibition & Conference, has graciously given his permission for In Compliance to republish this reader-favorite column. The Banana Skin columns were compiled by Keith Armstrong, of Cherry Clough Consultants Ltd, from items he found in various publications, and anecdotes and links sent in by the many fans of the column. All of the EMC Journal columns are available at: <https://www.emcstandards.co.uk/emi-stories>, indexed both by application and type of EM disturbance, and new ones have recently begun being added. Keith has also given his permission for these stories to be shared through In Compliance as a service to the worldwide EMC community. We are proud to carry on the tradition of sharing Banana Skins for the purpose of promoting education for EMI/EMC engineers.

320 Phone masts interfere with car immobilisers and alarms

Customers at two garages in Birmingham are reportedly being forced to freewheel their cars off the forecourt. 'National Tyres' and 'Car Spares', both on the city's Stratford Road, are experiencing interference from phone masts on the roof of the Centre Court office block and visitors to the sites have to push their cars nearly 100 yards out of range of the masts before starting them.

Clive Carter, from National Tyres garage, and Keith Murphy, from Car Spares, told the Birmingham Post that many customers could not start their vehicles in their forecourts. It is believed the mast's rays are interfering with car's ignition systems, immobilisers and alarms. Mr Carter said: "This has happened at least 20 times in the last year. The strange thing is that when a car is pushed down the road it starts easily. The mobile phone masts seem to be the only explanation for it."

(Taken from the HSE's internal newsletter, 7/3/05, sent in by Simon Brown)

321 Electromagnetic pulse gun stops speeding cars at 50 metres

A hi-tech device that can bring speeding cars to a halt at the flick of a switch is set to become the latest weapon in the fight against crime. Police forces in Britain and the US have ordered tests of the new system that delivers a blast of radio waves powerful enough to knock out vital engine electronics, making the targeted vehicle stall and slowly come to a stop.

David Giri, who left his position as a physics professor at the University of California in Berkeley to set up a company called ProTech, is developing a radio wave vehicle-stopping system for the US marine corps and the Los Angeles police department. Tomorrow, at the Euroem 2004 science conference in Germany, Dr Giri will describe recent trials of the device. The tests proved that the system could stop vehicles from up to 50 metres away.

The bulk of the device is designed to fit in a car boot and consists of a battery and a bank of capacitors that can store an electrical charge. Flicking a switch on the dashboard sends a burst of electricity into an antenna mounted on the roof of the car. The antenna then produces a narrow beam of intense radio waves that is directed at the vehicle ahead. When the radio waves hit the targeted car, they induce surges of electricity in its electronics, upsetting the fuel injection and engine firing signals. "It works on most cars built in the past 10 years, because their engines are controlled by computer chips," said Dr Giri. "If we can disrupt the computer, we can stop the car." A prototype is due to be ready by next summer.

The Association of Chief Police Officers confirmed that researchers at the Home Office's police scientific development branch are testing a radio wave vehicle-stopping system. "There's a potential to use this type of device to stop criminals on the road. High speed pursuits are very dangerous, especially in built-up areas," said an association spokesman.

(From "Police test hi-tech zapper that could end car chases", Ian Sample, science correspondent, Monday July 12, 2004, <https://www.theguardian.com/science/2004/jul/12/sciencenews.crime>.)

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Upcoming Events

February 16-19

Military Standard 810 (MIL-STD-810) Testing Open Course

March 2-4

Fundamentals of Random Vibration and Shock Testing

March 22-26

EUCAP 2021 - The 15th European Conference on Antennas and Propagation

April 5-9

EMC Week

April 22-23

Principles of Electromagnetic Compatibility

May 3-7

EMC+SIPI 2021

May 11

Annual Chicago IEEE EMC MiniSymposium

May 13

EMC Fest 2021

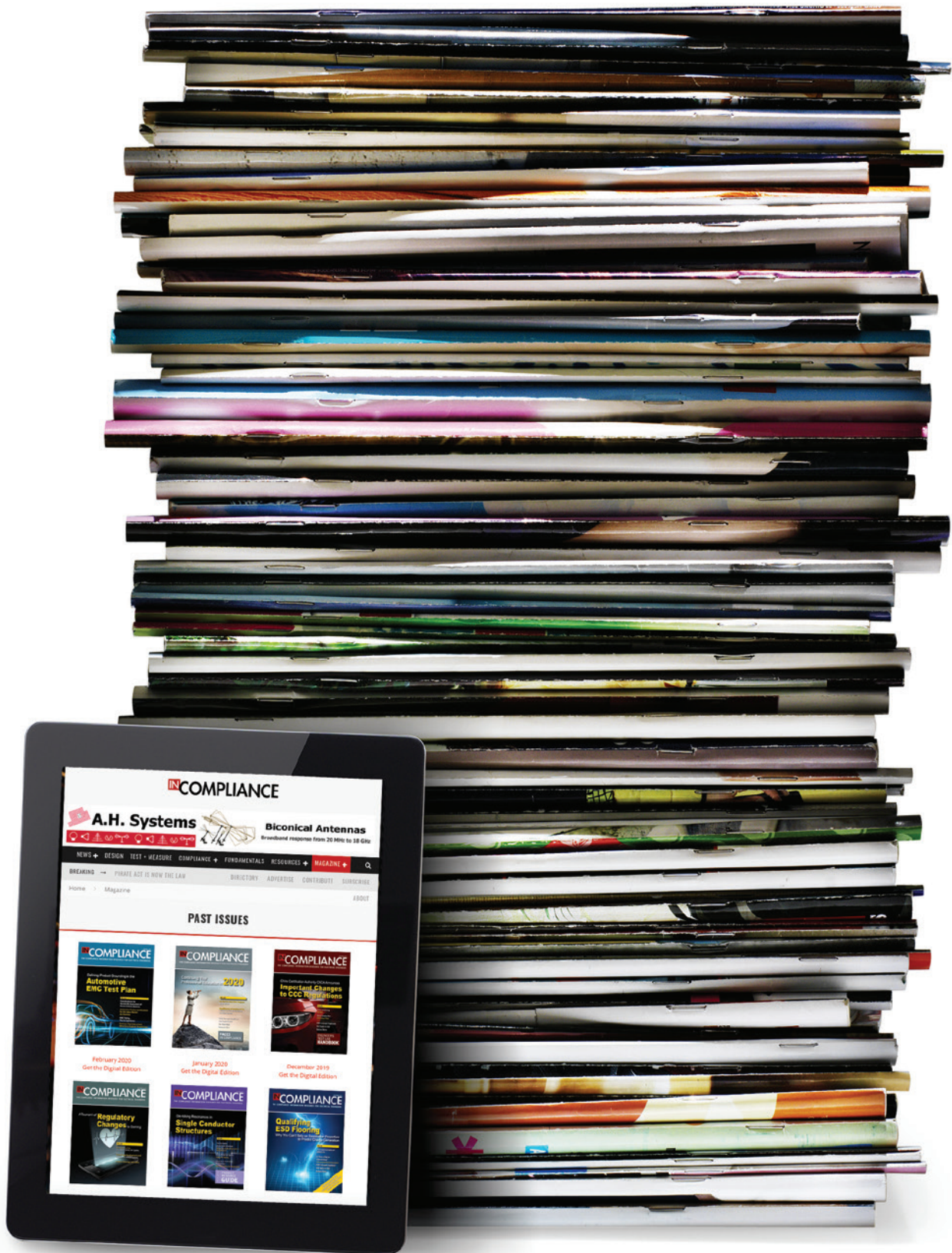
May 19-20

EMC & Compliance International 2021 Workshop

Due to COVID-19 concerns, events may be postponed. Please check the event website for current information.

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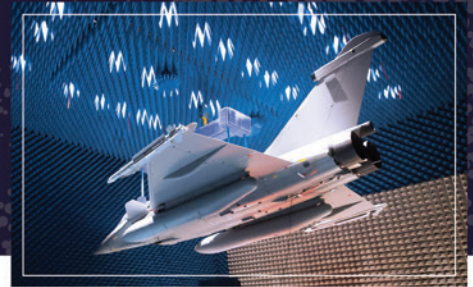
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