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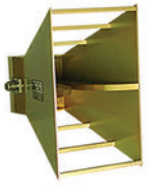

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FEATURE ARTICLES

SPECIAL COVERAGE

COLUMNS

DEPARTMENTS

All Mobile Phones Must Be HAC, says FCC

The U.S. Federal Communications Commission (FCC) has adopted new rules requiring that all mobile phones available on the market be compatible with hearing aid technologies (i.e., hearing aid compatible, or HAC).

According to an FCC press release announcing the rule change, the new rules are the result of years of extended discussions and collaboration by members of the FCC's Hearing Aid Compatibility Task Force. Once implemented, the 100 percent HAC requirement will provide an additional 48 million Americans dealing with hearing loss with the flexibility of choosing any model of mobile phone available to the general public.

In addition to the 100 percent HAC requirement, the FCC has also established a Bluetooth coupling requirement that will help to ensure connectivity between mobile handsets and hearing aids. Further, the FCC rules also require that all newly introduced mobile handsets meet volume control requirements that allow users to adjust handset audio volume without introducing distortion.

Mobile handset manufacturers have 24 months to comply with the FCC's new HAC requirements. Nationwide service providers are given a transition period of 30 months, while non-nationwide service providers have 42 months.

FDA Classifies Radiofrequency Toothbrush as Medical Device

As new and emerging technologies continue to define and influence our lives in the 21st Century, regulators must work to ensure that their own efforts reflect the latest technology developments and address potential regulatory and safety concerns.

The case is perhaps most interestingly illustrated by a decision by the U.S. Food and Drug Administration (FDA) regarding its review of an electric toothbrush that uses radiofrequency (RF) waves to remove plaque and stains from teeth. Developed by the company Home Skinovations Limited, the ToothWave™ electric toothbrush uses patented RF technology to direct RF waves to the teeth and gum line. The company claims that the RF waves destabilize impure molecules that bond to teeth and replaces them with new, purer molecules that provide a stronger protective layer.

The company submitted a De Novo classification request regarding the device to the FDA back in 2019. After a year-long extensive review, the FDA classified the toothbrush as a Class II device, that is, a device that requires specific "special controls" to provide reasonable assurances of the safety and effectiveness of the device for its intended use.

In the latest development, the FDA has now modified its regulations under 21 CFR Part 872, adding a "radiofrequency toothbrush" as a regulated device. In a Final Amendment and Final Order, the FDA now defines specific requirements applicable to this advanced dental care product that are intended to mitigate potential risks to health associated with the use of such a device.

ARRL Releases Updated Amateur Radio Handbook

The National Association for Amateur Radio (ARRL) has announced the release of an updated version of its classic guide to amateur radio technology and practice.

According to a press release posted on the ARRL website, the newly-released 101st edition of The ARRL Handbook captures "the state of radio science and technology in one authoritative work." The six-volume set spans over 1200 pages and provides a "deep dive" into radio electronics, circuit design, digital modulation techniques, and equipment construction.

Important updates to the latest edition of the Handbook include:

- Information on electromagnetic analysis, as well as cost-effective tools for modeling circuits, antennas, and propagation;
- Radio astronomy receiver and antenna design information;
- A newly added section on batteries and battery safety; and
- Updated information on RF safety and compliance with FCC exposure regulations.

Upcoming Events

December 3-5, 2024
Fundamentals of Random Vibration and Shock Testing Training

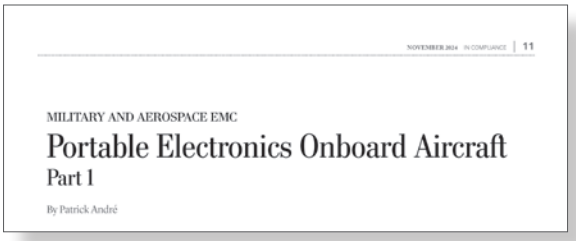
January 28-30, 2025
DesignCon 2025

LETTER TO THE EDITOR

The article in the November issue "Portable Electronics Onboard Aircraft" was quite informative. It is my understanding that the problem first arose when passengers' FM broadcast receivers interfered with communication and navigation signals. The FM broadcast band runs from 88 to 108 MHz, and the aircraft communication and navigation band runs from 118 to 137 MHz, with additional VOR navigation between 108 and 118 MHz.

Since the local oscillator in an FM superhet receiver normally runs 10.7 MHz (the IF) above the receiving frequency, and since the oscillator is rarely shielded against stray emissions, its radiation will almost certainly interfere with the aircraft's communication or navigation when a passenger's receiver is tuned between 97.3 and 108 MHz. Interference from other portable electronics arose in later years.

— Jonathan Allen



FROM THE AUTHOR

Thank you for the kind words and thank you for the additional information. Superheterodyne receivers do have a known ability to transmit at their local oscillator frequency, which is how the police can detect the use of radar detectors (called a radar detector detector of course).

— Patrick André

EMC BENCH NOTES

Embedded Processor Characterization and Design Review

By Kenneth Wyatt

Let's use the basic tools and spectrum analyzer setup I described ***in the last two months*** and use them to characterize an actual embedded processor board based on the Arduino design. I'll be using an "OSEPP Bluetooth" board, but you can use anything on hand or similar (Figure 1). The schematic and board layout are available in Reference 1. While most Arduino-based boards use linear regulators, I chose this board from my collection because it includes a DC-DC converter and uses a two-layer design with obvious EMC issues.

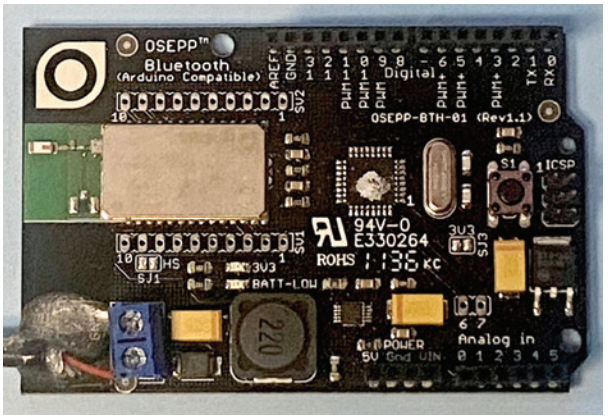


Figure 1: Our example unit under test is an Arduino-based single-board embedded processor with Bluetooth.

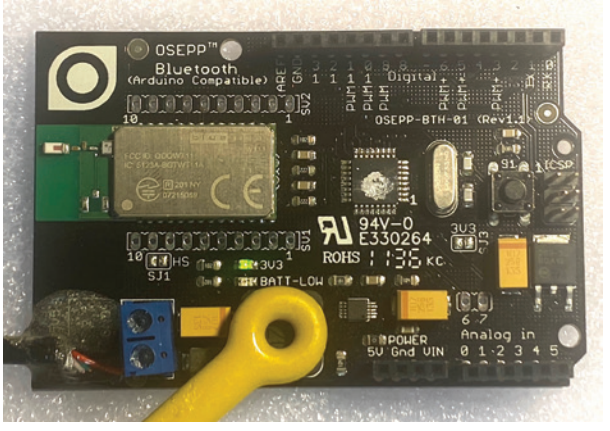


Figure 2: Probing the DC-DC converter switching currents by coupling the medium-sized H-field loop to the switching inductor, L1.

CHARACTERIZATION

This is a great board to evaluate and characterize for EMC issues. It is a two-layer board with ground fill but no solid return planes. It also includes an onboard DC-DC boost converter with a three-terminal 3.3V linear regulator. The processor is an ATMEGA328P with an external 16 MHz crystal clock. There is no other circuitry on the board other than the Bluetooth module, which we won't be evaluating.

Let's make some near field probe measurements; first on the DC-DC converter. This is easy to identify because of the large 22µH inductor at the bottom of the board. We'll non-invasively couple to the inductor (Reference 2), which is connected to the MAX1676 boost converter. Figure 3 shows the resulting frequency domain plot. Placing the spectrum analyzer in Max Hold mode, we can see a lot of switching energy extending out to 200 MHz. You'll notice that for each plot, I record the system noise floor (yellow trace). I also placed markers at some of the resonant peaks, which we may use in possible future analyses.

In addition, probing around the processor (Figure 4) reveals a lot of 16 MHz harmonic energy along with the broadband energy from the DC-DC converter (Figure 5).

Note that to confirm these narrow band harmonics are indeed 16 MHz, I have placed markers 3 and 4 on adjacent peaks. Subtracting the two frequencies confirms this.

Now, let's clamp our current probe around the DC power input cable (Figure 6). I've inserted some "bubble wrap" around the power cable to help isolate it from the metal case of the probe. Here, we observe very strong broadband switching noise with a 16 MHz peak (Figure 7).

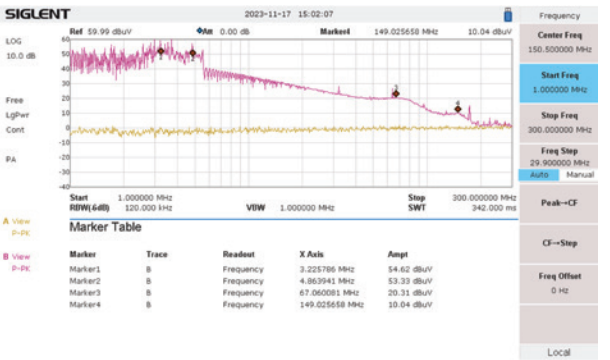


Figure 3: The resulting plot of the DC-DC converter. Note the broadband energy extends out to 200 MHz. The yellow trace is a record of the system noise floor.

Now that we've characterized the high-frequency currents traveling along the power cord, how about measuring the harmonic energy of a wire connected to the system ground return? This would represent an I/O cable, such as a USB, attached to the board (Figure 8).

Using a standard paper clip pushed into the "Gnd" socket and connecting a short clip lead, I measured the emissions in Figure 9. Note that we still see the broadband emissions from the DC-DC converter, as well as several 16 MHz harmonics from the processor clock.

Figure 4: Using the medium-sized H-field probe to characterize the 16 MHz clock harmonics. These narrow band harmonics extend past 500 MHz.

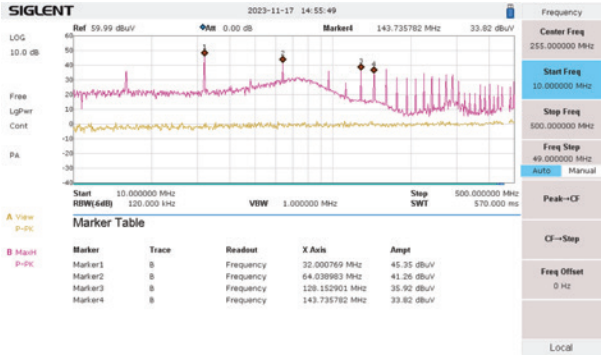


Figure 5: It is easy to observe the 16 MHz clock harmonics that extend past 500 MHz. The yellow trace is a record of the system noise floor.

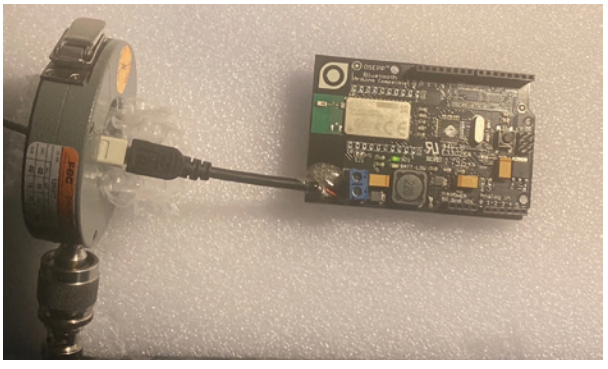


Figure 6: Using an RF current probe to measure the high-frequency harmonic currents flowing along the DC power cord.

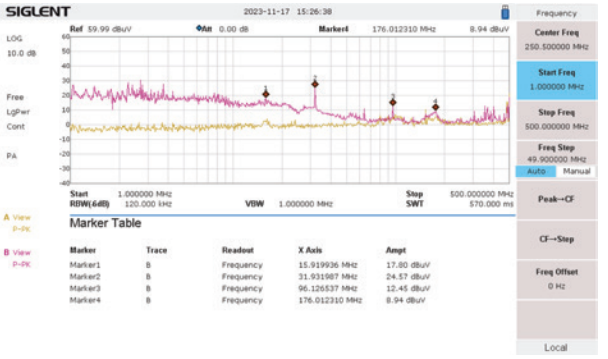


Figure 7: Not only is there the usual broadband EMI due to the DC-DC converter, but we also observe several 16 MHz clock harmonics. These would likely cause radiated emissions. The yellow trace is a record of the system noise floor.

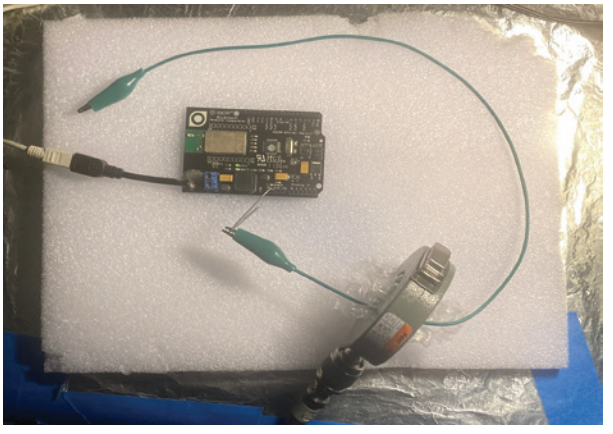


Figure 8: We can simulate an I/O cable, such as USB, by connecting a wire to the system ground return and measuring the high-frequency harmonic currents using an RF current probe.

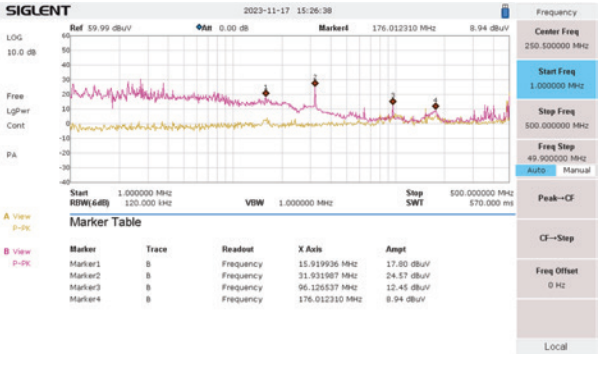


Figure 9: The harmonic currents measured on a short wire connected to the PC board ground return. There is a resonance at 128 MHz, the half-wavelength of the power cable, board, and wire combination. The yellow trace is a record of the system noise floor.

Note the interesting broad peak at 128 MHz. This is a half-wave resonance due to the combined length of the power cord, circuit board length, and attached wire. These physical resonances can reduce the margin or even throw you over the limit if not mitigated.

MITIGATION SOLUTIONS

Let's find out why this board is so noisy! Looking at the top and bottom layers reveals the main issue, and that is no solid return plane (Figure 10).

Ground fill is a fairly common technique when laying out PC boards, and one of the main reasons is that it conserves the etching chemicals and/or prevents board warpage. However, for EMC reasons, ground fill is debatable as to usefulness and can actually lead to "high-frequency traces crossing gaps" (Reference 3). In the case where we lack a solid return plane, this issue is compounded by the multiple possible couplings between top and bottom layer routing.

Digital signals are not the result of electron flow through circuit traces but are propagated via electromagnetic waves between the circuit trace and the nearest other metal. Because we lack a solid ground return plane, these EM waves must be "trapped" between two pieces of metal at all times to propagate the signal energy from point A to point B. However, without an adjacent and solid return plane, the signal energy in the EM wave will couple to all other traces they pass by. Please refer to my PC board design series starting with Reference 4.

It's possible to re-lay out this board with the top layer as mainly routed power and signals and then use a semi-solid return plane for the bottom layer with minimal non-critical signal routing. You'd need to be careful to avoid high-frequency traces crossing gaps in this return plane.

Many of my clients have already invested their design in a two-layer board, only to learn at the last minute that it may never pass EMC requirements. So, often, I'll suggest keeping the current layout but simply adding two additional ground return planes as layers 2 and 3, which should be bonded together (along with all ground fill) with stitching vias in a grid pattern. Today, the cost differential between two- and four-layer boards is insignificant, so this is often the most cost-effective solution. The suggested stack-up is shown in Figure 11.

SUMMARY

In this exercise, I've purposely selected a board design with known design issues to show the basic process I use for characterizing a circuit board using some basic

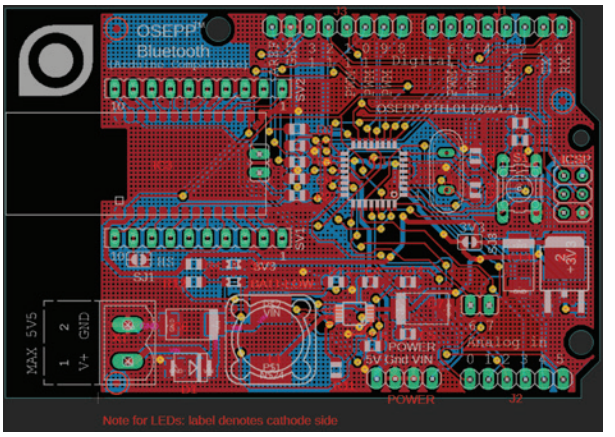


Figure 10: Here is the PC board layout showing the top (in red) and bottom (in blue) layers. Because there is no solid ground return layer, the fields from the DC-DC converter and 16 MHz clock couple throughout the board.

EMC probes. I suspect that adding the two solid ground return planes would resolve most of the emissions and immunity problems.

There are other design issues that would preclude me from using this particular board in a "real" product. For example, it lacks power input filtering as well as filtering or ESD protection on the I/O pins. I'd also change the I/O connectors to include optional I/O cable shields.

In future articles, we'll be characterizing a more complex embedded computer with USB, Ethernet and HDMI ports, along with multiple DC-DC converters.

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2. Wyatt, "Characterize DC-DC converter EMI with near-field probes," *EDN*.
3. Wyatt, "Gaps in return planes - yes or no?" *EDN*.
4. Wyatt, "Design PCBs for {low} EMI, Part 1: How signals move," *EDN*.

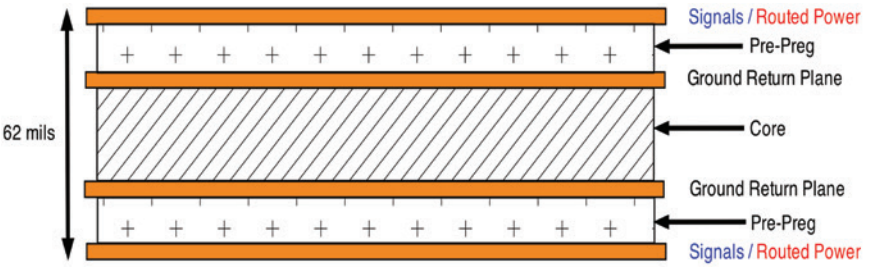


Figure 11: One possible stack-up suggestion with two added ground return planes that would likely mitigate most all the EMC issues: radiated, conducted and immunity.

MILITARY AND AEROSPACE EMC

Portable Electronics Onboard Aircraft
Part 2

By Patrick André

In the last blog, we discussed how the FAA and aircraft industry recognized that personal electronic devices, or PEDs, were causing problems aboard aircraft. With the proliferation of PEDs onboard, and especially those with wireless capabilities, action was needed quickly to address safety concerns. The FAA requested the RTCA form a new committee, SC-202, made up of over 100 individuals from the aircraft industry, airlines, computer, medical, telecommunication, and commercial electronics industries, consultants, FAA, and elected officials. The group was formed specifically to address PEDs that had transmitters, cellular technology, wireless radio frequency networks, and the like. These transmitting PEDs are referred to as T-PEDs.

There was a recognition that guidance for the use of T-PEDs was extremely important. Incidents were being reported, often anecdotal and erroneous or misinterpreted. However, it created much interest in the media and the public. Several issues with PEDs were found, including:

- They were not configured the same, or maintained, and thus could be degraded;
- They could be located anywhere in the passenger deck, including (and often) in the flight deck;
- T-PEDs could be activated, deactivated, carried on the person, stowed in luggage, or in a number of other variabilities;
- T-PEDs had less stringent standards applied than aircraft-installed equipment. This resulted in a collision between T-PEDs operating bands and aircraft radio bands.

SC-202 recognized that there was not a well-established understanding of the degree to which aircraft were tolerant of T-PEDs or the importance of each phase of operation (departure and arrival, cruise, taxi, or parked). The issue had to be quickly addressed, which induced performance of tests of the T-PEDs, analysis of the aircraft to be immune, and understanding that would be a monumental task on many aircraft, then to perform testing to determine potential issues. Front-door coupling (direct exposure to the aircraft antenna) and back-door coupling (exposure to the cabling or directly into the equipment) were addressed.

The technology of many aeronautical signals at the time was of 1940s vintage, including VOR, Glideslope, and Localizers used for landing. These did not include advanced signal processing to mitigate interference signals from PEDs or T-PEDs. Receivers that were exposed to out-of-band interference from T-PEDs could become desensitized, losing operational dynamic range. Intermodulation products, cross modulation, spurious emissions, and many other problems were considered. After four revisions were generated in four years, the 2008 edition of DO-294C, Guidance on Allowing Transmitting Portable Electronic Devices (PED) Tolerance, is 412 pages long and provides recommendations on how to deal with these issues.

Understanding this was not adequate, SC-202 also created DO-307, Aircraft Design and Certification for Portable Electronic Devices (PED) Tolerance. Work was continued by SC-234, which updated the document to

DO-307B in 2022. Along with the 2016 document DO-363, Guidance for the Development of Portable Electronic Devices (PED) Tolerance for Civil Aircraft, they provide airframe manufacturers and airlines with methods to determine safety margins and criteria for risk assessment and the ability to analyze, troubleshoot, and mitigate issues that may be found.

Much of the instrumentation testing is based on DO-160D and later. In general, to assure tolerance to T-PEDs, Category R is often the minimum level required for Section 20. Category R has two advantages. First, radiated susceptibility is stepped from 20 V/m below 400 MHz to 150 V/m above, where many of the T-PEDs transmitters operate. It also uses 0.1%-4% pulse modulation instead of squarewave amplitude modulation or 50% duty cycle pulse modulation. This short duration modulation is more in line with the type of transmissions encountered from T-PEDs. In comparison, Category W of 100 V/m starts at 100 MHz and is performed both CW and with 50% squarewave modulation. For many avionics, despite being a lower level above 400 MHz, Category W is a more difficult requirement to meet.

PRACTICAL ENGINEERING

Standards for Electricity Meters and Other Similar Devices

By Don MacArthur

Electricity meters and other similar devices have their own set of unique standards and requirements. The following describes these requirements, the challenges involved, and the status of some requirements.

ELECTRICITY METER NAMES/TYPES

Electricity meters are sometimes called AC watthour meters, demand meters, power metering and monitoring devices (PMD), power quality meters, and power quality analyzers, to name a few.

METER STANDARDS

There are both national (ANSI) and international (IEC) standards that cover the various meter names/types. Table 1 is only a partial list of meter requirements.

For meters going to Mexico, Comisión Federal de Electricidad (CFE) standard G0000-48-2010 is required for stand-alone meters. G0000-48-2010 derives its requirements from the IEC meter standards. In 2025, an entirely new standard for meters sold into Mexico will take effect. This standard is NOM-001-CRE and brings with it an entirely new set of requirements for meters and requires meters to have the capability for easy replacement via some type of extractable case.

Meters sold into Australia and New Zealand require certification by the Australian National Measurement Institute in accordance with NMI M6-1, which follows the Australian versions of the LEC meter standards.

IEC 61000-4-30, Power Quality Measurement Methods specifies two different classes of meters, Class A and Class S. Class A and Class S are determined by performing IEC 62586-2:2017, Power quality measurement in power supply systems - Part 2: Functional tests and uncertainty requirements on the meter. Class A pertains to highly accurate meters, whereas Class S is not as rigorous and is applied to less accurate meters.

IEC 61557-12, Performance measuring and monitoring devices (PMD) requires testing to IEC 61326-1 for EMC and IEC 61010-1, IEC 61010-2-030, and IEC 61010-2-201 for product safety.

ANSI Standard #	ANSI Description	IEC Standard #	IEC Description
C12.1-2022	Electric Meters - Code for Electricity Metering (Replaced C12.1-2014 & C12.20-2015)	IEC 62052-11:2020	Electricity metering equipment - General requirements, tests, and test conditions - Part 11: Metering equipment
ANSI C12.10-2011 (R2021)	Physical Aspects of Watthour Meters - Safety Standard	IEC 62053-22:2020	Electricity metering equipment - Particular requirements - Part 22: Static meters for AC active energy (classes 0,1S, 0,2S and 0,5S)
ANSI C12.18-2006 (R2016)	Protocol Specification for ANSI Type 2 Optical Port	IEC 62053-24:2020	Electricity metering equipment - Particular requirements - Part 24: Static meters for fundamental component reactive energy (classes 0,5S, 1S, 1, 2 and 3)
ANSI C12.19-2021	Utility Industry End Device Data Tables	IEC 61557-12:2018	Electrical safety in low voltage distribution systems up to 1000 V AC and 1 500 V DC - Equipment for testing, measuring, or monitoring of protective measures - Part 12: Power metering and monitoring devices (PMD)
ANSI C12.21-2006 (R2016)	Protocol Specification for Telephone Modem Communication	IEC 62052-31:2015	Electricity metering equipment (AC) - General requirements, tests, and test conditions - Part 31: Product safety requirements and tests
ANSI C12.22-2012 (R2020)	Protocol Specification for Interfacing to Data Communication Networks	IEC 61000-4-30:2015 +AMD1:2021	Electromagnetic compatibility (EMC) - Part 4-30: Testing and measurement techniques - Power quality measurement methods

Table 1

ANSI standards are applied to devices sold into the United States, Canada, and some Latin American countries. Entities such as the New York State Department of Public Service Commission require all meters used at their facilities to comply with ANSI standards.

Many of the ANSI meters standards are currently under revision, new standards are in progress, and a few are slated for replacement by newer versions.

- ANSI C12.31-202x establishes standard definitions of AC electrical power (active, reactive, and apparent), AC electrical energy (active, reactive, and apparent), and power factor in terms of sampled voltage and current measurements.
- ANSI C12.32-202x (2nd Edition) covers DC Metering.
- ANSI C12.46-20xx, based on OIML R46:2012 and many IEC standards, is a performance standard for the measurement of active, apparent, and reactive energy that is intended to replace ANSI C12.1.

Image by Pixelharvester from Pixabay

- A new ANSI demand metering standard is also in the work, the number of which has yet to be defined.

The chart in Figure 1 indicates the latest timeline for the release of new ANSI meter standards.

CHALLENGES OF MEETING METER STANDARDS

- ANSI C12.1 requires that voltage and current inputs to the meter pass a surge test of 6 kV and a 2 Ohm source impedance. This is a much tougher test than what is required by IEC standards.
- ANSI C12.1 requires the meter to pass Class B emissions.
- ANSI and IEC standards are not yet fully aligned, and keeping track of the differences is burdensome.
- ANSI standards are currently in a state of change, and the update process is lengthy.
- Depending on the requirement, meters must maintain accuracy during and after they are subjected to EMC immunity and other environmental influence quantities.

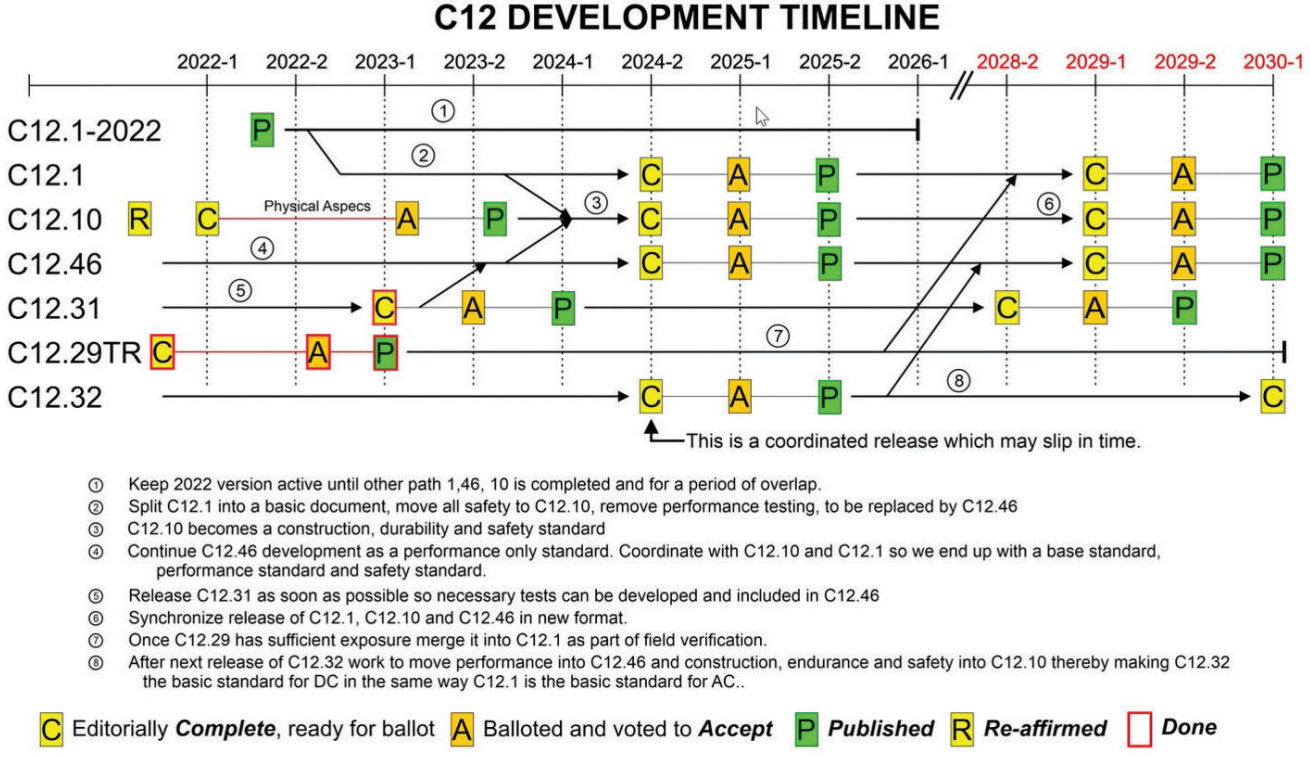


Figure 1

TACKLING LOW-VOLTAGE SIGNALING IN INVERTER DESIGN: PART 1

Managing High-Power Inverter Noise to Protect Low-Voltage Signals

Christopher Semanson is a System and Solution Engineer at Renasas Electronics America, Inc. in Durham, NC, supporting a wide variety of general-purpose applications dealing with microcontroller unit (MCU), memory protection unit (MPU), and electrical system design. He has previous experience in EMC Education at the University of Michigan, teaching EMC and Electronics with Mark Steffka and in Software Systems and John Deere and Ford Motor Company. Semanson has a bachelor's degree in electrical and computer engineering and a master's degree in electrical engineering from the University of Michigan Dearborn. He can be reached at chris.semanson@renesas.com.

By Christopher James Semanson

Not long ago, the electrification of consumer machinery was primarily limited to hybrid electric vehicles (HEVs), marketed as the next generation of clean propulsion but largely out of reach for the average consumer. Now, with the advent of affordable, high-end microcontroller units (MCUs) and high-efficiency semiconductors, the adaptation of motor control has become more accessible, expanding electrification into secondary markets such as turf care and agricultural equipment, in addition to a growing HEV market. This shift means that embedded system or module development engineers are encountering new challenges associated with electric drives.

Central to these advanced systems are the power electronic components that constitute the inverter system. These components are responsible for converting DC voltage from a generator or battery into an appropriate signal to drive a three-phase motor. Designing and interfacing with the control electronics of inverters present unique challenges, particularly in managing signal integrity and mitigating noise. To illustrate these complexities, a typical inverter system is depicted in Figure 1.

A significant challenge in designing and interfacing with electric drives is managing signaling levels and their susceptibility to conducted electrical noise from the inverter's output stage. However, with inverters switching hundreds of amps, the quest for high efficiency, module designers have optimized for minimal dead times, high drive strength, and fast edge rate; all of which come at the expense of electrical noise. These modules typically operate across a wide range of voltages, from 50V to several hundred volts, and at varying power levels tailored to specific applications. However, the signaling voltage levels, constrained by the process technology, generally range from 1.8V to 5.0V.

Balancing the need for the highest efficiency with typical voltage input output (V_{IO}) levels and ensuring that the controller can accurately manage the drive becomes a primary challenge for both embedded and analog engineers.

To better understand the challenges involved in designing, building, and debugging a high-power mixed-signal inverter, Part 1 of this two-part article will provide an in-depth discussion of the components and functions of an inverter. This includes examining

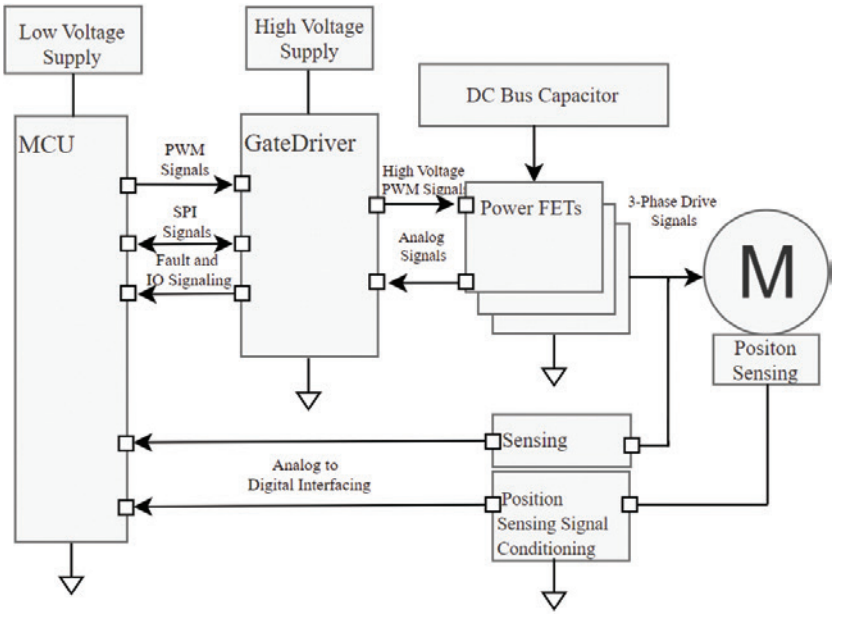


Figure 1: Example diagram of a typical inverter system

common application-specific integrated circuits (ASICs) that work alongside field effect transistors (FETs) and MCUs, focusing on their roles in interfacing and driving. We'll also address common functions such as communication and GPIO (general purpose input output) usage.

IDENTIFYING COMMON LOW VOLTAGE SIGNALING INTERFACES

Interfacing between the MCU and external ASIC circuitry as sensitive traces is the first step in mitigating noise since each interface plays a specific role in the command and control of the module at the application layer. To better understand their functions and potential failure modes, the low voltage interfacing is categorized into the following groups of GPIO:

- *Inter-integrated circuit communication interface (I^2C)/serial peripheral interface (SPI) communication lines*—These are the most common types of communication interfaces, especially for advanced ASICs such as smart gate drive devices and external monitor circuitry. I^2C operates with an open-drain configuration, while SPI uses a push-pull mechanism.
- *Low voltage drive signals*—These signals are used for the command and control of drivers, typically driven by a timer circuit. They generally interface with a level shifter or gate driver that controls the motor.
- *Critical GPIO signals*—These include fault processing signals used to quickly disable the drive, reset pins to alert the MCU of issues in the drive circuitry, and control pins for the ASIC's functionality. Although less common, these signals are needed to obtain real time operational fault and drive status while under operation.

In any of the above scenarios, incorrect signal detection due to coupled noise from the power FETs can lead to challenges specific to that signal's function. What makes these signals sensitive is the small signal-to-noise ratio they have, inherent in many ASICs and MCU interfacing structures. This vulnerability arises because ASICs tend to operate with low IO voltage (V_{IO}), typically on a CMOS level from either:

- *External V_{IO}*—Interfaces with the MCU, allowing the ASIC to signal at voltages as low as 1.8 V; or
- *Internal V_{IO}*—Logic levels designed around a 3.3V internal reference, a typical CMOS signaling level.

The *noise* generated by high-power switching transients is often comparable to these low signal levels. A transient that crosses the threshold for a long enough time (i.e., exceeds a deglitch time, or T_d) to trigger a logic switch results in incorrect actuation. To better understand how high levels of transients can affect IO signaling, it is essential to refer to the datasheet where the input high (V_{IH}) and low (V_{IL}) levels are defined.

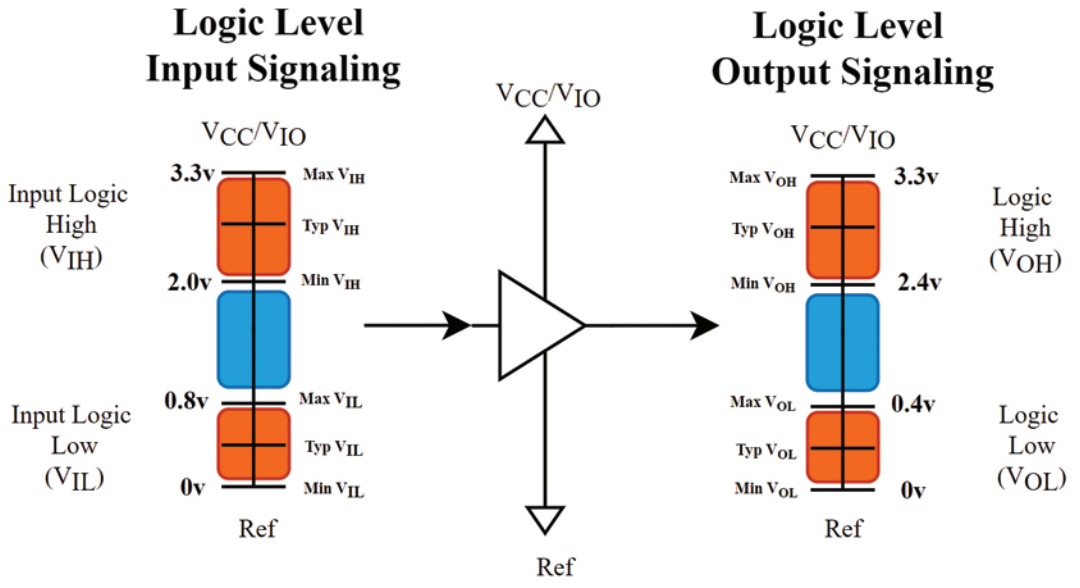


Figure 2: V_{IH}/V_{IL} signaling levels for an input buffer

EXAMINING V_{IH}, V_{IL} FROM THE DATASHEET

When designing a signaling interface to an ASIC, engineers should first consult the datasheet for minimum, typical, and maximum values. These datasheet values are tested at manufacturing, and the ASIC manufacturer strives to not ship pieces that operate beyond these limits. The values define your operating parameters and edge cases where you want to stay away from:

- V_{IH}—The voltage at which the input triggers a low-to-high transition;
- V_{IL}—The voltage at which the input triggers a high-to-low transition; and
- *Minimum pulse width, debounce, or deglitch time*—The minimum time a signal must persist above or below the voltage thresholds for a logic level threshold change.

Figure 2 illustrates typical 3.3v CMOS TTL gate-level input and output signaling.

To assess how these logic levels impact noise tolerance, we must first investigate the structure of an input buffer representative of a standard CMOS input to an ASIC.

The model shown in Figure 3 depicts an input logic circuit referenced to a V_{IO}, primarily at DC. At the top of the input, we generally find V_{IO} or a reference voltage, either externally fed or internally generated. The key voltage levels are when the inverter circuit recognizes a logic high, with added hysteresis, and when it recognizes a logic low, again with hysteresis. When transient characteristics are introduced, trace parasitic can significantly impact circuit performance during coupled switching transients on the reference, power, or input lines.

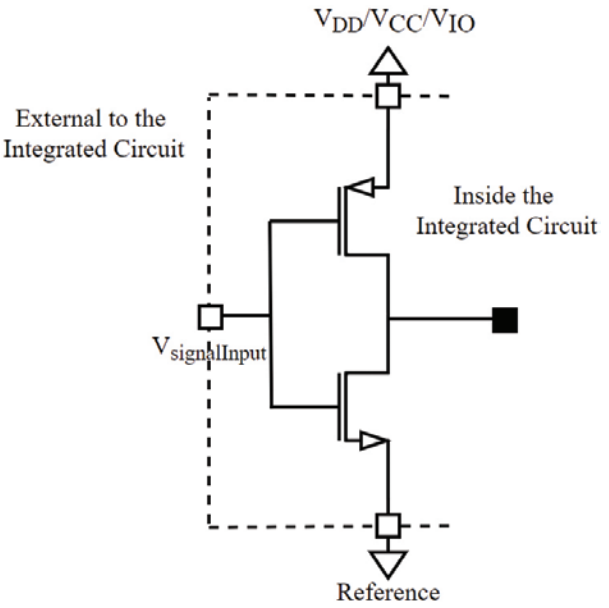


Figure 3: Example of a buffer circuit inside the ASIC

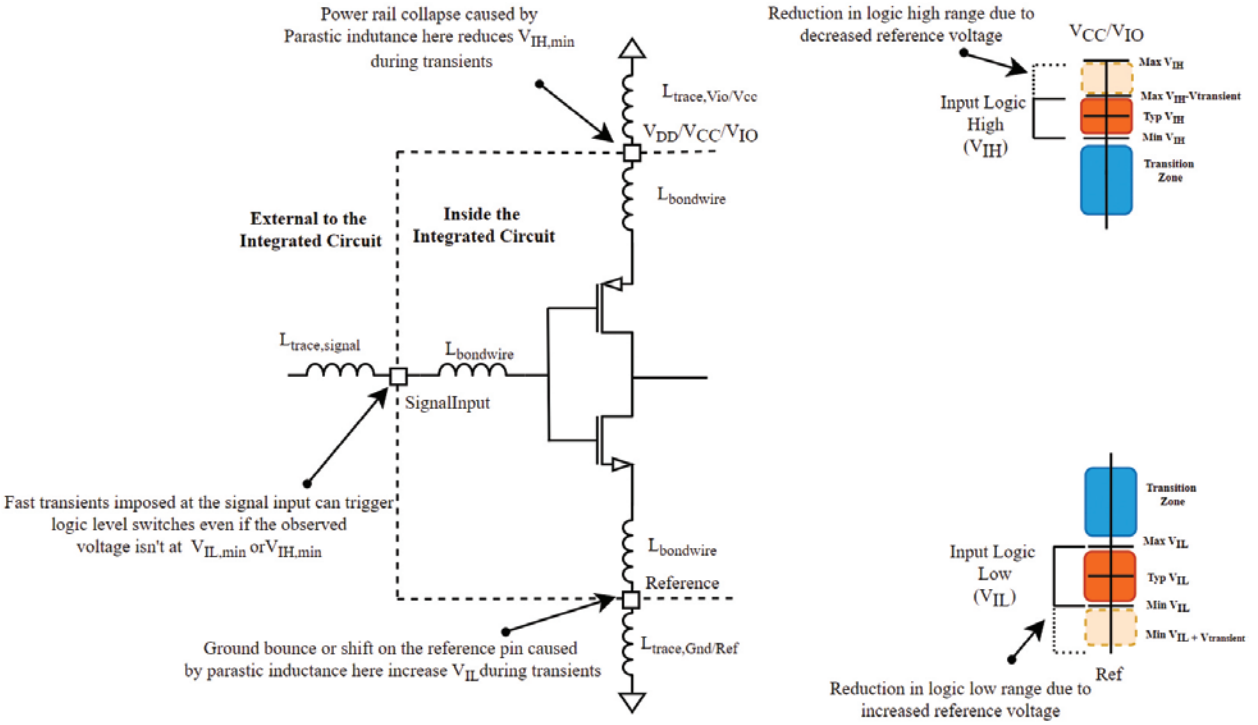


Figure 4: The previous circuit structure with labeled parasitic and its impact on V_{IH} and V_{IL} levels

Additionally, the voltage levels defined in datasheets are typically guaranteed at DC, determined by slowly ramping a voltage signal up and down to obtain minimum, typical, and maximum values. If we apply a switching transient coupled onto either the inverter input, power, or ground, ringing can:

- Collapse the power supply momentarily reducing your V_{IH} levels;
- Bounce the reference (or ground) momentarily impacting V_{IL} levels;

  or

- Couple onto your input signal, causing an incorrect V_{IH} to be detected, or even worse, cause overshoot that the typical oscilloscope is not able to detect.

The impact of the transient's scale with the speed and power of the switching signal. So the faster the transient, the more impact in terms of coupling, reference bounce, or power rail collapse.

After understanding how reducing V_{CC} or increasing the reference to your circuit can impact V_{IH} and V_{IL} values, the discussion can shift to how this noise impacts gate drive, I²C/SPI, and other GPIO signals that operate at CMOS levels.

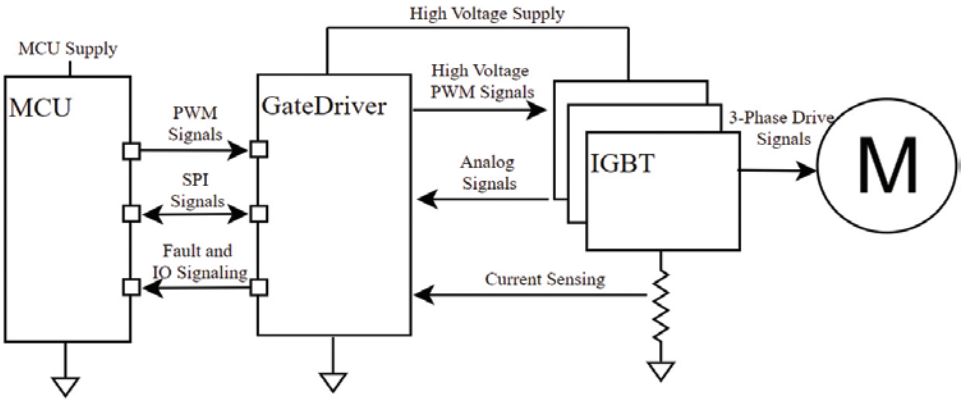


Figure 5: A simplified inverter system with gate drive

IMPACT OF NOISE ON GATE DRIVE ASICS

The control strategy behind an inverter and how it creates AC power from DC is complex enough to fill a book. However, at its most basic level, the motor is controlled by filtering tightly controlled pulses through motor windings to create AC currents. Since the MCU isn't capable of driving the output switches directly, a level shifter or a more commonly found gate drive ASIC is used (often labeled a "Smart" Gate Driver). A simplified diagram is depicted in Figure 5.

Applications that rely on gate drive ASIC performance generally employ features such as:

- *Monitoring the voltage and currents across the FETs*—Ensuring that parameters are within safe operating ranges and provides protection when they're not.
- *Automatic deadtime insertion*—Preventing shoot-through by inserting a delay between turning off one transistor and turning on the complementary transistor.
- *PWM mode selection*—Allowing the selection between 3 PWM (where opposite side drives are complementary, controlled by the gate driver circuit with trimmable deadtime insertion) or 6 PWM mode (where all low side PWM drive pulses are controlled by the MCU).

Despite the advanced functionality of the gate drive ASIC, it ultimately reacts to the low voltage side inputs. This means that if transient spikes on the input persist above the V_{IH} for longer than T_d, it will pass that pulse through to the high side of the gate driver. As a result, noise coupled onto the low voltage side of the device can manifest itself in several ways depending on how and where the noise is imposed onto the device IO.

If the noise voltage couples onto the low side PWM signals, it runs the risk of actuating the high side and low side at the same time. This could result in shoot through or shoot through protection, which occurs when both transistors conduct simultaneously, resulting in a temporary short circuit.

Gate drivers often include protection logic to prevent this, along with modification of deadtime to better control switching performance. The high-side and low-side gate pulses control the switching of

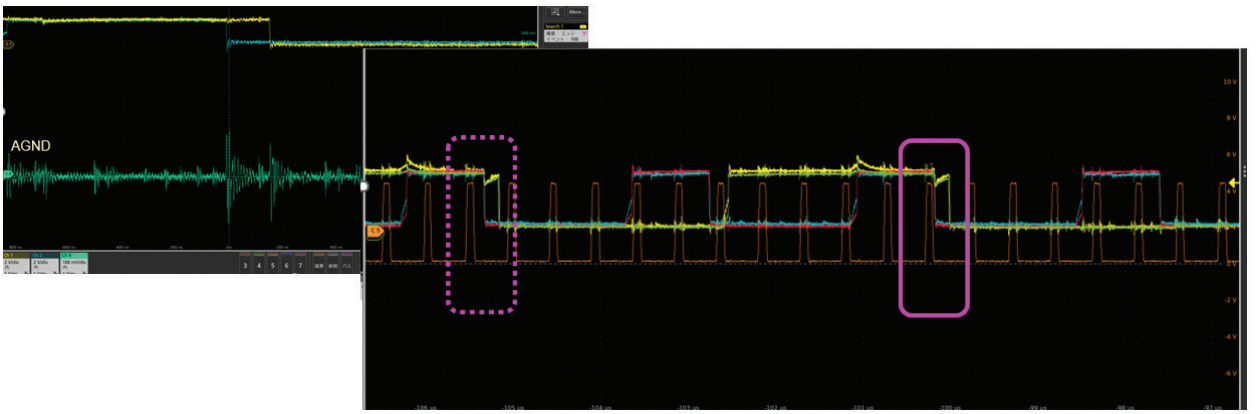


Figure 6: (Left) Noise on the AGND reference net that should be 0v, (Right) gate pulses, the cause of the reference noise

transistors that drive the e-machine and are generally complimentary to each other in 3-pwm mode, and in 6-pwm mode they are driven complimentary. Gate drive ASICs have functions and characteristics that manage these by automatically protecting the switches from short circuiting as well as automatic dead time insertion, along with calibratable drive strength.

The most common type of shoot through protection that ASICs employ is automatic early pulse termination. This, erroneously, happens either:

- When bounce on the reference plane from opposite side switching pulse either lifts the reference high enough to trigger the opposite side, or creates a noise voltage spike, causing an early termination of the driving pulse; or
- When a voltage transient larger than the VIH threshold is detected at the input of the low voltage side. These transients are generally very difficult to measure accurately due to the parasitic of the probe and probe clip being able to be easily loaded. As such, they are generally estimated from a measurement of the ground or by overlaying a switching pulse.

Examples of a reference bouncing are shown in Figure 6.

In both pictures, the magnitude of the noise on the "AGND" net causes the reference to move, caused by the orange PWM signals on the picture to the right. When lined up properly, as outlined in the solid pink box, this can cause incorrect actuation of the neighboring low voltage signal in either incorrect triggering or a missed trigger.

This interaction leads to the diagram below depicting early pulse termination and its impact on the high voltage drive pulse. As the diagram in Figure 7 shows, the moment the noise voltage crosses the V_{IH} threshold, the pulse is terminated, deadtime is inserted, and the pulse is driven low, only to be driven

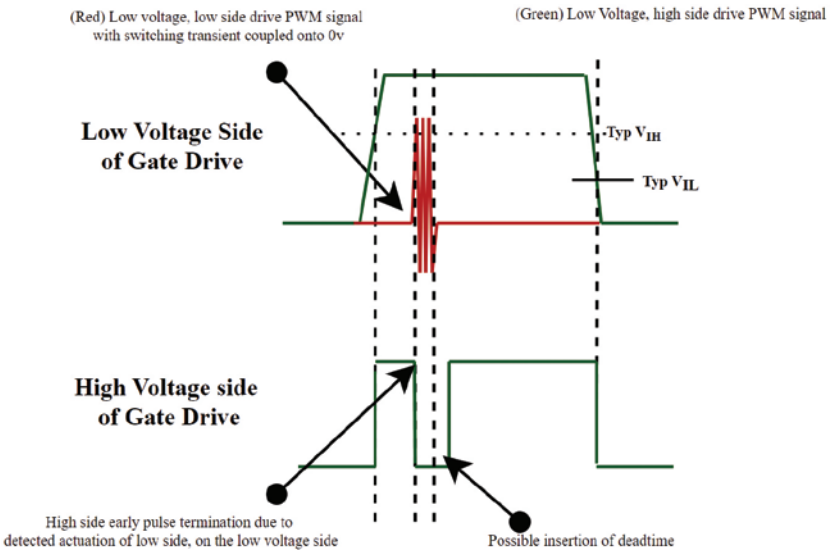


Figure 7: Example of early pulse termination due to the gate driver trying to prevent simultaneous high/low side actuation

high again when the transient event is over, causing erratic motor operation.

In the event the gate driver ASIC does not have active protection, designers generally rely on complimentary parts of a circuit to drive the output in 3-pwm mode, where the low side turns on when the high side turns off. However, the issue still remains and is compounded because, while the pulses are complimentary of each other, they are still subject to trace capacitance, which can impact the propagation delay of the complimentary signal, which could cause accidental shoot through.

Next, we'll focus on the impact of noise on I²C and SPI communication buses.

IMPACT OF NOISE ON COMMON COMMUNICATION INTERFACES

While incorrect actuation on IO and drive signals is relatively easy to visualize, their impact on standard communication interfaces like I²C and SPI is more subtle and can create difficult-to-debug challenges. To better identify these issues, let's briefly overview the interfaces:

- *I²C*—I²C is a common hardware interface and protocol used to facilitate communication between ASICs and a controller MCU. The hardware is designed as an open-drain, pulldown circuit, which requires pullup resistors to the IO voltage level. Its idle state is typically pulled high, and it counts nine clock edges per 8 bits of data transferred. I²C uses two wires: a clock line and a data line, connecting the controller to its peripherals.
- *SPI*— SPI is a common hardware-defined interface that functions as a shift register between the controller and peripherals. The hardware operates much faster than I²C, as it is a driven interface (commonly referred to as push-pull). SPI typically uses four wires: clock, data in, data out, and chip select.

The digital block in both of these communication interfaces typically features a state machine that counts edges when they receive the signal to begin a frame. The clock is specifically controlled by the controller in typical situations. If incorrect actuation occurs due to a high-power transient coupling onto

either the clock or data lines, we risk encountering the following challenges:

- *Data corruption:* When pulses on the data line aren't read properly by the controller, data validation can be performed via CRC. If the CRC does not match, the frame is dropped. This method applies to both I²C and SPI.
- *Clock corruption:* Clock corruption is more nuanced and depends on which part of the communication interface is impacted.
- *Near-end crosstalk:* Noise coupled onto the clock signal near the controller can cause the controller to count extra clock pulses. This could lead to early termination or releasing of the bus while the peripheral device is still transmitting, leading to a stuck bus condition.
- *Far-end crosstalk:* Noise coupled onto the clock signal near the peripheral device can cause the peripheral to count extra clock pulses. This could result in incorrect data being sent, or an error in communication between the peripheral and controller devices.

In all of these situations, the impact is again difficult to measure due to probe parasitic. In Figure 8, we can see what appears to be a good I²C transaction, but the result is a stuck bus line.

This situation resulted in the controller or peripheral clock counters becoming out of sync, incorrectly missing a clock pulse, even though an oscilloscope demonstrates otherwise. On a communication bus, this desynchronization can lead to a bus-stuck condition, where a device holds down either the clock or data, waiting for extra edges that will never come. Each situation requires software intervention to recognize the issue and release the bus.

Additionally, because each interface is controlled in a different circuit manner, they're impacted differently. Since I²C is an open-drain interface, it is primarily impacted by reference bounce and *pullup strength*, especially during transitions. The pulldown is expected to be referenced to the same 0 V at both the near and far ends.

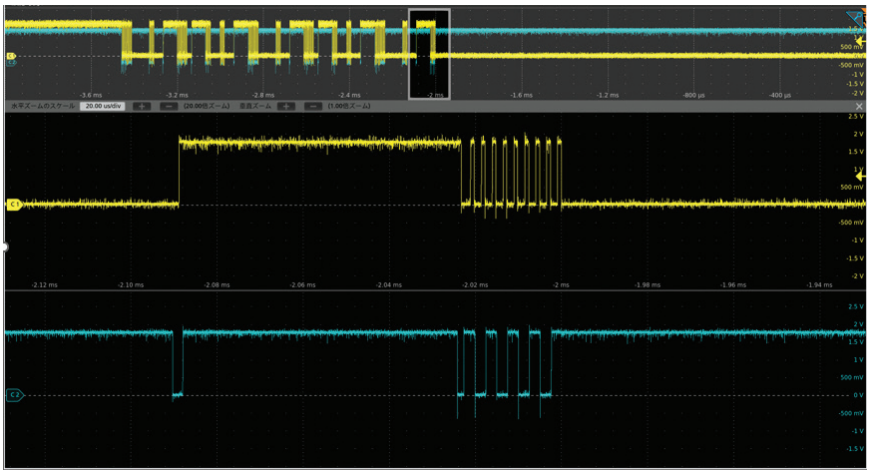


Figure 8: Example of an oscilloscope detected a proper I²C transaction, but the bus is held due to the ASIC not detecting the pulsetrying to prevent simultaneous high/low side actuation

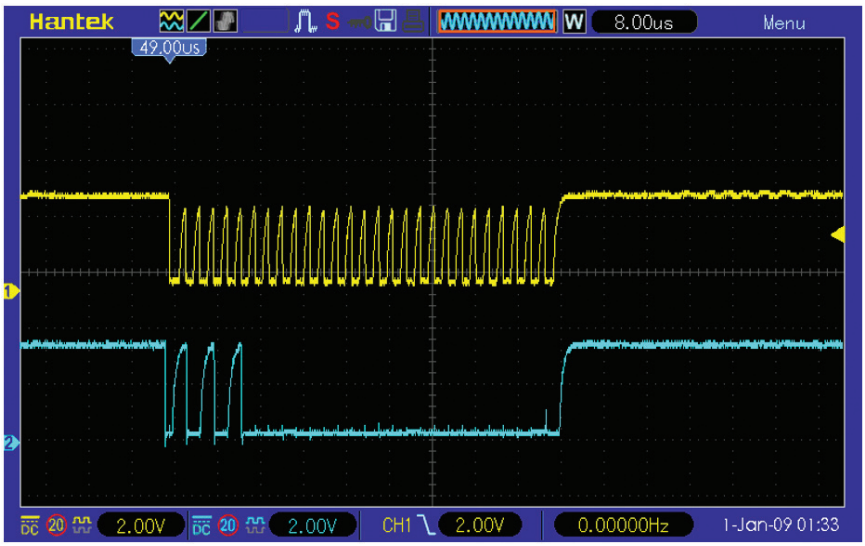


Figure 9: Example of a I²C transaction with a very weak pullup, clock glitching, and narrow duty cycle still being detected properlytransaction, but the bus is held due to the ASIC not detecting the pulsetrying to prevent simultaneous high/low side actuation

And while I²C is tolerant to a wide variety of pullup and duty cycle conditions, as shown in Figure 9, it is important to choose the right operating conditions.

As SPI is a push-pull interface, its impact is limited to glitches on either the clock or data lines during transmission, and typical errors here are in extra clock pulses inserted on the SCK (resulting in a stuck bus) or extra data pulses on either the serial out or serial in data lines (resulting in a corrupted packet).

While coupled transients can significantly affect GPIO drive signals and the communication interface to typical ASICs, we can now explore techniques and complementary circuits that can be implemented to mitigate these issues. In many situations, conducted electrical noise is inherent to the design of high-power inverter systems. Mitigation strategies can be divided into two main categories:

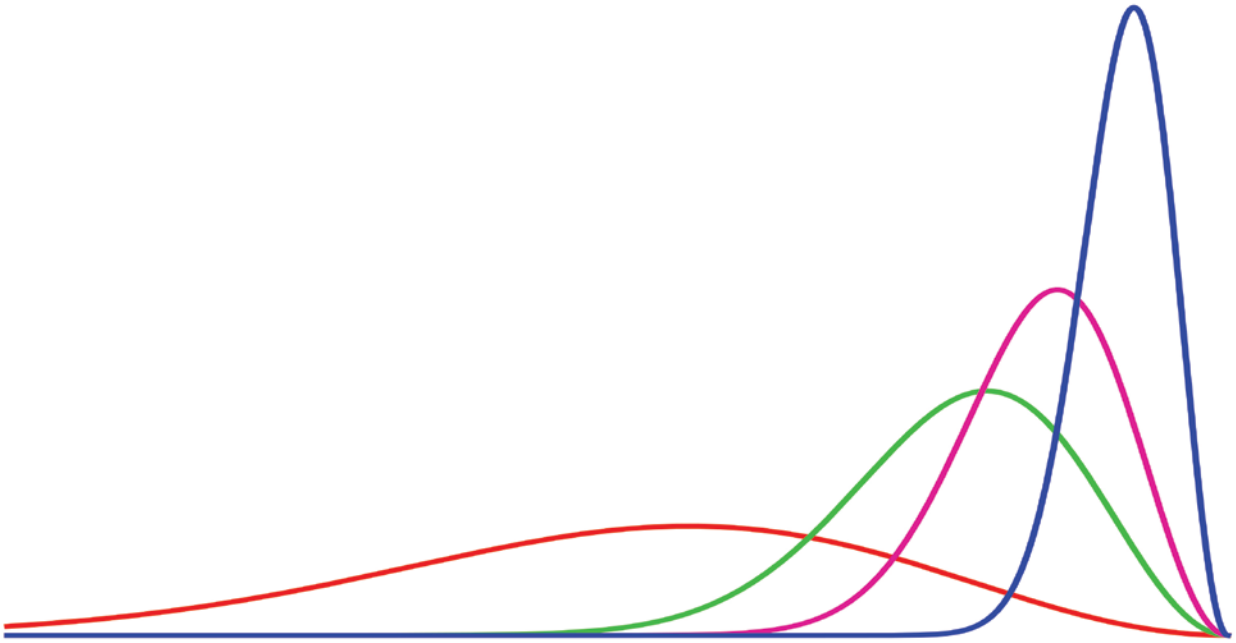
- Components used for impacting the sharp edges that are the source of electromagnetic interference; and
- Layout and planning to ensure that the system has the best chance of avoiding issues by placing connectors and creating a stack up that shield low voltage circuitry.

CONCLUSION

With the push across various industries to hybridize machines that would otherwise be pneumatic or hydraulically driven, inverters are becoming prolific. The design challenges that come along with these inverters are often centered around the balancing of being robust to high voltage transients on low voltage signaling and switching efficiency in order to get the most out of the inverter. In Part 2 of this article, we'll discuss the importance of choosing the correct PCB stack up during component selection and placement, including placeholders for components that otherwise can be unpopulated.

CURRENT PROBE SPECIFICATIONS AND THEIR IMPACT ON CONDUCTED EMISSIONS MEASUREMENTS

Addressing the Limits of CISPR 25 Measurement Methods



Current probes are used to perform conducted emission (CE) measurements in accordance with various product standards like CISPR 11, CISPR 25, or CISPR 32. All these product standards refer to the basic standard CISPR 16-1-2 (2014), which includes normative specifications for current probes in clause 5.1.3. Some of the current specifications include:

- *Insertion impedance:* 1 Ω impedance maximum;
- *Transfer impedance:* 0.1 Ω to 5 Ω in the flat linear range; 0.001 Ω to 0.1 Ω below the flat linear range (current probe terminated into 50 Ω load);
- *Added shunt capacitance:* less than 25 pF between the current probe housing and measured conductor; and
- *Frequency response:* Transfer impedance is measured over a specified frequency range to calibrate the probe; the range of individual probes is typically 10 kHz to 100 MHz, 100 MHz to 300 MHz, and 200 MHz to 1,000 MHz.

In the recent past, questions have been raised about the usefulness and appropriateness of these specifications and how commercially available and widely used current probes meet these specifications over required frequency ranges. These concerns have been formally documented, for example, in a document issued in April 2023 by CISPR/D, the subcommittee responsible for CISPR 25.

Furthermore, work related to the definition and measurement methods for the specification “insertion

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By Bruce Harlacher and Werner Schaefer

impedance" was initiated by CISPR/A/WG1 in 2017 to address the current lack of a standardized measurement method.

This article will discuss the following aspects related to the above CISPR 16-1-2 requirements, including:

- The appropriateness of the 1 Ω Insertion Impedance specification in the context of its impact on both the calibration process and for measurements using a simple CE test configuration, per CISPR 25 (see Reference 1);
- Meaning and usefulness of the shunt capacitance specification; and
- Practical purpose and usefulness of various inferred "limits" for current probe transfer impedance versus frequency, as documented in Reference 5.

CURRENT SITUATION

The CISPR 16-1-2 requirements cited in the introduction were originally included in CISPR 16-1 before 1999 and were transferred to CISPR 16-1-2 with no changes since then. No information is available in the CISPR 16 set of documents (e.g., CISPR 16-3) regarding the assumptions made for establishing current specifications as far as their values and associated frequency ranges are concerned. However, since these specifications are placed in the normative part of the standard, they are to be interpreted as normative requirements that current probes must meet in order to be used in measurements in accordance with product standards (e.g., CISPR 25).

The situation is compounded by the fact that for some specifications no definition for "insertion impedance" exists, and no agreed-on measurement methods are made available to determine the values of specifications like insertion impedance or "shunt capacitance."

Additionally, there is a misalignment between CISPR 16-2-1 and product standards regarding the frequency range for specifications. Most product standards use the current probe in the frequency range of 150 kHz to 30 MHz for conducted emission measurements, with the exception of CISPR 25, which calls out a maximum frequency of 245 MHz for current probe measurements. CISPR 16-1-2, on the other hand, defines several frequency ranges for the specification of frequency response, up to 1 GHz.

This situation has created considerable confusion among users as to how rigorously to apply the current probe requirements in CISPR 16-1-2 when purchasing current probes or calibration services for current probes. Some concerns were formally raised by some CISPR product committees like CISPR/D and CISPR/A that started the process to formally address these concerns. Several aspects are currently under discussion and the three topics previously outlined do serve as input to the resolution of currently existing problems related to current probe specifications.

INSERTION IMPEDANCE MEASUREMENT DISCUSSION

In CISPR/A, three different methods to measure the insertion impedance of current probes were proposed in 2018. However, these methods only cover the frequency range of up to 30 MHz, which excludes a large portion of the frequency range stipulated by CISPR 25 (up to 245 MHz). The rationale for the limitation of the frequency range to 30 MHz was given as the requirement for the calibration fixture dimensions needing to be small compared to the wavelength. This explanation is not obvious since the wavelength at 30 MHz is 10 m, and all calibration fixtures have dimensions that are more than an order of magnitude smaller for the current probes used for conducted emission measurements in accordance with CISPR product standards.

The three proposed measurement methods introduced by CISPR/A Working Group 1 are addressed in the following sections.

One-Port Reflection Method

The measurement setup for this method is shown in Figure 1.

While the suggested principle is plausible, it is unclear why the output of the fixture is terminated in a short and not in 50 Ω. In case of a short, the network analyzer measures a very high reflection in case of an empty fixture and with the probe placed inside the fixture. It seems preferable to measure close to the system impedance of 50 Ω since the uncertainty contribution of the network analyzer is minimized in this scenario, which improves the uncertainty of the insertion impedance measurement.

Series-Thru Method

The measurement setup for this method is shown in Figure 2.

This method seems to be more beneficial compared to the one-port reflection method since the system impedance of 50 Ω is maintained throughout the measurement process.

Shunt-Thru Method

The measurement setup for this method, as described in Reference 3, is shown in Figure 3.

In the description previously provided, it was unclear where the full two-port calibration of the network analyzer is performed. Is the reference plane for the measurement established at the end of the cables without considering the T-connector, or is the T-connector somehow included in the network analyzer calibration process? It seems that this method yields a larger measurement uncertainty since the T-connector can cause coupling of the source signal (Port 1) directly to the measurement channel (Port 2), and the reflected signal from the short termination can reflect back into the source channel. As stated in the document, the influence of the calibration fixture on measurement results was unknown, which seems problematic since no details of the fixture were provided in the contribution.

Further work in CISPR/A Working Group 1, completed in 2021, expands on the initial work regarding measurement methods for insertion impedance. The originally proposed measurement methods were repeated, using a calibration fixture

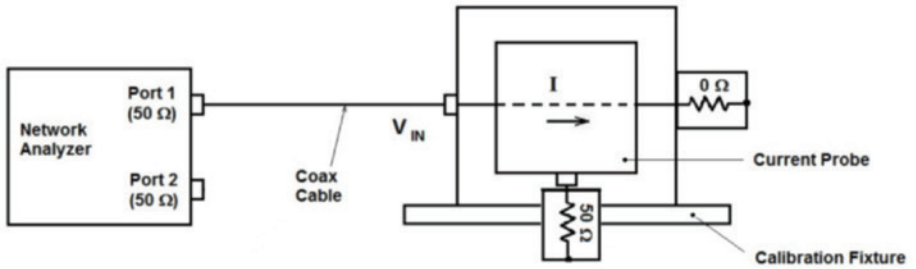

Figure 1: One-port reflection method

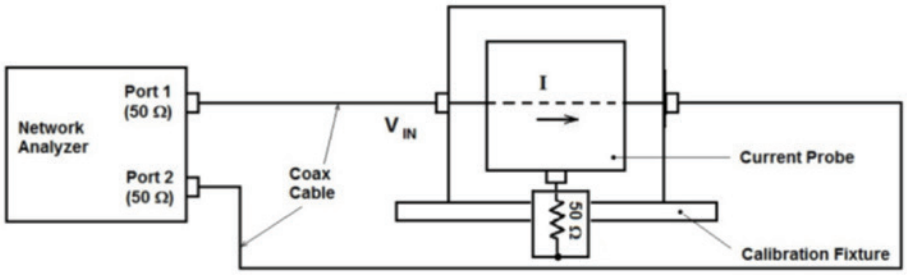

Figure 2: Series-Thru method

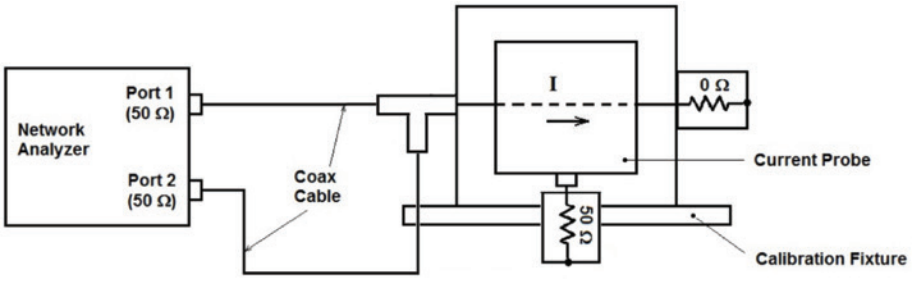

Figure 3: Shunt-Thru method

suggested by the current probe manufacturer for the probe under investigation. Based on the calculated measurement uncertainty associated with each method, the "shunt-thru method," using a transmission measurement, was identified as the most accurate method to determine insertion impedance. It is to be noted that the measurement uncertainty was only based on the contribution of the network analyzer, not considering possible fixture influences. It would be beneficial to investigate the influences by using different fixtures to be able to determine the impact on the insertion impedance measurements.

While the "shunt-thru method" to 30 MHz looks like the most promising method from a consistency and uncertainty standpoint, the results, presented up to 100 MHz, indicate two things of interest:

- First, the measured insertion impedance is about 3 Ω and rises with increasing frequency, which does not comply with the current specification; and
- Second, the measured insertion impedance appears to begin diverging between S_{11},$_{22}$ and S_{21},$_{12}$ at 30 MHz. This appears to illustrate the difficulty that will be encountered at frequencies above 100 MHz and most certainly at 1 GHz. The divergence shown in the resultant plot infers a fundamental problem in defining the "proper" method, particularly in light of the maximum test frequency range used by CISPR 25.

In CISPR/A, further work was completed in the form of a round-robin test (RRT) to determine the suitability of the "shunt-thru" method based on transmission measurements to 100 MHz to determine the insertion impedance of a current probe. That effort produced the following observations:

- A variety of calibration fixtures were used by participants of the RRT. Only one participant used the calibration fixture suggested by the manufacturer of the current probe.
- On the one hand, this would seem to violate a round-robin concept of all participants using the same hardware (not considering the probe electronics) to isolate differences in how various laboratories execute a given test method. On the other hand, it points out the importance of using a proper test fixture (recommended by the probe manufacturer).

The RRT summary report acknowledges the fixture issue as the "dominating influence above 600 kHz" and reinforces the notion that the use of the proper calibration fixture is crucial. Furthermore, one conclusion drawn in this paper states that "the measurement method is effective to measure Insertion Impedance of current probes." It is unclear how this general conclusion can be drawn since the measurements were made only up to 100 MHz, not covering the full frequency range to 245 MHz in CISPR 25. In addition, as stated before, the fixture has a significant impact. Therefore, the suitability of the method is dependent on the use of a "proper" fixture.

INSERTION IMPEDANCE MEASUREMENT METHOD

Our co-author Bruce's company (Fischer Custom Communications) developed the insertion impedance measurement method prior to CISPR/A's work referenced in this article to better understand insertion impedance. This effort was driven by increasing customer queries involved with measurements in accordance with CISPR 25. The selected insertion impedance measurement approach is very similar to existing calibration protocols and is based on the idea of working in a 50 Ω system.

Since the insertion impedance discussion tends to be more focused on the calibration aspect, our technical experts elected to focus initially on the calibration perspective, which is discussed later in this article.

Figure 4 shows the basic test setup we used for our insertion impedance investigations, which includes the following steps:

1. An S_{11} calibration was performed with short, open load at the end of the measurement cable with the network analyzer configured to measure impedance Z based on $S_{11;}$
2. The current probe was removed from the calibration fixture;
3. A network analyzer sweep was performed and saved;
4. The current probe was installed in the calibration, and another network analyzer sweep was performed and saved; and
5. The difference between the two network analyzer sweeps was calculated as the measured insertion impedance.

Early in our research of insertion impedance measurement methods, we recognized the potential for the current probe case to be an influence at higher frequencies. Although not extensively researched, it appeared that the probe case effect was not routinely addressed in the literature. CISPR 16-1-2 specifications treat the case impact as a limit: "Added shunt capacitance less than 25 pF between the current probe housing and measured conductor." Currently, there is no guidance in the CISPR documentation on how to measure shunt capacitance, nor is it clear if this requirement applies to an actual measurement application, a calibration scenario, or both.

References 3 and 4 seem to be typical attempts to model current probes. The primary focus is on the equivalent electrical circuit comprised of the electronics of a current probe. The probe case is not included in the modeling. The previously described measurement treated the probe electronics and its case as an integrated item. With the probe case being a major point of interest, we performed a variety of insertion impedance measurements with and without the use of an empty probe case in an attempt to remove the case influence on the measured insertion impedance.

Both types of insertion impedance measurements were made on two different probes. The first is a widely used current probe that has a nominal transfer impedance of about +13 dB ohms from about 5 MHz to 400 MHz. The second probe was one that has a nominal transfer impedance > =20 dBΩ from about 50 MHz to 1000 MHz.

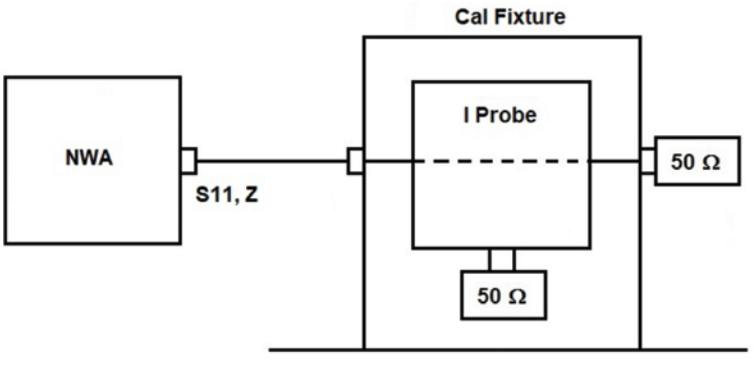

Figure 4: Insertion impedance method

Many of the experiments we performed measuring insertion impedance with and without case effect removal indicated a complex interaction, likely involving inherent transfer impedance, size of probe case, and maximum frequency of interest.

The results are presented in Figure 5 for both probes and both types of insertion impedance methods previously discussed.

Many of the experiments we performed measuring insertion impedance with and without case effect removal indicated a complex interaction, likely involving:

- Inherent transfer impedance;
- Size of probe case; and
- Maximum frequency of interest.

These factors seem to add to the difficulty of identifying the "proper" insertion impedance test method.

POSSIBLE IMPACT OF INSERTION IMPEDANCE IN A TEST SETUP

The inference of the CISPR 16-1-2 requirement that insertion impedance by less than 1 Ω at all frequencies (possibly to 1 GHz) is that any value above 1 Ω might adversely affect the actual conducted emission (CE) measurements. The origin and basis for this requirement is unknown but would seem to be extremely conservative from an application standpoint.

From Figure 13 in CISPR 25 (2021), it is apparent that a loop is formed by the equipment under test (EUT), the load simulator, the interconnecting wire, and the ground plane. It is not clear if the two artificial networks and the DC power supply are part of this loop or if the load simulator provides some electrical isolation between the EUT and power and artificial networks.

Reference 5 investigates the "influence of termination impedance on conducted emissions in automotive high voltage networks." In this document, the authors started with an equivalent circuit that consisted of a loop formed by the DC power (+) side, through a line impedance stabilization network (LISN), through the EUT, and then back to the DC power (-) side after passing through a second LISN.

Both of these examples point to the use of an electrical loop as a starting point to look at loop impedance versus frequency and how the potential addition to this loop impedance through the presence of a current probe might be important.

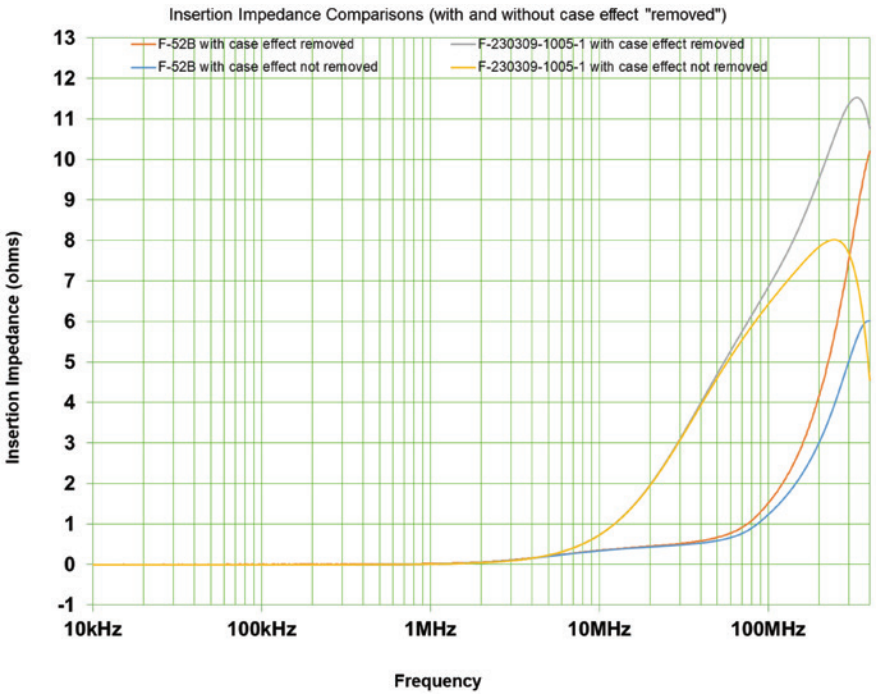

Figure 5: Comparison of insertion impedance measurements on two different probes with and without "removal" of probe case effect

An investigation was started by combining the two concepts into the configuration shown in Figure 6.

This figure includes the following elements:

- A DC power source assumed to have some inherent source impedance/resistance
- An optional LISN on the (+) side
- A cable harness over a reference ground plane, as per CISPR 25, specified as follows:
  - The length of harness set at 1700 mm as per CISPR 25;
  - The height of harness above ground plane set at 50 mm as per CISPR 25;
  - The harness outer diameter is a variable depending on DC current flowing through harness;
  - The harness suspended above ground plane with a dielectric material having a relative permittivity <= 1.4, as per CISPR 25; and
  - Harness introduces a series inductance to the loop impedance.
- A load impedance is assumed to be set by the operating current in the harness and DC power source voltage
- A series impedance introduced by the current monitor probe
- Shunt capacitance
- CISPR 16-1-2 states that the probe case to wire under test is to be considered. However, it is unclear if the assumption is that this capacitance somehow compromises the measuring ability of the probe (i.e., affecting its transfer impedance) or if this requirement infers that this capacitance is then coupled to reference ground. Figure 6 shows both types of capacitances.

A reasonable starting point would be to identify a configuration that has a relatively low loop impedance, where the potential impact of the added series impedance of the current probe would presumably have the maximum (worst) impact. This points to an operational configuration where a high DC current is used. Since the LISN can only add to the series loop impedance, deleting the LISN would also contribute to defining a low loop impedance.

The highest operating voltage for an electrical vehicle that we are aware of is 800 V[1]. Current probe users have expressed interest in current probes with a DC current handling of up to 1000 A. For simplicity reasons, it is assumed that 800 V_{DC} delivers 800 A, which infers a DC loop impedance of 1 ohm. In Figure 6, this 1 Ω would be the sum of Rs_{ource} and R_{load}.

To establish a nominal value for $L_{HARNESS}$ in Figure 6, the wire gage rated for 800 A was researched and found to be 750 AWG[2], which has a diameter of about 30 mm. Using "All About Circuits"[3], we established a harness inductance for this diameter wire, 1700 mm long and 50 mm above a ground plane over a dielectric material, and having a relative permeability of 1.4, yielding a value for $L_{HARNESS}$ of about 0.89uH.

It is obvious that $L_{HARNESS}$ will start to dominate the loop impedance at some point, depending

1. https://www.castleelectric.com
2. https://www.wiresizecalculator.net
3. https://www.allaboutcircuits.com

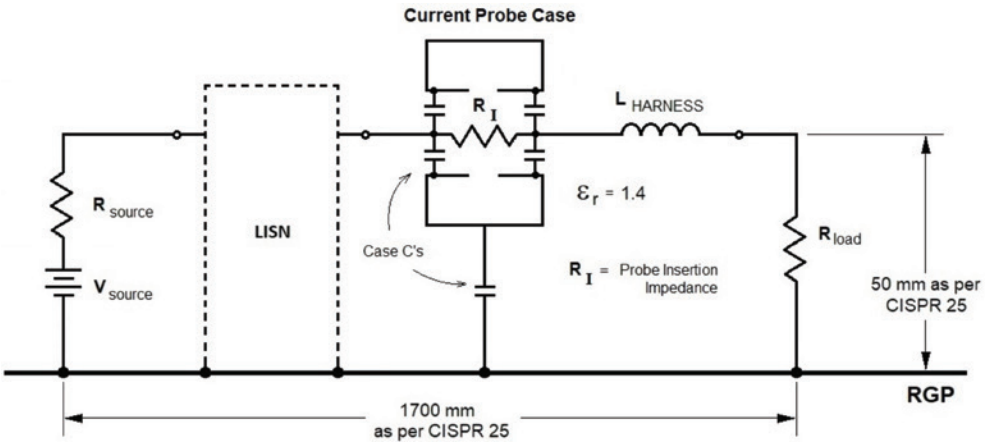

Figure 6: Conceptual layout of a CE current setup, per CISPR 25

on frequency. If it is assumed that the $L_{HARNESS}$ impedance is to be at least 10 times the presumed 1 Ω insertion impedance, introduced by the current probe, for the insertion impedance to be negligible, this leads to:

$$2 * \pi * f * L_{HARNESS}, = 10\ \Omega, \text{ therefore } f = 1.43\ \text{MHz}$$

Based on the consideration above, the following can be concluded:

- For a very low loop impedance, the harness inductance will start to dominate the total loop impedance above approximately 1.43MHz;
- As the operational current drops, the load resistance R_{load} will increase, which further mitigates any impact of the current probe insertion impedance; and
- If one 50 Ω/5 uH LISN, as defined in CISPR 16-1-2, is included in the series loop impedance, the loop impedance will only increase; at 150 kHz, this LISN would add an impedance of about 4.7 Ω. At the frequency 1.43 MHz previously calculated, the LISN added impedance is about 33 Ω. If a second LISN is included in the series impedance, the impedance will increase further, reducing any impact of the insertion impedance.

Considering the potential for resonances on the 1700 mm harness length, as specified in CISPR 25, the situation gets more complex. Assuming the rule of thumb applies that resonances will be negligible for frequencies when the wavelength is less than λ/10, for a wavelength of 1700 mm, the critical frequency is about 17.6 MHz. Above this frequency, potential resonances need to be considered. It is unclear what the meaning of insertion impedance in the presence of resonances really means.

Summarizing these factors, it is not clear why the specified insertion impedance of 1 Ω for current probes will ever have any serious impact on any CE test per CISPR 25 at test frequencies above a few 10s of MHz (and possibly much lower) and especially considering the upper usage frequency of 1 GHz, as inferred by CISPR 16-1-2.

Addressing the effect of the capacitance shown in Figure 6:

- CISPR 16-1-2 defines this shunt capacitance between the probe case to the wire under test. The origin of and rationale for this requirement is not known. If the assumption is that this capacitance is compromising the transfer impedance of the current probe, then it seems that this effect would be accounted for during routine probe calibration. If the intent is that this capacitance is possibly affecting the CE measurements, then this capacitance would be a presumed shunt to ground for measured CE signals.

  At 1 GHz, 25 pF is about 6.4 Ω. Based on a parallel argument to that made previously regarding the impact of $L_{HARNESS}$, it is not clear why the impact of this capacitance wouldn't also be minimized. For example, using the 1.43 MHz frequency, estimated in the above example, this capacitive impedance is about 4500 Ω; it doesn't seem a likely problem in a real test setup.
- No method for measuring this capacitance has been defined. De facto, the inference is that the shunt capacitance would have to be measured in the test setup itself, to "verify" compliance of the current probe. It does not seem practical to define such an in-situ specification (which indicates a pass/fail for the current probe and/or the test configuration), especially at high frequencies where suitable measurement devices either don't exist or are expensive to implement
- Therefore, it is not evident that such a specification is really needed.

SPECIFICATIONS FOR CURRENT PROBE TRANSFER IMPEDANCE IN CISPR 16-1-2

Currently, CISPR 16-1-2 calls out specifications for the transfer impedance and the frequency response of the transfer impedance. These are presented as normative where it seems they should be, at most, informative. Both specifications related to transfer impedance require all current probes to meet these specifications. Conversely, if current probes do not meet such requirements, they cannot be used, and measurement results are compromised. This inference is inaccurate and confusing to users of current probes.

The document prepared by CISPR/D in 2023 further reinforces this notion by showing a variety of current probes, separated into frequency ranges where the probe meets stated specifications, along with some limits for usability. Appendix B.3 of CISPR 16-1-2 infers that the upper "limit" of +15 dBΩ, shown in the CISPR/D document, derives from the notion that a higher transfer impedance automatically exceeds the 1 Ω insertion impedance requirement. This would appear to derive indirectly from the simplified circuit models for a current probe given in Appendix B.2. However, Reference 4, which discusses the wide-band characterization of current probes, states that models based on simple transformer theory may not work above 100 MHz. This reference presents a complicated mathematical method (possibly impractical for the average user to employ) for recovering current probe behavior at higher frequencies up to 3 GHz. Reference 4 also presents some modeling but only up to 100 MHz.

Therefore, it seems unnecessary to establish transfer impedance "limits," a fact that also causes confusion for users. Furthermore, the frequency response specification infers that the stated frequency ranges are the ones over which current probes should be calibrated, which is simply incorrect and misleading. The current specifications regarding transfer impedance should be removed from the normative part of the standard.

We further suggest revising Appendix B of the standard to provide information about the proper selection of current probes to achieve the necessary test system sensitivity, taking into consideration the current level to be measured, including measuring instrument noise floor, saturation, required resolution bandwidth, etc.

CONCLUSIONS

In general, CISPR/A should establish specifications for test equipment that support applications and measurement needs of product committees like

CISPR/D. Currently, the specifications related to current probes seem arbitrary and may even hinder the use of current probes in certain measurement scenarios.

The purpose of the 1 Ω insertion impedance requirement is not obvious. Other test considerations would seem to dominate over any possible impact of a 1 Ω impedance. Furthermore, suggested insertion impedance measurement approaches, presented up to 100 MHz, do not seem to yield results that allow an extension in frequency to ranges required, for example, by CISPR 25 (to 245 MHz). Therefore, it is suggested to remove this requirement from the normative part of CISPR 16-1-2.

Furthermore, the shunt capacitance requirement of 25pF is confusing since it is not clear if this requirement applies to the calibration aspect of current probes or to the use in an actual application. It seems very impractical to have users verify this value in an actual measurement setup. If this requirement is to be interpreted as an aspect of a current probe calibration process, its usefulness is questionable since the calibration setup (using a calibration fixture) will certainly differ from the actual measurement setup that uses a harness, for example. Therefore, it is suggested to remove this requirement from the normative part of CISPR 16-1-2.

It does not seem appropriate for CISPR/A to define frequency ranges for the frequency response of the transfer impedances since there is no basis provided for setting such requirements. These requirements set bounds on a user regarding the selection of a current probe for a specific application. Since there is no basis given for this requirement, it should be removed from the normative part of the standard.

Resolving the issues identified in this article will hopefully allow current probe users to perform measurements in accordance with product standards like CISPR 25 with the sensitivity required.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Alexander Kriz of Seibersdorf Laboratories in Siebersdorf, Austria for allowing us to reproduce the graphics that constitute Figures 1, 2, and 3 in this article.

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LABORATORY AUTOMATION WITH PYVISA

Applying Python and PyVISA to Automated Testing

Python has become a widely used programming language in the area of electronic test automation, especially when used with the PyVISA library. While the fundamental principles of lab automation have been around for a long time (i.e., the SCPI protocol), Python and PyVISA have made it easy to get started quickly with test automation. Once data has been collected, Python also has a plethora of data analysis tools (pandas, scipy, scikit, etc.) that are useful in analyzing data.

In this article, I will introduce how to interface with instruments using Python/PyVISA and give a practical example of measuring power supply efficiency. Finally, I will introduce how to plot gathered efficiency data directly in Python.

SCPI PROTOCOL

The Standard Commands for Programmable Instruments (SCPI) is a definition layer on top of the IEEE 488.2-1987 standard for instrument communication. While SCPI was originally meant for IEEE 488.1 (GPIB connections), this has expanded to include RS-232, Ethernet, USB, and several others. SCPI commands are sent in ASCII format and received as a string of ASCII text. Here is an example of a simple SCPI transaction:

Host query: `*IDN?`

Device reply: `Siglent Technologies,SDL1020X-E,SDLxxxxxxxxxx,1.1.1.21R2\n`

SCPI defines a number of generic commands like `MEASure` and `CONFigure`, which can be used to read data from or configure parameters on test equipment.

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By Dr. Zachary Nosker

VISA Specification

Unfortunately for the SCPI standard, different operating systems, interfaces, and devices meant that the early days of SCPI required different libraries for each device and bus system. In order to alleviate this pain, the Virtual Instrument Software Architecture (VISA) specification was created to seamlessly work with all devices and bus systems.

PYTHON AND PYVISA

Even with the VISA specification in place, it has traditionally been challenging to interface a host computer to measurement devices without expensive/cumbersome software and hardware. With these drawbacks in mind, the PyVISA library was created to simplify instrument communication and make lab automation more efficient.

Python itself is a free, interpreted programming language that can be used with any modern operating system. Since this is an interpreted (and not compiled) language, Python can generally be "installed" on any system, even where the user does not have admin/root access. While the syntax of Python can take some getting used to (spaces are used as delimiters instead of ; or other characters), it is a very widely used language with many libraries, examples, and code snippets available.

PyVISA works as a front end to the VISA library and simplifies the process of communicating with instruments. PyVISA is officially tested against National Instruments' VISA and Keysight IO Library Suite and can be used with hardware adapters from National Instruments, Keysight, and many others.

To get started, here is a simple program that queries what instruments are visible to PyVISA on my computer. In the below code snippet, I am using National Instruments VISA on a 64-bit Windows computer running Python 3.11.5 and PyVISA 1.13.0

In [2]:

```
import pyvisa
instruments = pyvisa.ResourceManager().list_
resources()
instruments
```

Out[2]:

```
('USB0::0xF4EC::0x1621::SDL13GCQ6R0772::INSTR',
 'USB0::0x2A8D::0x3402::MY61003767::INSTR',
 'GPIB0::12::INSTR',
 'GPIB0::22::INSTR')
```

This output shows there are four instruments connected to my computer, two connected by USB and two by GPIB. Now we can create an object for each instrument and query what it is. Note that all instruments will reply to the special `*IDN?` Command:

In [5]:

```
for i in instruments:
    inst = pyvisa.ResourceManager().open_resource(i)
    print(i,inst.query('*IDN?'))
```

```
USB0::0xF4EC::0x1621::SDL13GCQ6R0772::INSTR Siglent
Technologies,SDL1020X-E,SDL13GCQ6R0772,1.1.1.21R2

USB0::0x2A8D::0x3402::MY61003767::INSTR Keysight
Technologies,E36234A,MY61003767,1.0.4-1.0.3-1.00

GPIB0::12::INSTR HEWLETT-PACKARD,34401A,0,7-5-2

GPIB0::22::INSTR HEWLETT-PACKARD,34401A,0,11-5-2
```

From the query, you can see I have a Keysight power supply (E35234A) and a Siglent power supply (SDL1020X-E). For the following example, I am using the Siglent power supply only to read the input and output voltages of the device under test (DUT).

MEASURING EFFICIENCY

For a power supply, efficiency is the measure of how much power you get out per unit of power put in. Since $P = VI$, this can be written as:

$$\eta = \frac{P_o}{P_{in}} = \frac{v_O \times i_O}{v_I \times i_I}$$

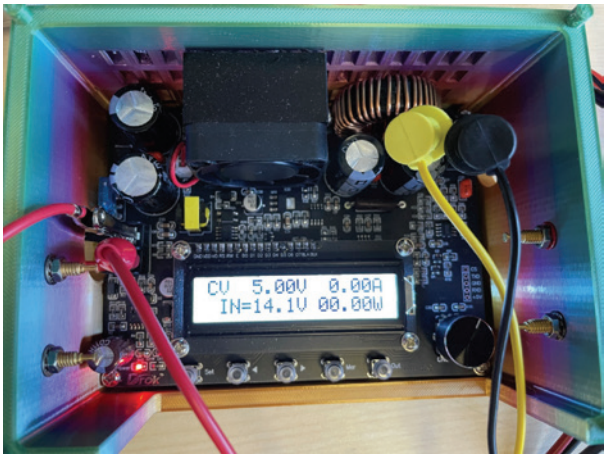

Figure 1: Drok 720 W Adjustable DC Power Supply

As this equation gives a fraction less than 1, it is customary to multiply by 100 and express efficiency as a percentage.

POWER SUPPLY SETUP

For the following test, I am using a 720 W adjustable DC-DC power supply from DROK (shown in Figure 1). For the purpose of this example efficiency test, I am using a constant input voltage of 25 V with a fixed output of 12 V. Note there is a large fan near the North side of the board which turns on when the power supply is under heavy load. We will see the effects of this fan in the full efficiency characteristic.

PRACTICAL EFFICIENCY MEASUREMENTS¶

In order to measure the efficiency of a DC-DC power supply, we must apply a source voltage v_s and a load current i_{LOAD}. The voltage source is a DC voltage and the load current is an electronic load running in the constant current mode. We step up the load current and measure the efficiency at various load points to create a full plot showing the efficiency characteristic of the power supply.

Since each measurement requires four values (input voltage, input current, output voltage, and output current), we need sufficient equipment to read all these parameters. In practice, it is beneficial to measure the input and output voltage on separate meters as close to the DUT as possible.

For current measurements, reading the current directly from the voltage source (for input current) and the electronic load (for output current) are generally close enough when using modern, calibrated equipment.

Instrument Objects for Efficient Data Collection

We can use the tools available in Python to create an object for each piece of equipment and create a standard list of methods that our instruments will use. As an example, we can make a read_v() method for all of our instrument objects to read the voltage value. At the top level, we just see the method instrument. read_v(), but this actually maps to the specific SCPI commands for our instrument and returns data that Python can read.

For this test, we will need four instrument objects, though the voltage measurements will be instances of the same object with different addresses (same meter, different GPIB address).

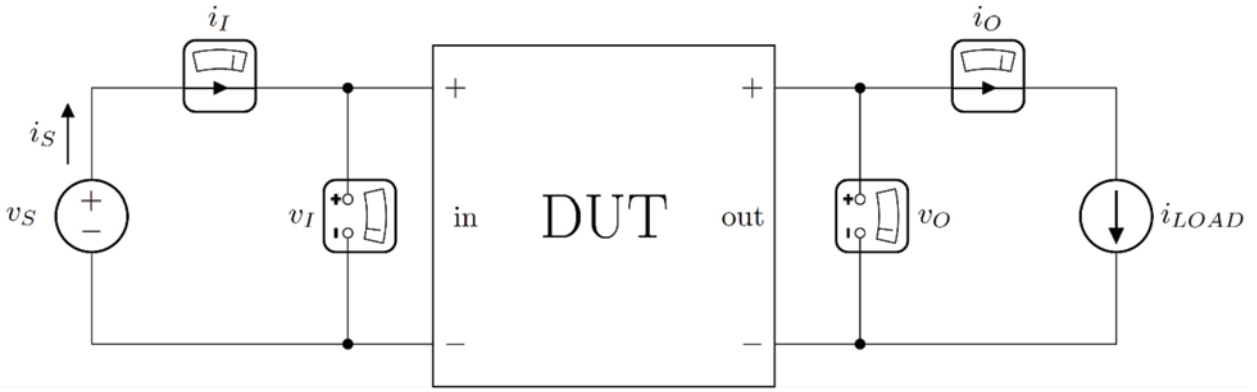

Figure 2: Practical instrumentation of power supply for efficiency measurements

GENESYS™ AC

TDK-Lambda Genesys™ AC Sources

Testing to global standards for consumer and industrial products, marine electronics, and avionics requires high quality, reliable and easy to use AC sources to generate the wide variety of voltages and frequencies used in the application worldwide, but also to easily and repeatedly simulate disturbances and irregular conditions. All of this was considered in the development of the Genesys AC family of AC Sources.

Compact yet powerful, the Genesys AC products offer 3kVA per 1U of rack space, that the user can combine to easily expand to higher power and multiphase operations. The 0-350VAC range per unit allows for three phase systems to be tested to over 600VAC L-L, at frequencies to 1200Hz.

The Genesys AC Pro models include the added functionality of AC+DC output, analog input for Real-Time control with low latency, and the option for frequencies up to 5kHz.

Genesys AC Source key features

- 2 and 3 kVA models in 1U design, that can be paralleled or combined for higher power and multiphase operation.
- AC from 0-350VAC and AC+DC models allowing +/- 500VDC, and providing offering full current range and power in DC modes.
- Clear and responsive color touch screen, offering easy access to the many features and functions through an intuitive menu structure.
- Wide selection of interfaces is standard with IVI/LabView drivers and Virtual Control Panel (GUI) included.
- IEC, marine and avionics test standards available.

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In [6]:

```
#Basic object for Keysight E36200 series power
supply
#Note that channel must be specified
class keysight_E36200(object):

    def __init__(self, visa_address, **kwargs):
        self.pyvisa = pyvisa.ResourceManager().
open_resource(visa_address)
        #
        #Setup some things
        #
        self.__channel = int(kwargs['channel'])

        #check if this is the correct device

    def set_v(self, voltage):
        self.pyvisa.write('VOLT {0:G}, (@{1})'.
format(voltage,self.__channel))

    def set_i(self, current):
        self.pyvisa.write('CURR {0:G}, (@{1})'.
format(current,self.__channel))

    def read_v(self):
        return float( self.pyvisa.query('MEAS:VOLT?
(@{0})'.format(self.__channel)) )

    def read_i(self):
        return float( self.pyvisa.query('MEAS:CURR?
(@{0})'.format(self.__channel)) )

    def output_enable(self):
        self.pyvisa.write('OUTP 1, (@{0})'.
format(self.__channel))

    def output_disable(self):
        self.pyvisa.write('OUTP 0, (@{0})'.
format(self.__channel))
```

In [7]:

```
class SDL1000X(object):

    def __init__(self, visa_address):
        self.pyvisa = pyvisa.ResourceManager().
open_resource(visa_address)
        #
        #Setup some things
        #

    def read_v(self):
        return float(self.pyvisa.
query('MEASure:VOLTage:DC?'))

    def read_i(self):
        return float(self.pyvisa.
query('MEASure:CURRent:DC?'))

    def set_i(self, current):
        self.pyvisa.write(':SOURce:CURRent:LEVel:I
MMediate {0:f}'.format(current))

    def output_enable(self):
        self.pyvisa.write(':SOURce:INPut:STATe ON')

    def output_disable(self):
        self.pyvisa.write(':SOURce:INPut:STATe OFF')
```

In [8]:

```
class hp34401(object):

    def __init__(self, visa_address):
        self.pyvisa = pyvisa.ResourceManager().
open_resource(visa_address)

    def read_v(self, average=1):
        #start from v=0, add values and average as
needed
        v = 0.0
        self.pyvisa.write("CONFigure:VOLTage:DC")

        for x in range(average):
            v += float(self.pyvisa.query("READ?"))

        voltage = v / average

        return voltage
```

We also need to import a few libraries which will be helpful for this test:

In [9]:

```
import time
import numpy as np
import pandas as pd
```

Then, create an object for each instrument with a descriptive name:

In [10]:

```
inst_load = SDL1000X('USB0::0xF4EC::0x1621::SDL13
GCQ6R0772::INSTR')
inst_supply = keysight_E36200('USB0::0x2A8D::0x340
2::MY61003767::INSTR',channel=1)
inst_vin_sense = hp34401('GPIB0::12::INSTR')
inst_vo_sense = hp34401('GPIB0::22::INSTR')
```

We now have objects for the four instruments we are using to measure efficiency, and each instrument has high-level methods with descriptive names. Note again that the actual SCPI commands sent to each object are very different, but the intended data (like measuring current) returns the appropriate data for Python.

Calibrate Input Voltage

The wire connecting from the power supply to the DUT has a finite impedance, and when the input current increases (due to increasing load current), the input voltage seen at the input of the DUT will decrease. In order to compensate for this effect, we can directly measure the voltage right at the DUT and increase/decrease the supply voltage to stay within a certain bound (in this case, 10mV).

In [11]:

```
def calibrate_vin(supply, sense, v_target):

    v_meas = sense.read_v()
    v_diff = v_meas - v_target

    #Keep input to within 10mV
    while abs(v_diff) > 0.01:
        supply.set_v(supply.read_v() - v_
diff/1.5)
        time.sleep(1)

        v_meas = sense.read_v()

        v_diff = v_meas - v_target
```

Cooldown¶

When using the calibration function above and at very high load currents, it is possible that the input voltage will be so high that it could electrically overstress (EOS) the device we are testing. To avoid this, we can create a simple "cooldown" loop that decreases the load and lowers the supply voltage slowly down to a safe voltage:

In [12]:

```
def cooldown(v_final,steps):
    #Read current and voltage right now
    v_now = inst_supply.read_v()
    i_now = inst_load.read_i()

    #Determine step size
    v_step = (v_now - v_final)/steps
    i_step = i_now/steps

    #Reduce by step sizes
    i_now -= i_step
    v_now -= v_step

    for s in range(steps):
        inst_supply.set_v(v_now)
        inst_load.set_i(i_now)
        i_now -= i_step
        v_now -= v_step
        time.sleep(1)
    #Disable when current is 0 and voltage is at
target
    inst_load.output_disable()
    inst_supply.output_disable()
```

Initial Setup¶

Next, we need to set up the loads point we will use for our test and set the remaining parameters. All test data will be stored in a Pandas DataFrame object which will be useful for plotting and exporting to .csv later on.

In [13]:

```
load_currents = np.linspace(0,5,51) #100mA steps
#load_currents = np.logspa
ce(-2,0.6989700043360189,100)

supply_voltage = 25

inst_supply.set_v(supply_voltage)
inst_supply.output_enable()
time.sleep(1)

inst_load.set_i(0)
inst_load.output_enable()

input("Press ENTER when ready\n")

row_counter = 0

column_labels = ['Vin_set','Iload_set','Vin','Iin'
,'Vout','Iout','Efficiency']
all_data = pd.DataFrame(columns=column_labels)
```

Loop Through Currents¶

The main loop works as follows:

1. Set the next load current value on the electronic load;
2. Wait for the current to stabilize;
3. Calibrate the input voltage (right at the DUT) to keep this close to the supply voltage value;
4. Read all meters and calculate efficiency;
5. Store all read data as a new row in the all_ data DataFrame; and
6. Increment the row counter and continue to the next load value.

In [14]:

```
for lc in load_currents:
    inst_load.set_i(lc)
    time.sleep(1)
    calibrate_vin(inst_supply, inst_vin_sense,
supply_voltage)

    data = [supply_voltage,
    lc,
    inst_vin_sense.read_v(),
    inst_supply.read_i(),
    inst_vo_sense.read_v(),
    inst_load.read_i()]

    efficiency = (100* data[4] * data[5]) /
(data[2] * data[3])
    data.append(efficiency)

    #print(*data, sep=",")
    all_data.loc[row_counter] = data

    row_counter += 1
```

Cooldown and Save Data¶

Once the loop is complete, cooldown in 10 steps and save the all_data DataFrame to a .csv file (with a timestamp that guarantees all data files are unique):

In [15]:

```
cooldown(supply_voltage,10)

timestamp = time.strftime("%Y.%m.%d.%H.%M.%S")

all_data.to_csv('.\\data\\
Efficiency_'+timestamp+'.csv')
```

Plot data inline¶

Since the entire all_data DataFrame still exists in memory, we can easily plot this using matplotlib:

In [22]:

```
%matplotlib inline
import matplotlib.pyplot as plt
```

In [31]:

```
all_data.plot(x='Iout',y='Efficiency')
plt.title('Efficiency vs. Load Current')
plt.xlabel('Load Current (A)')
plt.ylabel('Efficiency (%)')
plt.show()
```

Note that there is a large dip in efficiency when the load current is near 2 A. This is the point where the fan on the DC-DC converter turns on and causes a noticeable kink in the efficiency characteristic.

Plot With Log X Axis¶

Similarly, we can change the X axis to logarithmic scale, which tends to show a smooth curve when plotting efficiency:

In [37]:

```
fig, axs = plt.subplots(1)
all_data.plot(ax=axs,x='Iout',y='Efficiency')
plt.title('Efficiency vs. Load Current')
plt.xlabel('Load Current (A)')
axs.set_xscale('log')
plt.ylabel('Efficiency (%)')
plt.show()
```

SUMMARY

Using Python and the PyVISA library, we have created instrument objects and a simple program to tabulate the efficiency of a DC power supply.

We have also used the plotting tools in Python to create graphs of efficiency for this test.

With the basic program in place, it is possible to modify this program to add features, including:

- Loop through different input voltages;
- Change the tested currents;
- Save plot data as image or pdf files; and
- Save data as a Word document or PowerPoint slides.

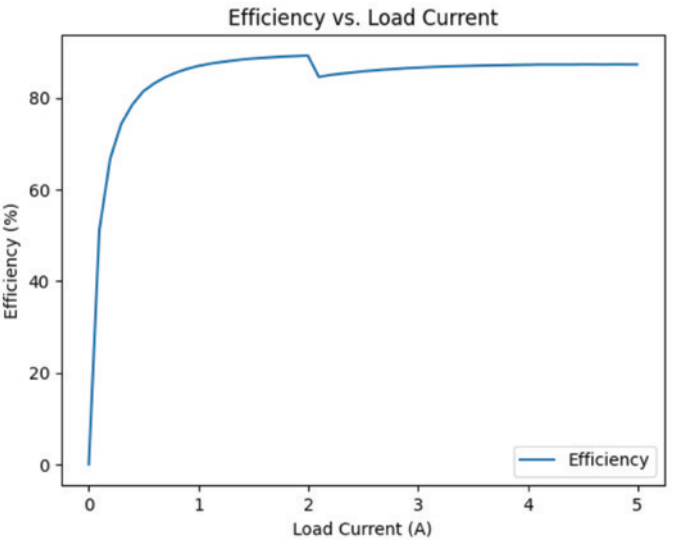

Figure 3: Python plot of efficiency vs. load current

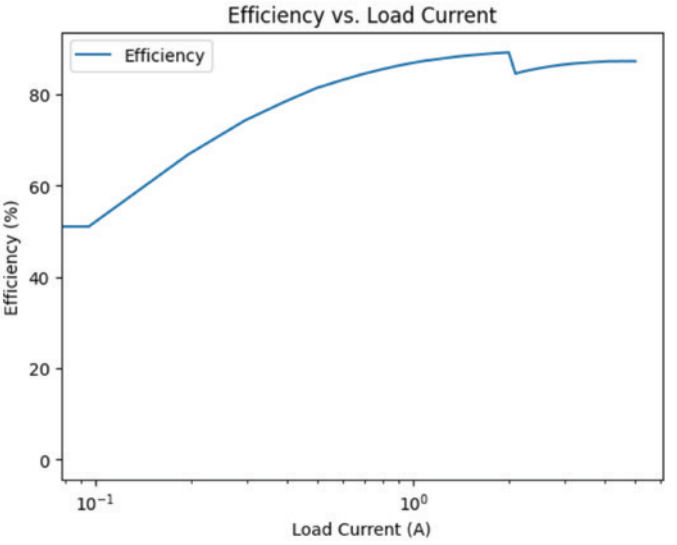

Figure 4: Plot of efficiency vs. load current with a logarithmic X axis

THE ENGINEER'S

TEST LAB HANDBOOK

Inside

OBTAINING NRTL APPROVALS

Don MacArthur, The Practical Engineer, is a Guest Contributor to *In Compliance Magazine*. He has over 30 years of experience in product development, EMC, testing, and product safety compliance. He has developed products for military, commercial, and industrial applications.

By Don MacArthur

Most markets of electrical/electronic devices require some form of third-party safety agency certification of the products before they can be sold into that market. In North America, this involves working with a third-party safety certification agency, also known as a Nationally Recognized Testing Laboratory (NRTL), the entity that verifies the product complies with the applicable UL/CSA safety standards.

Working with an NRTL such as UL or CSA can be very challenging and frustrating. The usual experience is that projects are late, costs are overrun, and certification reports are often inaccurate. This is not always the fault of the NRTL.

CUSTOMER ACCEPTANCE

For most electrical/electronic products, the NRTL certification logo must be printed on NRTL-approved labels, and the label must be placed on the products before they can be installed at a customer's premises, installed into customer racks or panels, and later powered on for official use by the customer. The NRTL logo on the product confirms it has been evaluated by an NRTL and complies with all applicable product safety standards. Due to OSHA, other safety regulations, and customer requirements, there is usually no way to bypass the NRTL third-party certification process, and involvement of an NRTL in electrical/electronic development is nearly necessary.

THIRD-PARTY PRODUCT SAFETY CERTIFICATION APPROVAL PROCESS

An NRTL certification process is a lengthy 5-step process culminating in either a "Findings Report" for products that do not comply or a "Certification Report" for products that do comply. The Certification Report is used during factory inspections to verify that the product continues to be manufactured as originally certified.

The 5-Step Certification Project Process is as follows:

Step 1: Construction Review

The assigned NRTL engineer reviews the physical design of the product to determine its compliance with the applicable safety standards and inspects samples of the product while verifying and documenting compliance. They will confirm spacings (creepage and clearance distances), review the instruction manual, and all markings and labels. This is a time-consuming process, and the report is hundreds of pages in length. As part of their investigation, the NRTL will review schematics, block diagrams, unvarnished (or un-potted) samples of transformers, adequacy of dimensions/spacings on actual samples, adequacy of safety-critical components such as fuses, Y-capacitors, X-capacitors, optocouplers, terminal blocks, the enclosure, and other product markings. The safety instructions required by the standards must be included in the instruction manual and the NRTL will also review this information as part of the certification efforts.

During their investigation, the NRTL is looking for any issue that would jeopardize protection against electric shock or protection against mechanical hazards.

They look for resistance to mechanical stresses, protection against the spread of fire, equipment temperature limits and resistance to heat, protection against hazards from fluids, protection against radiation, including laser sources, and against sonic and ultrasonic pressure. Finally, they look for protection against liberated gases and substances, explosion, and implosion if applicable to the product.

The purpose of testing is to confirm that safety hazards do not exist during normal operation and single fault conditions. A test plan guides the NRTL in selecting test conditions and test parameters for each test and each product variation to be tested.

Step 2: Testing

The worst-case product configuration/loading is selected for testing. The purpose of testing is to confirm that safety hazards do not exist during normal operation and single fault conditions. A test plan guides the NRTL in selecting test conditions and test parameters for each test and each product variation to be tested. When prototypes are available, several samples of the product must be sent to the NRTL, or the NRTL must visit the manufacturer to conduct a safety investigation and perform testing. The NRTL will conduct many tests on the product, including temperature, humidity, dielectric strength, impulse, ingress protection, overload, breakdown of components, transformer abnormal operation, ground continuity, and impact – just to name a few!

Step 3: Project Reports

Based on the results of the construction review and testing, one of two different reports may be generated by the NRTL.

Findings Report

If it is determined the product is non-compliant in construction features or test results, the NRTL engineer provides a Findings Report that summarizes their concerns. The NRTL engineer working on the project is usually not allowed to provide solutions to correct any non-compliance; they may, however, provide suggestions for bringing the product into compliance. If a Findings Report is received, expect an extension of the project timeline and an increase in fees associated with a re-evaluation of the corrected product.

Certification Report

If all goes well and the product is found to comply during the construction review and testing, the NRTL engineer drafts a Certification Report instead of a Findings Report. The Certification Report controls the elements of the product that are critical to bringing the product into compliance with the safety standards. Items that are considered critical include safety critical components (i.e., items that provide isolation), dimensions, materials, safety instructions, and required markings. Pictures and illustrations are included in the report. Manufacturers use this report to guarantee they continue to produce a product that complies with the safety standards.

Step 4: Project Review

A second NRTL engineer reviews the draft Certification Report produced by the original NRTL engineer assigned to the project. The second NRTL engineer must agree with the first engineer's conclusions that the product complies with the safety standards and the product was tested adequately. Very often, the reviewing engineer finds discrepancies that affect the Certification Report and which the first engineer must correct before certification is granted. Sometimes, this finding negatively impacts the manufacturer, especially if additional testing is deemed necessary or a component is found non-compliant with the safety standards late in the product development cycle.

Step 5: Report Issued

After review and approval by a second NRTL engineer, the NRTL issues the Certification Report.

The manufacturer must verify this report is accurate prior to project closure; otherwise, they could receive a variation notice (i.e., non-compliance finding) during one of the unscheduled quarterly factory audits that are performed by the NRTL. It is during these audits that the NRTL reviews the report issued against the product produced to ensure the manufacturer is continuing to produce a product as described in the report and which complies with the safety standard.

With the manufacturer's help, the NRTL must determine the worst-case configuration for testing, and this often involves some experimentation, resulting in extra time and money over what is typically required for much simpler products.

PRODUCT COMPLEXITY

Complicating the product safety certification process is that many electrical/electronic products have many different configurations available, several of which have circuits that are considered hazardous from a safety perspective because of the voltages, currents, and/or energies involved. This variety and complexity confuse the NRTL, making their job much more difficult. With the manufacturer's help, the NRTL must determine the worst-case configuration for testing, and this often involves some experimentation, resulting in extra time and money over what is typically required for much simpler products.

HISTORICAL NRTL ISSUES

Some of the issues the author has experienced during product safety certifications include:

- NRTL engineer lacked experience and overlooked some requirements.
- NRTL didn't understand the full scope of the project prior to quoting.
- Tests were not performed correctly, and retesting was required.
- NRTL requested additional scope not originally agreed upon during project planning resulting in further delays and increased costs.
- Issues with safety-critical components were identified too late in the project.
- Uncoordinated findings were provided throughout the review.
- Inconsistent instruction manual safety information provided.

WHAT MANUFACTURERS CAN DO TO MAKE THIRD-PARTY SAFETY CERTIFICATION GO EASIER?

Projects that do not involve long-term testing can be completed within an 8-to-12-week timeframe; however, the author has experienced that the time required is much longer with some NRTLs.

Here are some tips that have proved helpful in obtaining NRTL approval more effectively:

- Generate a critical component list early in the product development process and verify that these components comply with relevant UL/CSA/IEC standards. Obtain third party-issued IEC CB Certificates, UL/CSA File numbers, and datasheets for these safety-critical components.
- Consider having the NRTL conduct a preliminary investigation of the design, especially if involves a new product concept or unique design.
- Don't wait for perfect samples to start testing.
- Consider breaking up one big project into smaller ones, as the scope of the smaller projects will be much easier for the NRTL to understand and manage.
- Provide correct/detailed insulation diagrams at the launch of the NRTL evaluation.
- Read the applicable standard and know it as well as or better than the NRTL engineers.
- Design the product to comply with the standard from product inception.

SUMMARY

Working with an NRTL to obtain product safety certification is often a laborious process that often results in cost increases and product shipment delays. With slight changes to how manufacturers go about it, many of these troublesome issues can be avoided, costs will decline, and product shipment deadlines will be met.

REFERENCE

1. CertifiGroup, *Understanding the UL – CSA Certification Process.*

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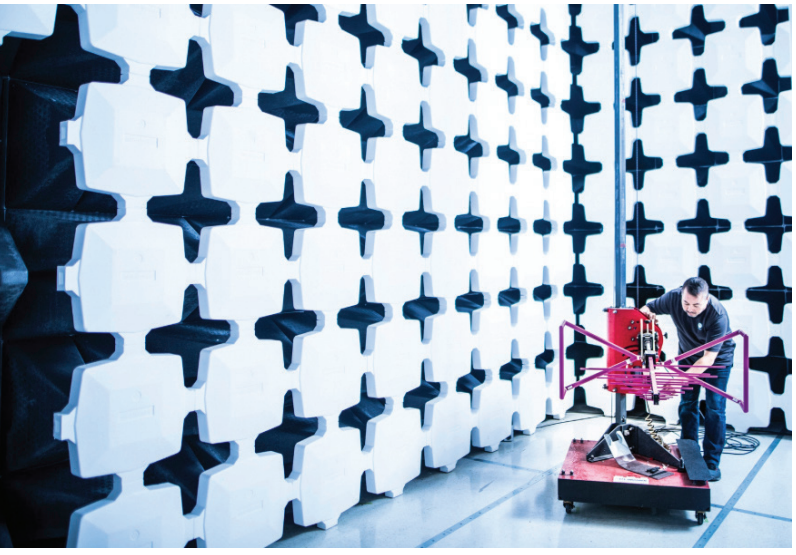

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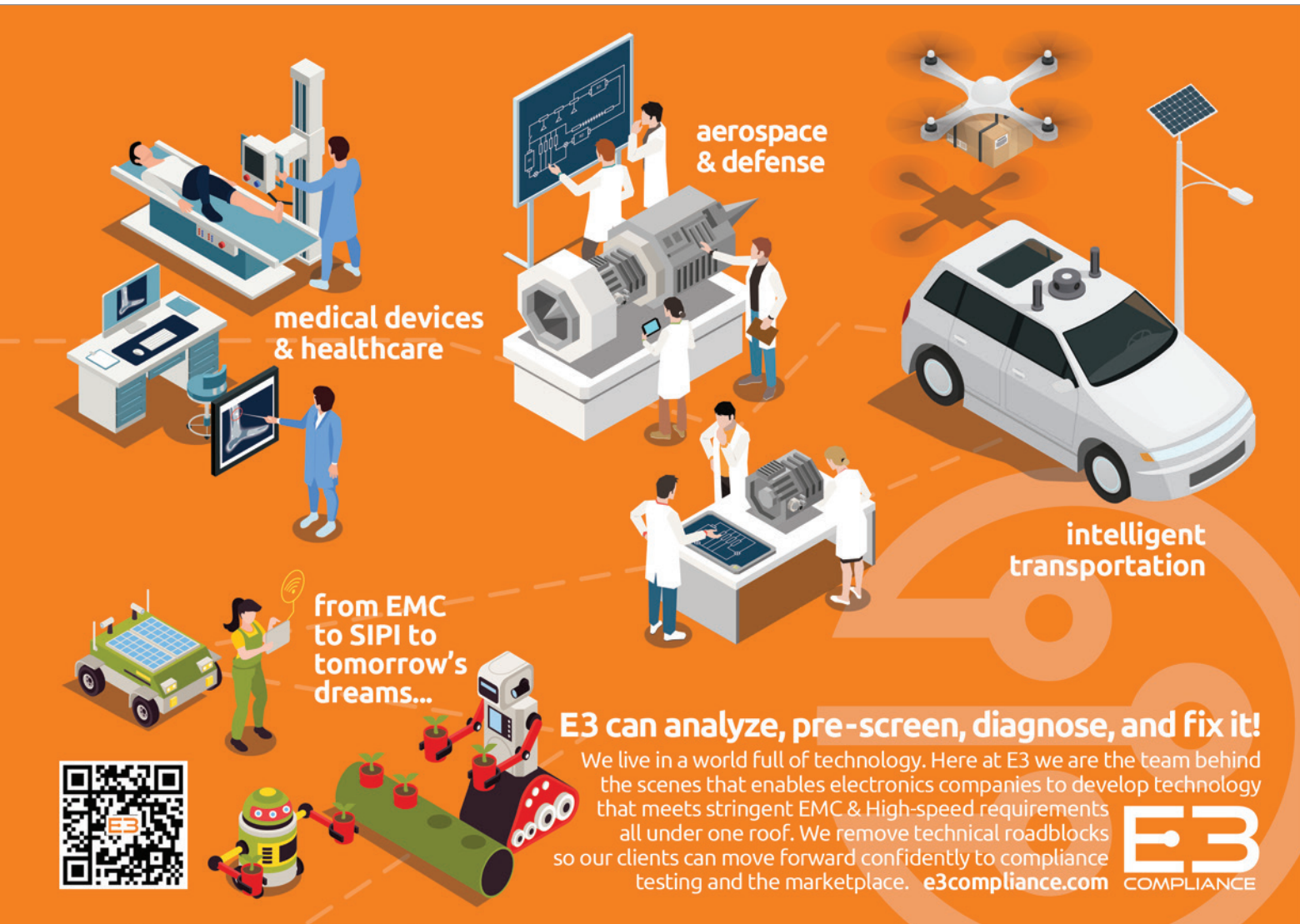

ANALYSIS OF TRANSMISSION LINES IN SINUSOIDAL STEADY STATE

Different Circuit Models and Their Applications: Part 3

By Bogdan Adamczyk

This is the third and final article discussing four different circuit models of transmission lines in sinusoidal steady state. In [1], Model 1 and Model 2 were presented. Model 1 was used to present the solution of the transmission line equations. Model 2 introduced the standing waves. Model 3 discussed in [2] led to the evaluation of the *values* of the minima and maxima of standing waves. This article uses Model 4 to determine the *locations* of the minima and maxima of standing waves. This determination is first done analytically, followed by the graphical method using the Smith chart.

Dr. Bogdan Adamczyk is professor and director of the EMC Center at Grand Valley State University (http://www.gvsu.edu/emccenter) where he performs EMC educational research and regularly teaches EM/EMC courses and EMC certificate courses for industry. He is an iNARTE-certified EMC Master Design Engineer. He is the author of two textbooks, "Foundations of Electromagnetic Compatibility with Practical Applications" (Wiley, 2017) and "Principles of Electromagnetic Compatibility: Laboratory Exercises and Lectures" (Wiley, 2024). He has been writing "EMC Concepts Explained" monthly since January 2017. He can be reached at adamczyb@gvsu.edu.

1. TRANSMISSION LINE MODEL 4

To present Model 4, it is helpful to recall Model 3, shown in Figure 1.

In Model 3, we are moving away from the source, located at $z = -L$ to the load located at $z = 0$. Model 4 is shown in Figure 2.

In Model 4, we are moving away from the load located at $d = 0$, towards the source located at $d = L$. Model 4 is obtained from Model 3 by simply relating the distance variables according to

$$d = -z \tag{1.1}$$

Model 3 was led to the expression for the magnitude of the voltage at any location z away from the source as

$$|\hat{V}(z)| = |\hat{V}_z^+|\{[1 + \Gamma_L^2 + 2\Gamma_L \cos(2\beta z + \theta)]\}^{\frac{1}{2}} \tag{1.2}$$

With the change of variables given by Eq. (1.1), Model 4 produced an expression for the magnitude of the voltage at any location d away from the load as [2],

$$|\hat{V}(d)| = |\hat{V}_d^+|\{[1 + \Gamma_L^2 + 2\Gamma_L \cos(2\beta d - \theta)]\}^{\frac{1}{2}} \tag{1.3}$$

In the next section, we will use this equation to determine the *locations* of the voltage maxima and minima in terms of the distance d away from the load.

2. LOCATION OF THE VOLTAGE MAXIMA AND MINIMA – ANALYTICAL SOLUTION

Examining Eq. (1.3), we deduce that the maximum magnitude of the voltage occurs when the cosine function equals 1 or its argument satisfies the condition

$$2\beta d_{max} - \theta = n2\pi, \quad n = 0,1,2,\ldots \tag{2.1}$$

and thus

$$d_{max} = \frac{\theta + 2n\pi}{2\beta}, \quad n = 0,1,2,\ldots \tag{2.2}$$

Since $\beta = 2\pi/\lambda$, Eq. (2.2) becomes

$$d_{max} = \frac{\theta + 2n\pi}{2\frac{2\pi}{\lambda}} = \frac{\theta\lambda}{4\pi} + \frac{n\lambda}{2}, \quad n = 0,1,2,\ldots \tag{2.3}$$

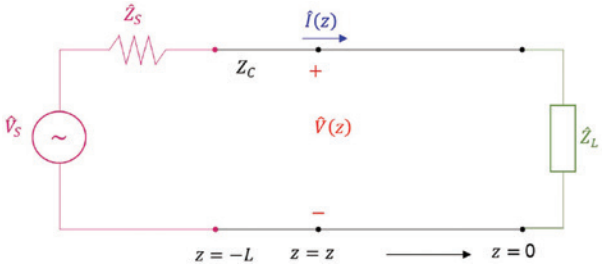

Figure 1: Transmission line circuit – Model 3

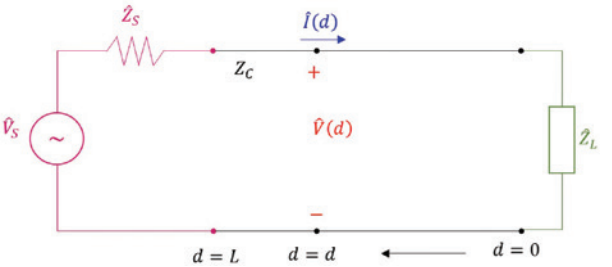

Figure 2: Transmission line circuit – Model 4

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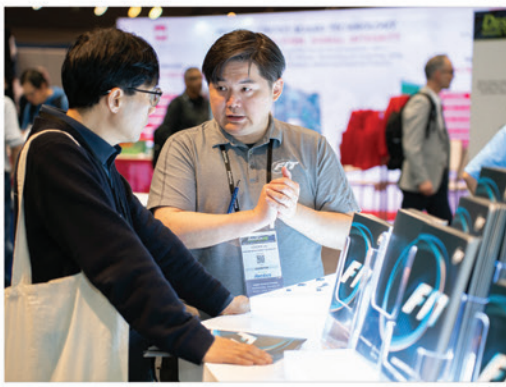

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leading to

$$d_{max} = \frac{\theta\lambda}{4\pi} + \frac{n\lambda}{2} \quad \begin{cases} n = 1,2,\ldots & if\ \theta < 0 \\ n = 0,1,2,\ldots & if\ \theta \geq 0 \end{cases} \tag{2.4}$$

The minimum magnitude of the voltage occurs when the cosine function equals -1 or its argument satisfies the condition

$$2\beta d_{min} - \theta = (2n+1)\pi, \quad n = 0,1,2,\ldots \tag{2.5}$$

and thus

$$d_{min} = \frac{\theta+(2n+1)\pi}{2\beta} = \frac{\theta+(2n+1)\pi}{2\frac{2\pi}{\lambda}} \tag{2.6}$$

leading to

$$d_{min} = \frac{\theta\lambda}{4\pi} + (2n+1)\frac{\lambda}{4}, \quad n = 0,1,2,\ldots \tag{2.7}$$

The spacing between adjacent minima and maxima is λ/4. The *first* minimum can be obtained from the *first* maximum as

$$d_{min} = \begin{cases} d_{max} + \frac{\lambda}{4}, & if\ d_{max} < \frac{\lambda}{4} \\ d_{max} - \frac{\lambda}{4}, & if\ d_{max} \geq \frac{\lambda}{4} \end{cases} \tag{2.8}$$

3. LOCATION OF THE VOLTAGE MAXIMA AND MINIMA – GRAPHICAL SOLUTION USING SMITH CHART

To illustrate this graphical solution, consider a load with the normalized load impedance [3],

$$\hat{z}_L = 2 + j1 \tag{3.1}$$

represented by point *A* in Figure 3.

Recall the phase-shifted load reflection coefficient [4]

$$\hat{\Gamma}(d) = \hat{\Gamma}e^{-j2\beta d} = \Gamma e^{j\theta}e^{-j2\beta d} = \Gamma e^{j(\theta-2\beta d)} \tag{3.2}$$

At point *B*, the total phase of $\hat{\Gamma}(d)$, that is, (θ - 2β*d*), is zero, or -2*n*π, (*n* being a positive integer).

As stated earlier, the maximum magnitude of the voltage occurs when the cosine function in Eq. (1.3) equals 1 or its argument satisfies the condition

$$2\beta d_{max} - \theta = n2\pi, \quad n = 0,1,2,\ldots \tag{3.3}$$

which is exactly the condition satisfied at point *B*. Thus, point *B* is the location of the voltage maxima.

At point *C*, the total phase of $\hat{\Gamma}(d)$, that is (θ - 2β*d*), equals -π or – (2*n* + 1)π (*n* being a positive integer).

As stated earlier, the minimum magnitude of the voltage occurs when the cosine function in Eq. (1.3) equals -1 or its argument satisfies the condition

$$2\beta d_{min} - \theta = (2n+1)\pi, \quad n = 0,1,2,\ldots \tag{3.4}$$

which is exactly the condition satisfied at point *C*. Thus, point *C* is the location of the voltage minima.

The corresponding minima and maxima are λ/4 apart.

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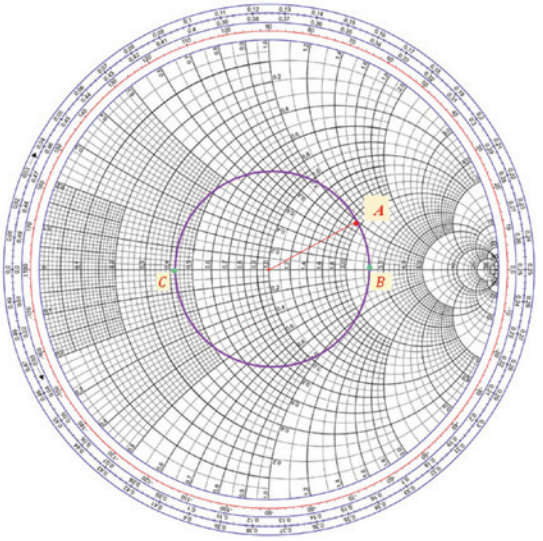

Figure 3: Smith Chart and the voltage maxima and minima

PRODUCT Showcase

THE IMPACT ON ESD RISK OF AI ON SILICON FABRICATION AND THE IMPLICATIONS OF INCREASING MEMORY STACKS

By James Davis, Greg O'Sullivan, Souvick Mitra, and Bong Andres for EOS/ESD Association, Inc.

Artificial intelligence (AI) has emerged as a significant game-changer across various industries. This influence of AI has fueled a dramatic increase in silicon fabrication, leading to substantial advancements in the semiconductor industry.

One of the most notable advancements in silicon fabrication and manufacturing is the development of high bandwidth memory (HBM) stacks. This should not be confused with the human body model for electrostatic discharge (ESD) model. These memory die stacks, which are located near the processor, have been increasing in number. This proximity and increased die stacking enhance memory density and the speed and efficiency of data transfer, significantly improving the performance of electronic devices that utilize AI hardware algorithms.

One concern with multiple die stacking is the risk of ESD at the die-to-die (D2D) interface during the manufacturing process. Because of this, there is a requirement to balance the amount of ESD protection on the interface without interfering with the speed, silicon area, and design at the interface. Progressively, advances in the D2D interconnect are becoming smaller and denser, further limiting the amount of acceptable ESD protection.

Recognizing this challenge, the ESD industry council recently updated a whitepaper. [1] This whitepaper presents the charge device model (CDM) specifications and requirements specifically for

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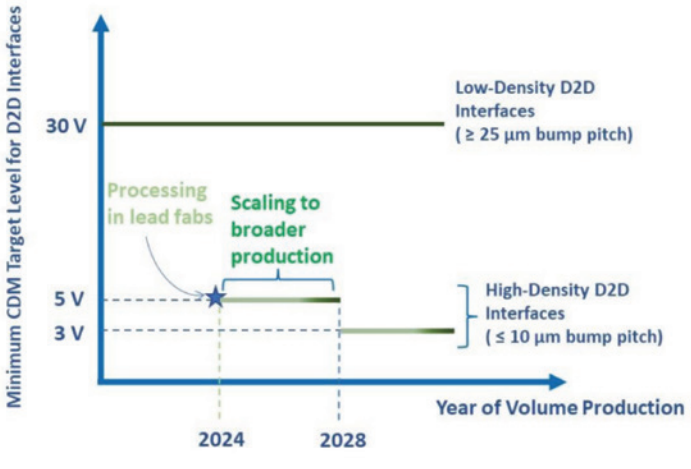

Figure 1: ESD Industry Council "Roadmap of CDM Targets of Die-to-Die Interfaces" [1]

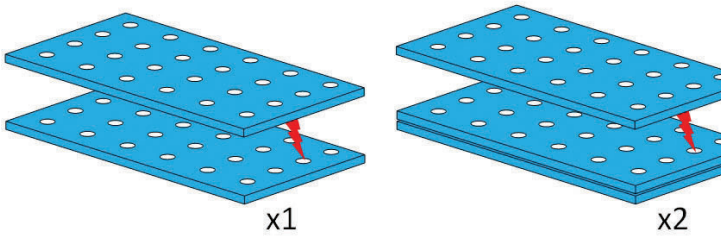

Figure 2: Repetitive ESD stress with multiple die stacking

D2D interfaces. Figure 1, taken directly from the whitepaper, details the future reduction of CDM targets as the density of the D2D interfaces continues to increase. This roadmap is critical for aligning manufacturing ESD levels with the ESD protection at the D2D interfaces.

The increasing number of die stacks presents an additional challenge: the potential for cumulative ESD damage. Figure 2 demonstrates that with multiple die stacks, a repetitive ESD event could occur and propagate through the die interconnect with each die placement.

This repetitive stress, even within the "acceptable" D2D voltages suggested by the white paper, could lead to ESD damage. This damage could be observed with degradation in oxides based on the time dependent dielectric breakdown (TDDB) or with other time-to-fail ESD methods. [2] [3] [4]

The very-fast transmission line pulse (vfTLP) is an ESD tool that we can use to evaluate key elements for on-chip ESD design. With a constant 1ns pulse width at a set voltage, we can increase the number of stresses from a single pulse to a larger stress number to observe the impact of cumulative stresses. Figure 3 demonstrates measured data, showing the reduced performance of stress across a gate oxide and the reduced performance also for the fusing capabilities of metal interconnects.

In conclusion, as with all on-chip ESD designs, there is a delicate balance to maintain. This balance is between supporting the minimum amount of ESD protection to prevent damage during manufacturing and avoiding ESD over-protection, which could lead to speed and silicon area limitations. The white paper provided by the ESD council helps align this balance. However, due to the innovative advancements of the D2D interfaces, special circumstances may need to be considered.

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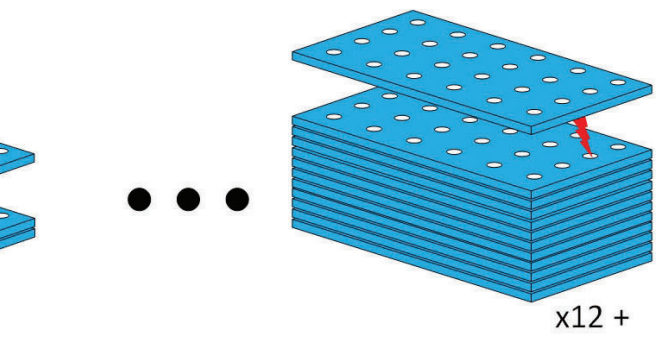

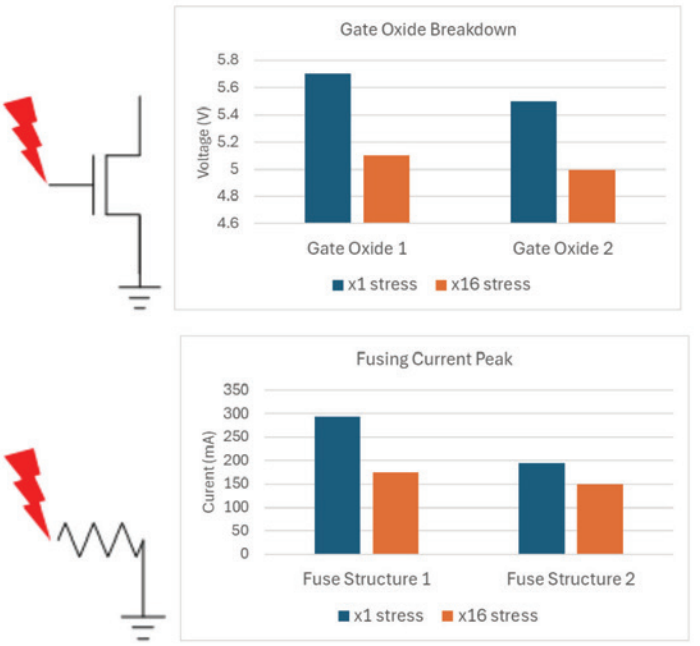

Figure 3: vfTLP repetitive stress impact on gate oxide and metal interconnects

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