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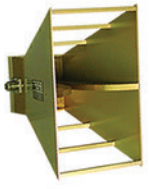

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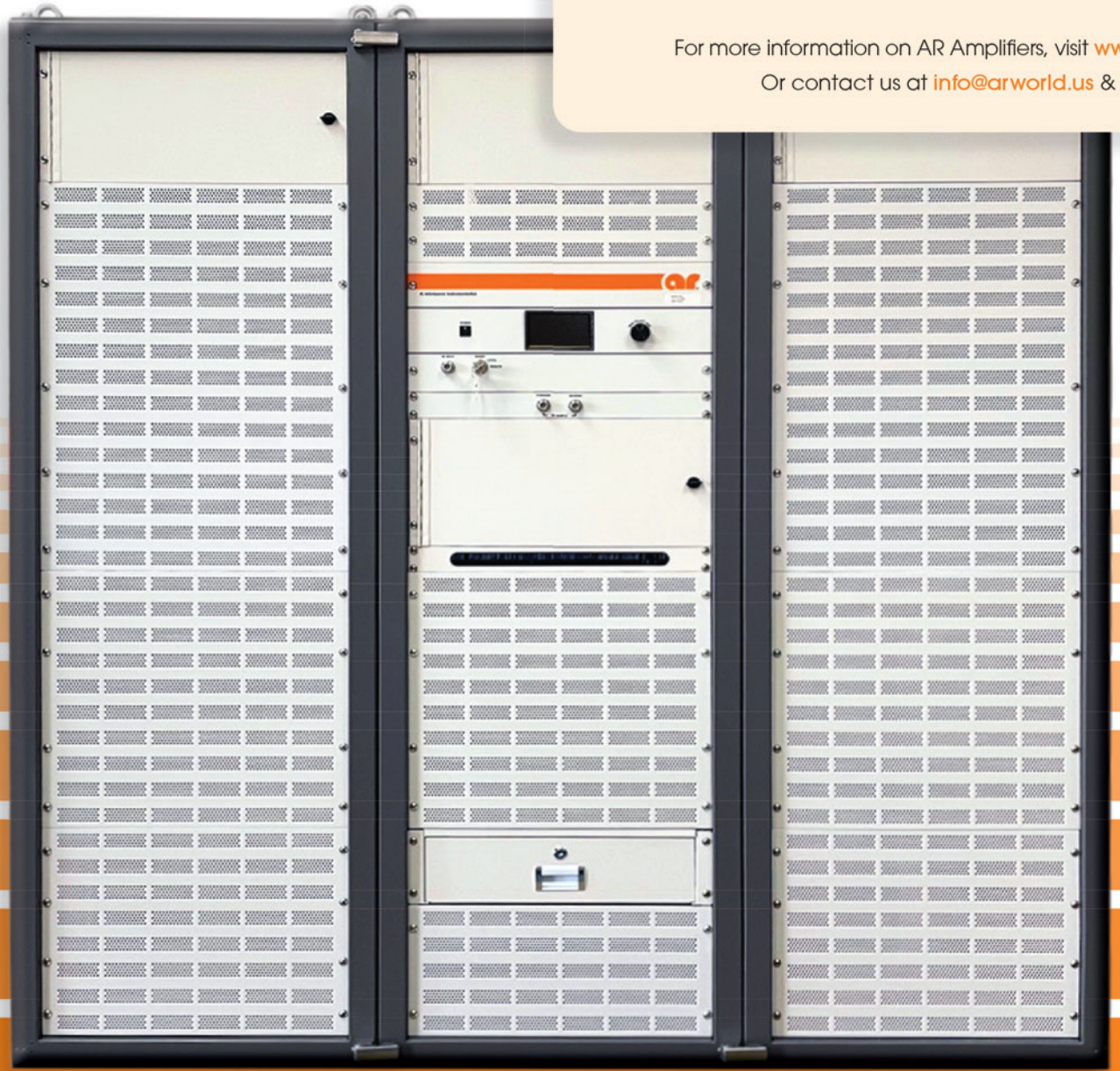

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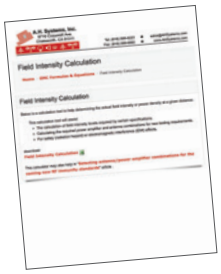

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FCC Affirms $2.3 Million Fine for Pirate Radio Broadcasting

The U.S. Federal Communications Commission (FCC) has affirmed a $2.3 million financial penalty against two brothers for illegal pirate radio broadcasts in Queens, NY.

According to a Forfeiture Order issued by the Commission, Cesar Ayora and his brother Luis Angel Ayora "engaged in the longstanding illicit operation of an unauthorized radio station known as Radio Impacto 2," in violation of the provisions of the Communications Act, and have been ordered to pay $2,316,034.

The Ayoras were originally recipients this past March of a Notice of Apparently Liability for Forfeiture (NAL) in connection with their years-long pirate radio operations, following extensive surveillance by field agents of the New York Office of the FCC's Enforcement Bureau. In that NAL, the Commission calculated a proposed forfeiture of over $21 million but reduced the amount to $2,316,034 based on statutory limits.

However, the Ayoras failed to file a response to the NAL, hence the issuance of the Forfeiture Order.

FDA Issues Guidance on Electronic Submissions of 510(k)s

The U.S. Food and Drug Administration (FDA) has released its final guidance on premarket notification (510(k)) submissions by electronic format.

The Guidance, "Electronic Submission Template for Medical Device 510(k) Submissions," provides a detailed explanation of the structure of the agency's current eSTAR 510(k) electronic submission template, along with a thorough description of the kind of information expected for each individual template listing (e.g., "device description," "consensus standards," "predicates and substantial equivalence," "labeling," etc.).

Where appropriate, the Guidance also lists the applicable standards and other documents that device developers should use in assessing the compliance of their device with the FDA's requirements.

Guidance documents issued by the FDA and other agencies are intended solely to provide insight into the current thinking of regulators and should be viewed only as recommendations and not requirements.

EU Commission Extends Date of Expanded Radio Equipment Requirements

The Commission of the European Union (EU) has extended the effective date of its expanded application of the essential requirements of its Radio Equipment Directive (2014/53/EU, also known as RED).

Published in the *Official Journal of the European Union*, Delegated Regulation (EU) 2023/2444 extends until August 2025 the expanded application of the RED detailed in Delegated Regulation (EU) 2022/30. That Delegated Regulation includes the cybersecurity of internet-connected equipment under the scope of the RED and was originally scheduled to take effect in August 2024.

Internet-connected equipment specifically subject to the provisions of EU 2022/30, includes:

- Radio equipment designed or intended exclusively for childcare;
- Radio equipment covered under the scope of the EU's Directive on the Safety of Toys (2009/48/EC);
- Radio equipment designed or intended to be worn, strapped to, or hung from any part of the human body or incorporated into any clothing worn by humans, such as headwear, hand wear, or footwear;
- Radio equipment that enables the holder or user to transfer money, monetary value, or virtual currency.

Internet-connected equipment expressly not included under the expanded scope of cybersecurity requirements detailed in the draft Delegated Regulation includes medical devices covered under the EU's Medical Device Regulation (EU 2017/745) and the In Vitro Diagnostic Medical Device Regulation (EU 2017/746). Also excluded are internet-connected equipment and devices used in civil aviation applications (EU 2018/1139) and in automotive systems and components (EU 2019/2144).

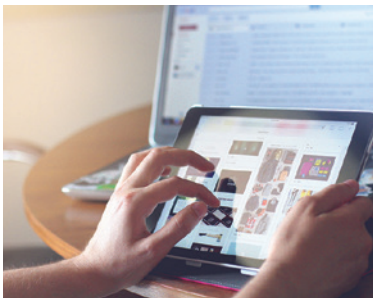
EU Commission Designates Six "Gatekeepers" Under Its Digital Markets Act

The Commission of the European Union (EU) has named six major digital platform companies as "gatekeepers" under the EU's Digital Markets Act (DMA).

According to an EU Commission press release, Alphabet, Amazon, Apple, ByteDance, Meta, and Microsoft have received designations as gatekeepers. The EU defines gatekeepers as large digital platforms providing so-called core platform services, such as online search engines, app stores, and messaging services.

EU-designated gatekeeps are subject to Commission oversight and are required to comply with the obligations and prohibitions detailed in the DMA. Specifically, gatekeepers must:

- Allow third parties to "inter-operate" on the gatekeeper's digital platform;
- Allow business users to access data generated from the use of the gatekeeper's platform;
- Provide companies advertising on their platform with the tools and information necessary to independently verify their advertising hosted by the gatekeeper; and
- Allow businesses to promote their offers outside of the gatekeeper's platform.



- At the same time, gatekeepers cannot:
- Provide preferential treatment to products and services offered by the gatekeeper itself;
- Prevent consumers from linking up to businesses outside of their platforms;
- Prevent users from uninstalling any pre-installed software or app if they wish to do so; and
- Track end users outside of the gatekeeper's platform services without receiving the consent of the end user.

MEASUREMENT UNCERTAINTIES IN OUTDOOR FAR-FIELD ANTENNA RANGES

How to Be Certain About Your Uncertainties

By Dr. Edwin Barry, Pieter Betjes, and Eric Kim

Pieter Betjes holds a Master of Science degree in Electrical Engineering from Delft University of Technology, with a specialization in avionics and RF technology. He has authored and co-authored numerous technical papers throughout his career with Fokker Aircraft B.V., Netherlands Organisation for Applied Scientific Research (TNO), and NSI-MI Technologies. He can reached at pieter.betjes@ametek.com.

Eric Kim holds a Bachelor of Science degree in Mechanical Engineering from Polytechnic University. Eric's career at NSI-MI Technologies includes the development of compact range reflectors, radome test systems, and numerous custom multi-axis positioning systems. Eric has published numerous technical papers developed from his research on highly accurate mechanical positioning systems. He can reached at eric.kim@ametek.com.

Dr. Edwin Barry—See "In Memoriam" at the end of this article.

Since the advent of compact antenna test ranges and, somewhat more recently, near-field antenna test ranges, the number of newly built indoor test facilities has far surpassed the number of outdoor test facilities that have been constructed. Outdoor far-field testing requires suitable real estate, is subject to interference from external transmissions, and requires favorable weather conditions. However, the measurement of very large or very low-frequency antennas sometimes precludes a suitable indoor configuration.

While the antenna measurement methodology for outdoor far-field direct illumination ranges is well established, and there are several references to estimates of specific uncertainty terms [1]-[3], there are no comprehensive recommended practices for the estimation of measurement uncertainty. This is in contrast to the existing recommended practices for near-field [4] and compact antenna range measurements [5].

In this article, we identify key uncertainty terms for an outdoor elevated far-field antenna range and present a procedural methodology for predicting and evaluating the measure of uncertainty. The method for analyzing each term is described in detail in accordance with [6], commonly referred to as the Guide to the Expression of Uncertainty in Measurement (GUM). We then accumulated all uncertainty terms into a single value and present example uncertainty budgets for the antenna's peak gain and -30 dB sidelobe measurements.

RANGE DESCRIPTION AND COORDINATE SYSTEM

The range we considered in this uncertainty analysis has a total range length of R = 1,086 m spanning a valley containing woodland, asphalt roads, and several buildings. The range operates in the antenna under test (AUT) receive configuration. Referencing Figure 1, the height of the transmit source and AUT are h_t = 143 m and h_r = 71 m above the lowest point in the valley floor, respectively. A reference antenna, used to provide a phase reference for the measurement, is co-located just below the AUT. The valley slopes up toward the source and AUT location gradually.

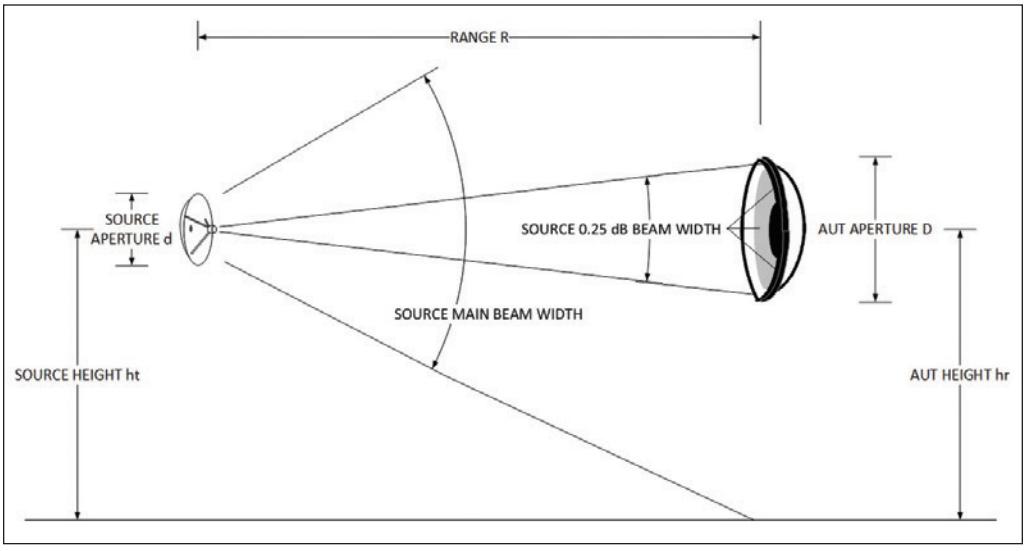


Figure 1: Range Geometry

The source antenna is a 0.935 m linearly polarized parabolic reflector antenna, the AUT is a 1.2 m circularly polarized parabolic reflector, and the frequency of operation for the analysis is 7.5 GHz.

Shown in Figure 2 is the AUT positioner stack-up configured as roll/slide/azimuth/elevation. It allows full polarization control of the AUT as well as translation along the z-axis. The conventional spherical coordinates are used to define the AUT coordinate system, also depicted in Figure 2. Here, the z-axis is defined as perpendicular to the AUT aperture plane, which may or may not coincide with the antenna's electrical boresight.

The source antenna is mounted on a polarization positioner so that it can transmit two orthogonal polarizations for reconstruction of the circularly polarized response of the AUT. The source antenna and source polarization positioner are affixed to a squint mount and positioned such that the z-axis of the source and AUT can be made coincident.

The gain of the AUT is determined using the gain substitution method, where a gain standard antenna with a known gain value (in this case, a calibrated standard gain horn) is used to determine the absolute gain of the AUT. The standard gain horn had previously been calibrated by the manufacturer in a compact antenna test range and had been issued a certificate of calibration.

UNCERTAINTY ANALYSIS AND EXAMPLE

The following assessment leverages the industry standard 18-term analysis for near-field ranges [1], [8], as well as historical and modern literature relevant to far-field and compact range assessments [2], [9].

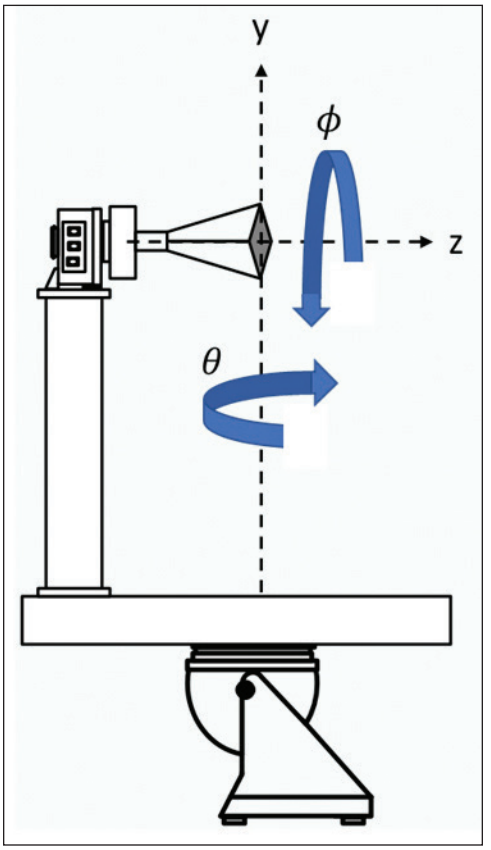


Figure 2: AUT positioner configuration and coordination system

We evaluated each of the identified uncertainty terms by analysis, observation, or measurement for their effect on boresight gain and the -30 dB sidelobe level. Each term is also classified as a Type A or Type B uncertainty, and its relevant divisor assigned such that the standard uncertainties may be combined. Finally, the terms are collected and combined by the root sum squared method, and a coverage factor is assigned to bring the confidence level to 95% (k = 2).

Source Polarization Purity (Type B)

When measuring a circularly polarized AUT with a linearly polarized source antenna, the imperfect axial ratio of the source has a significant impact on the measurement error [5]. On outdoor ranges, it's often desirable to have broadband source antennas with relatively high gain. But this requirement often comes at the expense of source polarization purity.

The source polarization purity term can be estimated using the following equation [2]:

$$U_1 = \frac{1+\rho_w^2\rho_A^2+2\rho_A\rho_w\cos 2\theta}{\left(1+\rho_w^2\right)\left(1+\rho_A^2\right)}$$

where $\rho_\omega = (r_w + 1) / (r_w - 1)$ and $\rho_A = (r_A + 1) / (r_A - 1)$.

Here r_w is the axial ratio of the transmitting antenna, r_A is the axial ratio of the receiving antenna, and θ is the angle between the source and receiving polarization vectors. Assuming an ideal linearly polarized standard gain antenna (SGH), a purely circularly polarized AUT, and a Tx antenna axial ratio of 30 dB, the gain uncertainty can be estimated as ±0.279 / √3 = ±0.161 dB.

AUT Alignment (Type B)

This error term concerns the AUT azimuthal errors with respect to the range axis. Assuming that the AUT

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pattern is approximately parabolic around the 3dB point and using the standard quadratic function, the associated error can be estimated as:

$$U_2 = -3\left(\frac{\theta_{err}}{\theta_{3dB}}\right)^2$$

where θ_{err} is the stated accuracy of the positioner and θ_{3dB} is the 3dB beamwidth of the AUT. This term may also be evaluated experimentally.

Assuming a standard positioner accuracy of 0.03 degrees and an AUT 3 dB beamwidth of 2.5 degrees, the estimated error for this term is approximately ±0.0004 dB and is, therefore, negligible.

Gain Standard (Type B)

This error is due to the gain uncertainty of the standard gain antenna itself and only impacts the gain measurement uncertainty. It is often one of the largest contributors to the total uncertainty budget and can be somewhat mitigated through careful gain calibration. For a typical standard gain horn, the manufacturer's analytical gain curves are accurate to within about ±0.3 dB to ±0.5 dB, which may be sufficient depending on the required value for the total uncertainty budget. Other types of antennas used as gain standards must generally be calibrated in a separate measurement. Common gain calibration types, in order by increasing levels of uncertainty (k = 2):

- 3-antenna extrapolation ranges (~±0.1 dB)
- 3-antenna ranges without extrapolation (~±0.25 dB)
- Substitution method (~±0.5 dB)

The calibration certificate for the range SGH states that the k = 2 uncertainty is, as measured by the manufacturer, ±0.570 dB. Therefore, the standard gain uncertainty for the SGH is U_3 = ±0.285 dB.

Connection Repeatability (Type A)

This error term is due to mating/de-mating the cable connections to the AUT, which may induce errors due to improperly torqued connectors and excessive flexing in the cabling. Care should be taken to properly torque the connectors using a calibrated torque wrench and to avoid unnecessary cable flexure and strain. Still, there will be a small but finite variation in signal level. This error affects the gain but does not affect sidelobe measurements.

The associated uncertainty is estimated by taking ten measurements of the peak of the beam RF signal after de-mating and then mating the cable to the AUT. The standard deviation of the measured signal is the estimate of the gain uncertainty, which we determined to be U_4= ±0.058 dB.

Source and AUT Coupling (Type B)

The coupling between the source antenna and the AUT can be divided into two terms: inductive coupling and mutual coupling. For an outdoor far-field range, the inductive term is generally insignificant unless the AUT is electrically small and the source to AUT separation is approaching the $2D^2/l$ far-field criterion. Likewise, the mutual coupling (or mutual reflection) term, which is due to radiated energy being reflected back and forth between the source and AUT, is typically quite small when the range length is much greater than the size of the source aperture. Nonetheless, both terms will be described below for completeness.

Inductive Coupling

The ratio of the inductive field to the radiating field between the source antenna and AUT is given by [7]:

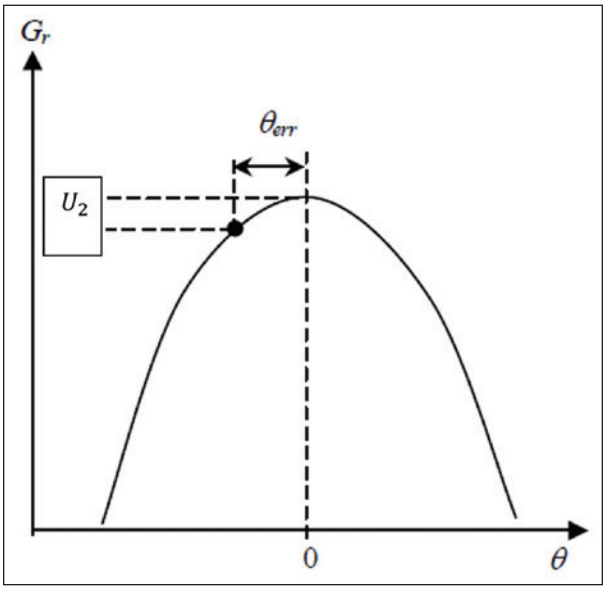

Figure 3: Model for the estimate of Azimuthal errors

Radiation coupling occurs when the receiving antenna re-radiates the transmitted signal back to the source antenna and the source antenna then re-radiates that signal back to the receiving antenna.

$$\rho_{\varepsilon} = \frac{\lambda}{2\pi R}$$

where R is the range length and λ is the wavelength of operation. At 7.5 GHz, with a range length of 1086 m, the stray signal level due to inductive coupling on the considered outdoor far-field range can be estimated at -105 dB and can, therefore, be ignored.

Radiation Coupling

Radiation coupling occurs when the receiving antenna re-radiates the transmitted signal back to the source antenna, and the source antenna then re-radiates that signal back to the receiving antenna. The antenna will re-radiate an amount of energy equivalent to the return loss of the component attached to the antenna terminals. For example, if the VSWR seen by the receiving antenna is 3.0, the return loss will be 6 dB. If the amplitude taper for the source antenna across the AUT aperture is significant, ripples in the main beam of the AUT will be created.

The normal error allocated for this problem is 0.05 dB, meaning that the ratio of the re-radiated signal at the receiving antenna to the original signal should be at least -45 dB. Reference [2] derives the equation for the ratio of the power seen by the AUT from the re-radiated signal from the source antenna to the original power transmitted by the source antenna when both are parabolic reflectors as:

$$\frac{P_r'}{P_r} = k_t k_r \left(0.92 Ú_t Ú_r\right)^2 \left(\frac{\alpha_D}{\theta_s}\right)^4$$

where $\alpha_D = D/R$ is the angle subtended by AUT diameter and:

P_r' = re-radiated power seen by the receiving antenna

P_r = desired power seen by the receiving antenna

k_t = linear value of the reflected signal at the transmit antenna (for example, a return loss of 6 dB is a linear $k = 0.25$)

k_r = linear value of the reflected signal at the receive antenna (for example, a return loss of 6 dB is a linear $k = 0.25$)

$\acute{U}_t$ = efficiency of the transmit antenna = 0.5 (assumed)

$\acute{U}_r$ = efficiency of the receive antenna = 0.5 (assumed)

α_D = the angle subtended at the source antenna by the aperture of the AUT

θ_s = the HPBW of the source antenna

Assuming a 3-degree HPBW for the source antenna, an AUT diameter of 1.2 meters, and antenna efficiencies of 50%, the equivalent stray signal is -92 dB, and, therefore, negligible. The calculation of the coupling term for the gain standard will result in similarly negligible values.

Multipath Reflections (Type A)

Based on the range geometry, it is possible to estimate the effect of specular reflections on gain measurements [2],[3]. The geometry for the analysis is shown in Figure 4.

The path to the AUT via the specular reflection is:

$$R_{reflection} = \left[R^2 + \left(h_r + h_t\right)^2\right]^{1/2}$$

The grazing angle Ψ is given by:

$$\psi = \tan^{-1}\left[\frac{h_r + h_t}{R}\right]$$

Note that the grazing angle should be less than the Brewster angle. The Brewster angle is the incident angle at which energy that is polarized normal to the reflecting surface will have almost no reflection. For air over ground, the Brewster angle is approximately 14 degrees [2].

The range from the source to the center of the specular region is:

$$R_S = \frac{h_t}{\tan\psi}$$

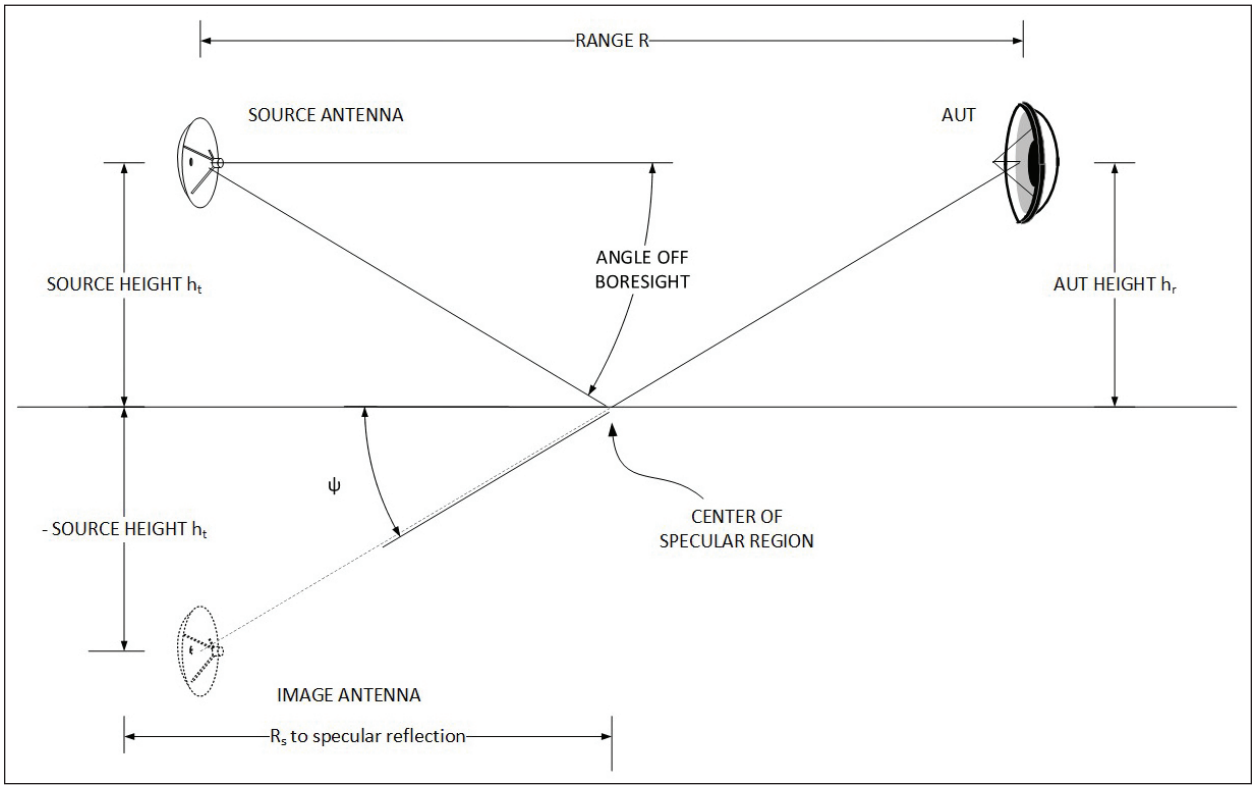

Figure 4: Range geometry for multipath reflection analysis

The magnitude of the specular reflection signal at the AUT represents a stray signal that combines with the direct ray signal that is desired. The reflected signal will be below the desired signal by:

$$10\log_{10}\left(\frac{E_R}{E_D}\right) = dB\ down\ on\ the\ source\ pattern\ @\ \psi$$
$$+20\log_{10}\left(\frac{R}{R_{ref}}\right)+20\log_{10}(k)$$

Here, E_R and E_D are the magnitudes of the direct and reflected signals, and k is the reflection coefficient of the ground. Assuming that the specular region is covered by low grass, a typical value is k = 0.3 [3]. Using this and the geometry of the range, we find the stray signal level to be -41dB, leading to an estimated uncertainty of ±0.080 dB.

While the above analysis gives a useful approximation of the level of uncertainty due to reflections, the real outdoor range surface is far more complicated than the model. There are likely to be several points of reflection that will contribute to the error, along with several types of ground surface. Therefore, we use measurement to establish the reflection contribution.

The example range is equipped with an offset slide along the AUT z-axis. We took measurements as a function of slide position and recorded the maximum to minimum variation of the signal in the quiet zone. Finally, the maximum deviation from the RMS value of the measurement set is used to estimate the error due to reflections. The uncertainty in AUT gain is estimated to be U_{13} = ±0.033 dB, while the uncertainty in the -30 dB sidelobe level is estimated to be ±1.127 dB. When repeated for the gain standard, the measurement set resulted in a gain uncertainty of U_6 = ±0.08 dB and has no effect on the sidelobe levels.

Leakage – (Type A)

Unwanted radiation, usually caused by improperly torqued cable interfaces, broken cables, improperly sealed mixers, multipliers, sources, and isolators, is deemed leakage. Additionally, there can be crosstalk within the RF system itself due to poorly designed internal circuitry that permits leakage. These two terms are tested separately. Internal crosstalk can be measured by terminating the output of the signal source and the input of the receiver and taking a frequency-

dependent sweep. External leakage is first measured by disconnecting the source antenna, terminating the cable, and taking a frequency-dependent sweep. Finally, external leakage on the AUT side can be measured by disconnecting the AUT, terminating the cable, and taking a frequency-dependent sweep. Typical levels should be near the system noise. We estimate the uncertainty in AUT gain to be U_{14} = ±0.000 dB, while the uncertainty in the -30 dB sidelobe level is estimated to be ±0.006 dB. Similarly, the gain uncertainty of the standard gain horn is estimated to be U_7 = ±0.002 dB.

Impedance Mismatch Error (Type B)

Impedance mismatch errors occur because of non-perfect impedance matches between the AUT and its cable network and between the SGH and the same cable network. This term affects the absolute gain measurement only.

The estimated uncertainty may be obtained by evaluating the following equation [10]:

$$U_8(dB) = 20Log_{10}\left(1 \pm \Gamma_{AUT}\Gamma_{Rx}\right) + 20Log_{10}\left(1 \pm \Gamma_{SGH}\Gamma_{Rx}\right)$$

where Γ_{AUT} = 0.126, Γ_{Rx} = 0.130, and Γ_{SGH} = 0.069 are the measured reflection coefficients of the AUT, receiver, and gain standard, respectively. It should be noted that the mismatch uncertainty is different from all other type B uncertainties in that it has a U-shaped distribution, whereas the rest are assumed to be rectangular [11]. The error due to mismatch can, therefore, be calculated as U_8(dB) = 0.222/√2 = ±0.157 dB.

Receiver Amplitude Linearity (Type B)

The non-linearity of modern digital receivers typically has very little impact on the measurement accuracy of an antenna's peak of beam. However, the error induced may become significant when measuring an antenna's low sidelobe levels where the dynamic range is large. The linearity of a receiver is usually given in its manufacturer's specification sheet in units of dB/decade.

The receiver we used in the example test campaign was an MI-750 Advanced Digital Receiver with a stated amplitude linearity of 0.05 dB/10 dB. The effect on the gain uncertainty is assumed to be near zero, while the effect on the -30 dB sidelobe level measurement accuracy can be calculated as (0.05 · 3) /√3 = ±0.157 dB.

Receiver Dynamic Range (Type A)

The dynamic range of the RF subsystem is referred to as the receiver dynamic range in the standard near-field 18-term error analysis. However, it is truly due to a combination of factors, including system cabling, AUT and source antenna gain, attenuation used to mitigate mismatch loss, and the dynamic range of the receiver, and other factors.

Similar to the receiver amplitude linearity, errors for this term tend to be negligible on the peak of the AUT beam and more significant on the sidelobe measurement accuracy. In practice, the RF subsystem dynamic range can be determined by measuring the signal level at the AUT peak of beam, disconnecting the source antenna, and terminating the cable with a 50 Ω load, and comparing the difference between the two signals. The dynamic range was found to be 107.5 dB and, therefore, has almost no impact on the gain uncertainty and only ±0.02 dB on the -30 dB sidelobe levels.

Phase Error (Type B)

The phase error on a far-field range is due to the imperfect "plane wave" impinging on the AUT. There will necessarily be a finite error due to the variation of the phase over the aperture of the AUT. Assuming a flat aperture and using the common criterion of 22.5° of phase variation, the far-field criteria can be found by [1]:

$$R = \frac{2D_{AUT}^2}{\lambda}$$

where R is the range length, λ is the wavelength at the frequency of operation and D_{AUT} is the diameter of the AUT. At 7.5 GHz, the range length is more than 15 times longer than the far-field criterion, and the uncertainty due to phase error can be estimated to be 0 dB for both the gain and -30 dB sidelobe levels.

Random Errors – Environmental Stability (Type A)

This uncertainty term is a combination of all non-repeatable errors due to the receiver, cables, temperature, AUT variations, etc. It is expected that the temperature will vary greatly on an outdoor range and that the source antenna may be subject to movement due to wind loading. Additionally,

scattering due to the dynamics of the forest canopy that covers the valley between the source and AUT is captured in this term.

The most direct way of estimating this quantity is to compare the far-fields of two or more azimuthal scans taken with the exact same scan parameters. Preferably, five or more repeat measurements are performed without any change in the measurement system. The far-field patterns of the repeat measurements are then averaged, and the average is compared to a single measurement by complex plot subtraction. The pattern comparison and the RMS level are then used to determine the estimated uncertainty [7].

In Figure 5, we show the average of five azimuthal cuts, the first of the five patterns, and the pattern subtraction between them. From the RMS of the

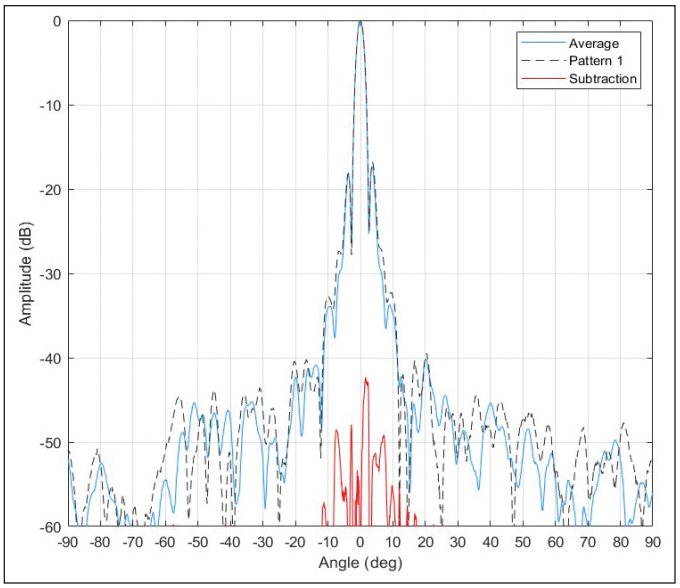

Figure 5: Pattern subtraction for estimation of random errors

pattern subtraction, we estimate error contributions to the gain uncertainty and -30 dB sidelobe levels to be U_{15} = ±0.032 dB and ±0.973 dB, respectively.

Accumulation of Errors

Note that each term above, unless deemed negligible, has been expressed in its standard form. We now use the root sum squared method to combine the terms into a measure of total uncertainty for the gain and sidelobe levels. Strictly speaking, this requires each of the terms to be independent and uncorrelated to the other terms. A coverage factor is also assigned to increase the level of confidence. It's typically recommended that the k is in the range of 2 or 3, giving a 95% or 99% level of confidence, respectively. Here, we choose k = 2 and present the final result in Figure 6.

CONCLUSIONS

In this article, we have described a methodology for identifying and estimating measurement uncertainties in gain and -30 dB sidelobe levels in measurements on an outdoor elevated far-field antenna range. We utilized the industry standard NIST 18-term range assessment technique for near-field ranges as a baseline for the analysis and also considered analysis specific to the range geometry. We also gave specific consideration to assigning the correct divisor to differing uncertainty types to convert the quantities to a standard distribution such that the terms could be correctly combined.

No.	Error Source	Gain Uncertainty (dB)	-30 dB Sidelobe Uncertainty (dB)
1	Source Polarization Purity	0.161	0.000
2	AUT Alignment	0.000	0.000
3	Gain Standard Uncertainty	0.165	0.000
4	Repeatability	0.058	0.000
5	Mutual Coupling - Gain Standard	0.000	0.000
6	Multipath Reflections - Gain Standard	0.080	0.000
7	Leakage - Gain Standard	0.002	0.000
8	Impedance Mismatch	0.157	0.000
9	Receiver Amplitude Linearity	0.000	0.087
10	Receiver Dynamic Range	0.000	0.002
11	Phase Error	0.000	0.000
12	Mutual Coupling	0.000	0.000
13	Multipath Reflections-AUT	0.033	1.127
14	Leakage	0.000	0.006
15	Random Errors	0.032	0.973
	Combined Uncertainty (1σ)	0.299	1.492
	Combined Uncertainty (2σ)	0.599	2.983

Figure 6: Summary of outdoor FF range error sources

IN MEMORIAM

It is with deep sadness that we share Dr. Edwin "Ned" Barry, the lead author of this article, passed away in August 2023.

Ned was a Senior Applications Engineer for NSI-MI Technologies. Ned's thesis title for his Doctorate was "Terahertz Generation in Submicron Nitride-based Semiconductor Devices." Much of the work in his career was spent in antenna design, development, and characterization of antenna performance. In addition to his thesis, Ned was the author or co-author of 9 journal articles and 14 conference papers and presentations.

He was our colleague, friend, and family member. He will be greatly missed.
NSI-MI Technologies

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IT SERVER HARDWARE COMPLIANCE, PART 1

A Detailed Overview of Testing Requirements for Mainframes and Servers

By John Werner, Rebecca Morones, and Arkadiy Tsfasman

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This 2-part series of articles will focus on hardware compliance aspects of specific information technology electronics equipment which includes mainframes, server computers, and subcomponents. In Part 1 of this series, we will provide a technical overview of server components and subcomponents and discuss specifics regarding product safety regulations and testing.

Part 2 of this series will address additional areas of regulatory compliance, including electromagnetic compatibility and environmental concerns. We'll also discuss how IT equipment is tested and certified to compliance standards for worldwide shipments.

The goal of this 2-part series is to provide our readers with a better understanding of the requirements for executing hardware compliance testing and certification, as well as the technical details of every compliance discipline.

TECHNICAL OVERVIEW OF SERVER COMPUTER AND SUBCOMPONENTS

Before diving into the details of each discipline of hardware compliance, it is important to understand the product being tested. This article focuses on the application of hardware compliance to information technology (IT) server computers and their subcomponents, such as processor drawers, input/output (I/O) drawers, cooling subsystems, cryptographic security cards, etc.

A maximally configured server computer with the front doors removed is shown in Figure 1. The mainframe is made up of many subcomponents that fall into one of the following three categories: 1) subcomponents that are designed and manufactured by the information technology (IT) company that will own the end-product; 2) subcomponents designed in partnership with another company who owns the sub-component and that sells it to IT company that will own the end-product; or 3) completely off-the-shelf original equipment manufacturer (OEM) parts.

Figure 1: Maximally configured mainframe with front doors removed

Figure 2 shows a breakdown of the subcomponents within a single rack air-cooled server.

The system in Figure 2 contains two processor drawers, three (IO) drawers, two one-rack unit (1U) servers that manage the built-in service network, and two Ethernet switches that support communications between subcomponents for the built-in service network. Each of these subcomponents contains anywhere from one to four power supply units (PSUs), which take single-phase input within a rated range of 200Vac to 240Vac RMS. In addition to the processors themselves, the processor drawers contain memory and I/O cards to communicate with either other processor drawers or I/O drawers.

The I/O drawers support multiple different I/O cards that support different communication protocols (e.g., ethernet, fiber optics, etc.) to communicate with the outside world. The server also contains four power distribution units (PDUs) that contain connectors where users can supply power to the system from their facility. The power provided to each of the four PDU inputs can be 200Vac to 240Vac single-phase, 380Vac to 415Vac three-phase wye, or 200Vac to 240Vac three-phase delta power. The PDUs convert the input to a 200Vac to 240Vac single-phase output which is then distributed via internal cables to the PSUs. The PDUs are redundant, meaning that the server can run on half the PDUs, ensuring that the system continues to run if a PDU fails, a cable is unplugged or fails, or a power feed is lost that supplies power to the PDUs.

AN OVERVIEW OF REGULATORY COMPLIANCE

Typically, when describing regulatory hardware compliance, it is good to start with the result of hardware compliance work, that is, a compliance label

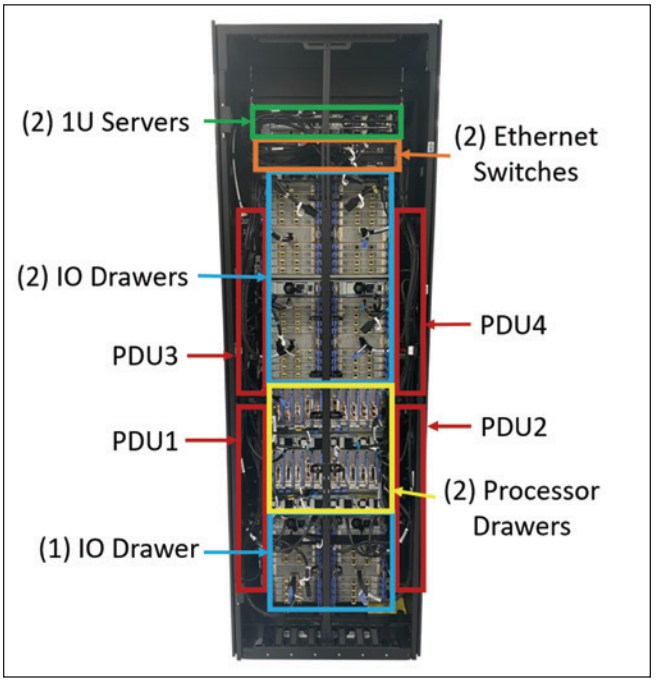


Figure 2: Rear view of the subcomponents within a single rack air-cooled server

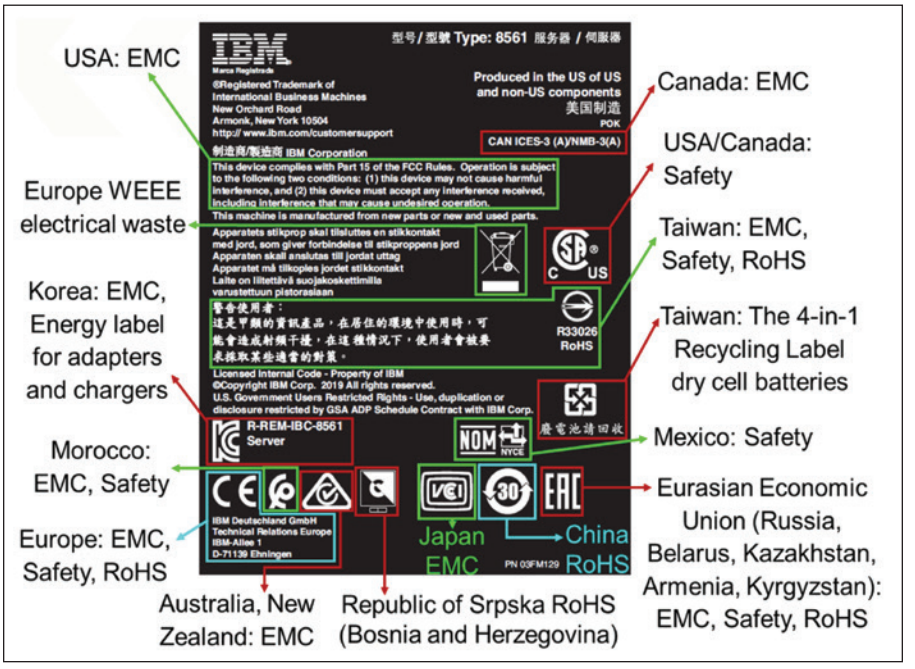


Figure 3: Hardware compliance label

with many certification marks as shown in Figure 3. Such compliance labels can be viewed as a "passport" that allows products to be sold around the world when they are determined to be compliant with local regulations. Just about any electronic product or its packaging includes one of these labels. Figure 3 shows an example of an IBM agency system-level compliance label with several of these marks.

Each of these mini graphic symbols (marks) indicates that the product has been tested and certified that it meets/complies with specific country requirements in the areas of product safety (e.g., doesn't exceed the current rating of a power cord), electromagnetic compatibility (e.g., doesn't interfere with nearby devices), and environmental compliance (reduction of hazardous materials). The scope of certifications around the world is partially determined by voltage rating or power consumption, and the agency marks that appear on a compliance label are not going to be universal for all the products. In addition, marks on the label often need to be changed as regulators in various countries and jurisdictions change laws.

Marks can also be displayed differently for each product. Some products list agency marks either on the packaging, supplied documents (manuals), or via the product software/firmware (i.e., smartphones, smaller electronic devices).

To legally display the marks shown on the compliance label, a product needs to successfully comply with specific regulations and standards. Most countries around the world regulate products for adherence to industry standards for product safety, electromagnetic compatibility (EMC), and environmental characteristics. Compliance testing laboratories perform tests required by regulatory agencies or industry standards as shown in Figure 4 on page 24. Regulatory product certification for ship support requires that internal company testing and reports be submitted to external product safety and EMC agencies for full worldwide country certification. Some companies have the ability to self-certify while others use third-party companies for certification. For instance, for some companies the U.S. and the European Union (EU) allow parties to self-certify EMC compliance, which can help to significantly shorten the certification process.

The job of hardware compliance is to ensure that products meet regulations that allow them to be marketed and sold around the world, but also to uphold the company's reputation, protect it from litigation, and avoid fines. Compliance also helps to protect product service and installation professionals and end users from injury or death. Further, it helps to improve quality, enhance customer satisfaction, reduce the cost of product damage during transit, and protect the environment.

INTEGRATING COMPLIANCE TESTING INTO THE PRODUCT DEVELOPMENT PROCESS

Compliance testing needs to be integrated into the development stage of a product. All compliance testing is the gateway for approval or certification before the products move onto the next phase of development and are eventually released to the market. While each company might approach compliance differently whether they have in-house compliance personnel or go to an independent third-party testing organization, they still must do compliance testing.

Precompliance Evaluation

Many times, compliance personnel are involved in hardware development discussions because they need to determine what needs to be tested. Compliance technical leads define the test and/or certification milestones and communicate this not only to the development engineers but more importantly to executives for utilizing test metrics. The pre-compliance evaluations may include software simulations and early user hardware testing, all with the goal of identifying and eliminating issues and/or problems with the hardware prior to the final stages of testing.

Even with pre-evaluations, products still need to go through the final compliance stage prior to the release. This final stage is where the approvals and the certifications are obtained for the product so it can ship globally. The final stages of testing include minimum ship-level hardware testing (hardware being used by a potential client). Material declarations are obtained in this stage to ensure they need environmental compliance. Component vendor safety certifications are also obtained during this stage to figure out if there will be any issues prior to shipping. Once all the final stage compliance requirements are met, the product is allowed to go to market.

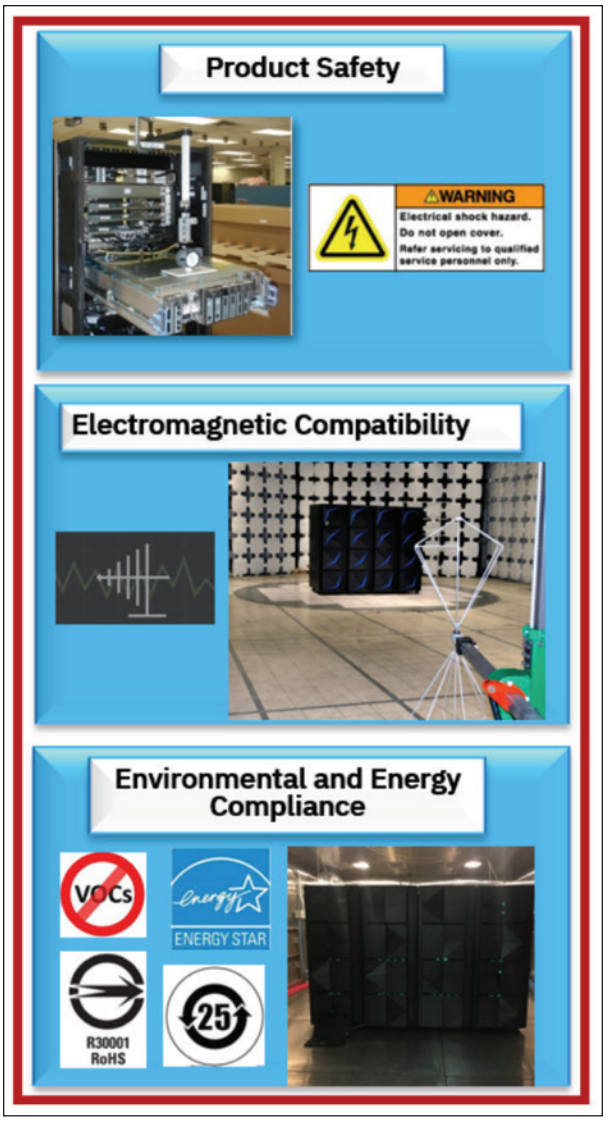


Figure 4: Example of compliance disciplines

Hardware Evaluation

Evaluating hardware early in the design process and obtaining information on a given product is not only quite a bit of work but carries with it the cost associated with compliance testing. There is always a fine balance between the need to test, what to test, and when to test it. Ultimately, the decisions are defined by the compliance groups and developed based on experience and engineering judgment.

Another defining cost for compliance work is finding a balance between obtaining the minimum ship-level hardware for testing while still securing

the certifications and testing approvals needed to ship the hardware globally. Each compliance test has different requirements that drive the hardware needed for testing and its associated cost. Each of these aspects will be further defined in the rest of this article. Ultimately, EMC requires all configurations to be tested, while Product Safety testing and volatile organic compounds (VOC) emissions testing require worst-case maximum configuration. However, VOC emissions testing needs brand-new hardware, while Product Safety testing can use hardware that has run-time hours on it. There is always a balance in the corporate world between the cost of the hardware and scheduling all the hardware compliance testing required to meet ship support dates.

The Cost of Compliance

The cost of compliance can be broken down into two cost types: capital and expense. Capital costs include necessary tools for testing, such as test chambers, software for regulatory tracking, or databases for tracking all the compliance work. There is also the capital cost associated with headcount. All compliance work must have proper staffing to meet ship support dates. When there are a lot of systems being released and compliance testing such as EMC must test each configuration, there needs to be the right number of staff to get all of this done.

Other costs include costs associated with test equipment calibration, especially when the compliance testing laboratories are ISO/IEC 17025:2017 accredited. This also includes the cost of the accreditation and all the activities associated with it. Some companies' expenses can also be attributed to external compliance testing. Each company must determine what schedule and cost work best for their product release cycle.

Aligning Product Release Plans and Compliance Efforts

One might wonder how the compliance test schedule works within the development cycle and is still completed prior to the product's release to the market. Compliance engineers learn of scheduled product launch dates from their company. With this information in hand, engineers can establish a staged testing schedule to align with those dates. In some cases, product release schedules are staged geographically, allowing test engineers to conduct required testing in phases.

For these reasons, compliance engineers need to be familiar with the regulatory activity by geography and know what tests are required for those geographies. Effective scheduling also requires internal coordination of the compliance testing sequence. For example, certain tests, such as VOC testing, must be conducted with brand-new hardware, so they must be scheduled before any other testing that uses the same equipment.

TESTING FOR PRODUCT SAFETY COMPLIANCE

Product safety hardware compliance testing is a crucial step in the development and manufacturing of any product that incorporates electronic components such as servers and subcomponents. Product safety testing ensures that products meet the required safety standards and regulations, protecting users from potential hazards and reducing the risk of liability for manufacturers.

Applicable Standards

Both servers and their subcomponents fall under the category of information and communication technology (ICT) equipment and are subject to meeting the requirements of multiple standards. As of the writing of this article, the product being certified (either the server or a subcomponent) typically needs to meet the requirements of IEC 60950-1, Information Technology Equipment – Safety – Part 1: General Requirements, as well as both the 2nd and 3rd Editions of IEC 62368-1, Audio/Video Information and Communication Technology Equipment – Part 1: Safety Requirements, with all amendments and country deviations. Compliance with more rigorous standards may be necessary to meet the requirements of a nationally recognized test laboratory (NRTL) such as UL, CSA, or TUV to facilitate regulatory approval in jurisdictions around the world. Even more rigorous testing requirements may be implemented by original equipment manufacturers (OEMs) to ensure the highest possible level of safety.

The specific tests required by each standard are similar, but testing limits can vary from standard to standard. To ensure compliance with all the standards, a superset of worst-case test limits is typically utilized for each test case; a server or subcomponent that meets the worst-case limits of all of the applicable standards is best positioned to meet the requirements in any regulatory jurisdiction.

Product safety compliance efforts begin during the earliest development stages of the server. Because of the potential costs and scheduling changes that can result from non-compliant hardware, it is incumbent on the product safety engineer to attend design meetings and to review both electrical and mechanical designs as early in the development process as possible, and provide feedback for design improvements that will ensure the final design passes all the requirements of the standards.

Some of the early work includes: 1) reviewing prints; 2) reviewing electrical schematics to ensure any power outputs are current-limited; 3) reviewing printed circuit board (PCB) layouts to ensure proper spacing of components (e.g., creepage and clearance distances); 4) reviewing 3D mechanical CAD models and/or early mechanically-good hardware for access to energized parts, hazardous moving parts, and sharp edges; 5) reviewing thermal simulation data to identify locations that may exceed touch temperature limits (potential burn hazards) or critical components that may exceed their operating limits and could result in smoke or fire, and 6) reviewing the overall grounding scheme of the server or subcomponent.

Product Configuration Considerations

There are many configurations offered for each server or server subcomponent. Customers can choose a desired I/O configuration, memory configuration, or processor configuration, as well as many other options that will result in different components being installed into their chosen customized system. Therefore, when hardware is available for safety tests, it is important that the correct configuration is selected for testing.

Each test within the product safety standards requires that the product is tested in the most unfavorable scenario of normal use.

For server subcomponents, the safety engineer must consider the worst-case configuration for that subcomponent, which may not match the configuration for that same subcomponent when implemented within a fully configured server. The subcomponent may be over-tested (e.g., tested in a higher room ambient temperature, utilizing fan speeds that are suboptimal for each test, etc.) which provides some buffer against failure when that same subcomponent is installed in a server during system-level product safety testing. For server-level product safety testing, the maximum system configuration is selected for testing which includes the highest number of processor drawers, I/O drawers, PDUs, and server racks.

Types of Product Safety Testing

Some of the product safety tests that are required to be performed on a server or subcomponent include steady force, accessibility to electrical energy sources and safeguards, electric strength, capacitor discharge after disconnection of a connector, the resistance of the protective bonding system, prospective touch voltage, touch current measurements, sharp edge testing, accessibility to moving parts, stability testing, input testing, normal operating conditions temperature measurements, and simulated abnormal and fault conditions testing. The following sections provide details on each of those types of tests.

Steady Force Testing

Steady force testing requires the safety engineer to push on mechanical enclosures and barriers or parts mounted on a PCB with a specified force (e.g., between 10N and 250N, depending upon the location) to ensure that electrical insulation is not bridged or hazardous energy sources do not become accessible.

To assess accessibility to electrical energy sources and safeguards, the test engineer uses a test finger instrument and applies that to all user-accessible areas to determine if a part of a specific current, voltage, or power level can be touched. During this test, the engineer can remove any door, cover, or component that does not require a specialized tool to gain access. The same test finger instrument is used to evaluate

accessibility to moving parts. Here, the test engineer determines if the instrument can access components such as a moving fan blade or pump motor.

Sharp Edge Testing

A sharp edge test determines if any sides, edges, or corners of the server or subcomponent are sharp enough to injure a user. A sharp-edge test instrument is used that applies a specific force to a tape head that is slid across the area of concern. Any location that cuts through two layers of tape on the tape head results in a test failure, and the manufacturing process must be reviewed and modified as necessary to ensure that the location is rounded or smoothed.

Stability Testing

Stability testing requires the test engineer to place each rack of the server on a tilt table and then place the table at an angle of 10 degrees for one minute. Should the rack tip over on any side, it fails the test. The test engineer must ensure that the system is configured in the worst-case allowable configuration that may induce tilting (i.e., the most top-heavy configuration).

Capacitor discharge after disconnecting a connector requires the test engineer to measure the capacitance present at the input pins to the PDU (at the system level) or power supply unit (PSU) (at the component level) to ensure that the voltage reduces to a safe level within a given amount of time (e.g., 2 seconds).

Electric Strength Testing

Electric strength testing requires the test engineer to apply a high voltage (typically around 2500V) across parts for one minute to test the effectiveness of the insulation (e.g., air gap, FR4, etc.). If there is a sudden breakdown of the insulation material that allows current to flow between the parts, the insulation poses a shock hazard and is deemed to have failed.

Resistance of the Protective Bonding System Testing

Resistance of the protective bonding system requires the test engineer to apply a high current to the equipment, double the current rating of the minimum required upstream breaker (e.g., test current could be as high as 126A on a server) between the input connector ground pin of the PDU or PSU and the grounded chassis of each component, and measure the resistance across those two points. The voltage drop is then calculated and must not exceed 2.5V. This ensures that, if a fault were to happen in the system that put voltage on the grounded system chassis, a path exists for that current to reach the input power cord and make its way back to and flip the upstream breaker, such that a user would not be exposed to that voltage if they touched the server or subcomponent chassis.

Prospective Touch Voltage, Touch Current, and Protective Conductor Current Testing

Prospective touch voltage and touch current are measurements of the voltage and current that flow through the human body when a person touches the server or subcomponent and another ground location that may be present in the data center. These measurements are made under normal and fault conditions, but the worst-case measurement is typically obtained when a fault simulating the loss of the ground connector on the power cord is tested. In this scenario, any leakage current present on the chassis of the server or subcomponent now flows

Figure 5: Touch current test

through a person. A touch current network is used to obtain a measurement that simulates the impedance of the human body. The touch current and touch voltage obtained must be below a level specified in the standard to be deemed a passing result.

Figure 5 shows an image of a safety engineer performing a touch current measurement.

Input Testing

Input testing ensures that the server or subcomponent does not exceed its rated input current. For this test, the system power is maximized. The maximum configuration is tested with the highest power I/O cards and memory DIMMs installed, and the cooling fans and pumps are set to their highest supported speeds. The system or subcomponent is then tested in the highest supported ambient temperature (e.g., 40°C), and an exerciser is executed on the system that simulates the high end of a customer workload.

The system can also operate in a condition known as N-mode. The power subsystem is designed for full redundancy, meaning that there are twice as many PDUs and PSUs as required such that if a failure happens in the field, the system will continue to run. N-mode is the minimum number of PDUs or PSUs required before functionality is lost and the system or subcomponent goes down.

Input measurements are made under normal and N-mode conditions at the ends of the rated voltage ranges, common voltages used in specific countries around the world, and tolerance voltages 10% above and 10% below the rated voltage ranges. Worst-case measurements are obtained during N-mode testing because the total power required to run the server or subcomponent is divided between a smaller number of PDUs or PSUs. The testing ensures that the measured current at all these voltage and configuration permutations does not exceed the input rating of the server or subcomponent.

Normal Operating Conditions Temperature Testing

Measurements of temperatures under normal operating conditions are made to ensure that components do not exceed their operational limits, which could result in smoke or fire incidents, and that locations that can be touched do not exceed temperature limits that could cause burns or cause a user to hurt or shock themselves due to an involuntary action where they pull their hand away from a hot location.

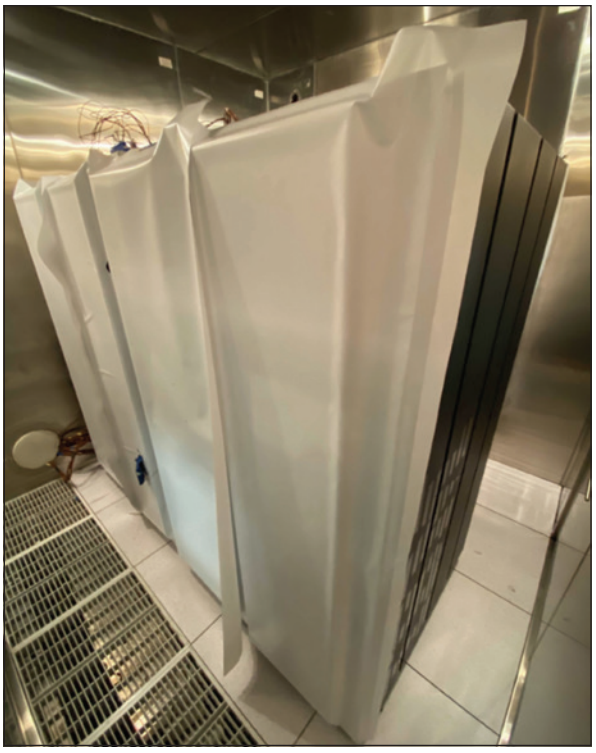


Figure 6: Blocked ventilation test

To perform this testing, thermocouples are attached to safety-critical components and common touch locations. The maximum configuration is then tested with the highest power I/O cards and memory DIMMs installed, the system or subcomponent is tested in the highest supported ambient temperature (e.g., 40°C), the cooling fans and pumps are set to perform as they normally would in the current ambient condition and may be set to an even lower speed for subcomponents to provide buffer when that subcomponent is tested at the system level, and an exerciser is executed on the system that simulates the high end of a customer workload. Tests are executed at multiple voltage setpoints, including at the ends of the rated voltage ranges, common voltages used in specific countries around the world, and at tolerance voltages 10% above and 10% below the rated voltage ranges. Each test lasts a minimum of 1 hour or until temperatures on all thermocouples reach equilibrium.

Abnormal and Fault Conditions Testing

Simulated abnormal and fault conditions testing is very similar to normal operating conditions temperature testing except that a single abnormal or fault is introduced and tested one at a time. Abnormal and fault conditions include fan failure, power supply failure, blocked ventilation, loss of cooling water flow, pressure testing, and reverse polarity testing.

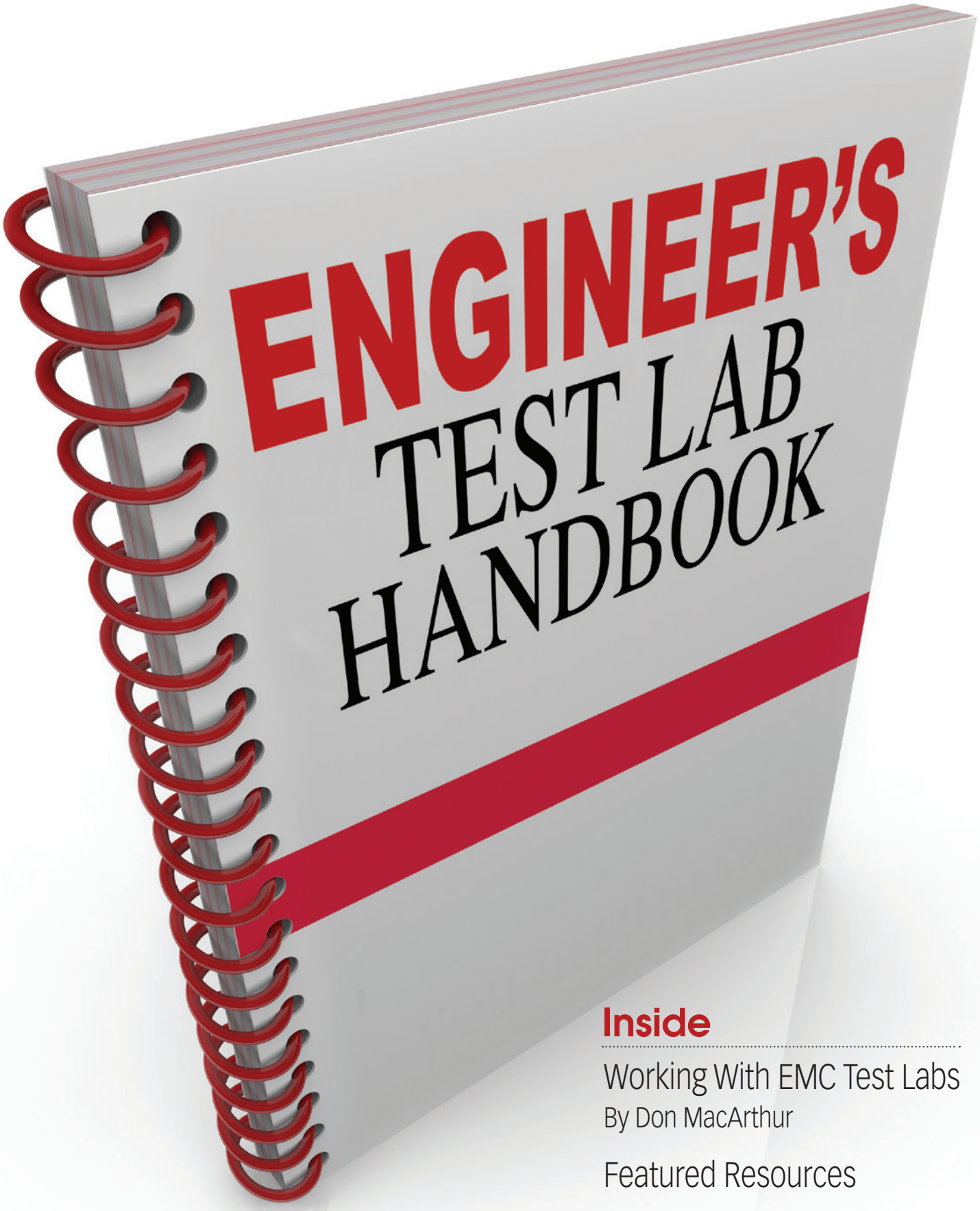
An example of a blocked ventilation test is shown in Figure 6.

In addition to monitoring temperatures of all the thermocouple locations, the system or subcomponent behavior is monitored to record changes to fan speeds, a shutdown of components or the system, pressure increases, increases in current or power, etc. This testing determines if a safety concern could arise if there is a single fault, so it is acceptable for the system or subcomponent to shut down during testing if it shuts down in a way that does not introduce a safety concern.

In conclusion, product safety testing is a critical aspect of hardware compliance that evaluates a product's electrical components to ensure they meet safety standards and regulations. By conducting product safety testing, manufacturers can ensure that their products are safe for use and that they meet the applicable safety standards. It also protects against foreseeable misuse, helping to ensure the safety of clients, support engineers, and anyone exposed to a product.

SUMMARY

In this article, we've provided a technical overview of server components and subcomponents, the process of integrating compliance testing into the product development process, and details regarding the various types of product safety testing. In Part 2 of this series, we'll address additional areas of regulatory compliance, including electromagnetic compatibility and environmental concerns. We'll also discuss how IT equipment is tested and certified to compliance standards for worldwide shipments.



Inside

WORKING WITH EMC TEST LABS

What Every Electronics Engineer Needs to Know

Don MacArthur is a Guest Contributor to *In Compliance Magazine*. He has over 30 years of experience in product development, EMC, testing, and product safety compliance. He has developed products for military, commercial, and industrial applications. He can be reached at don_macarthur@live.com.

By Don MacArthur

Choosing an EMC test lab to work with is one of the most important decisions any electronics design engineer or product developer must make. Selecting the wrong EMC test lab could mean non-acceptance of test reports, incorrectly performed tests and associated added rework, inability to sell product into specific countries, late product launches, excessive test budgets, added liability, added overhead, and other headaches that are usually associated with inefficient test and certification processes. With this background in mind, this article will quickly highlight what every engineer can do to ensure they select the best EMC test lab to work with.

PRE-COMPLIANCE TESTING

Before we get started, here is a quick note about the importance of performing pre-compliance testing early in the product development cycle. Taking your product out to a third-party test facility is expensive and time-consuming. Often it is the last step in the product development process to occur before production units can ship. Now is not the time to find out if your product fails radiated emissions or some other EMC test. To solve EMI problems during this late stage of the product development program, the available techniques are few, and their relative costs are high. Think about going to the EMC test lab to pass, not to fail. This means performing some kind of pre-compliance testing very early in the program to ensure a higher probability of passing formal EMC qualification tests when the time comes. Setting up an internal pre-compliance testing capability is not that hard or expensive. There are several resources available out there that can get you pointed in the right direction, and Reference 1, described at the end of this article, is one that is highly recommended.

ACCREDITATION

Determine if you need to use an accredited EMC test lab. Sometimes this will be driven by your customer and other times by the type of approval you need to ship your product legally. For instance, under the Code of Federal Regulations, Title 47, Chapter I, Subchapter A, Part 2, Subpart J, Section 2.948, the FCC requires that equipment authorized under the certification procedure be tested at an FCC-recognized accredited testing laboratory with the appropriate scope of accreditation (meaning the tests you need

Some important items to consider when selecting an EMC test lab to work with include things like turnaround times for reports, technical expertise, cost, layout of the facilities and accommodations, responsiveness to requests for quotes, and thoroughness of quotes.

to be performed are included on the lab's scope of accreditation). For equipment authorized using the Supplier's Declaration of Conformity (SDoC) procedure, it is not necessary to perform the testing at an FCC-recognized accredited testing laboratory if that is the route you need to take; however, an accredited testing laboratory may be used if desired. Be sure to check if accreditation is required and, if so, that the EMC test lab is properly accredited. A list of FCC-recognized accredited testing laboratories is provided on the FCC website. [2]

Take note that just because a test lab is accredited does not necessarily mean they are going to be a perfect EMC test solution provider. It's not that accreditation is meaningless, it does establish that a test lab has met certain credentials and qualifications, but it doesn't make it clear whether any particular test lab will be a good fit for you and your particular EMC testing needs.

OVERALL CONSIDERATIONS

Some other important items to consider when selecting an EMC test lab to work with include things like turnaround times for reports, technical expertise, cost, layout of the facilities and accommodations, responsiveness to requests for quotes, and thoroughness of quotes.

Look for other services the test lab may be able to provide that may also save you time and money, such as their ability to act as an FCC telecommunication certification body (TCB) for the U.S. or as a Notified Body for the European Union's EMC Directive, should you require those services.

Perhaps you want to also perform other non-EMC tests like environmental, enclosure protection testing (IP Code), salt fog, safety, vibration, etc. at their facility instead of sending your device out to many laboratories. Just be sure the test lab can perform these other tests as well as they can their EMC tests.

It might be a good idea to visit the test lab and perform a mini quality audit. Ask about their typical test report turnaround times. Good labs should be able to have a test report back to you in less than two weeks. I have seen test reports completed as fast as a few hours and as long as a few months!

The test lab should have experts on staff who can help diagnose and suggest design improvements should the product fail. Make sure you're not just getting button pushers who do not thoroughly understand the purpose of the test and what to look for if test anomalies arise. A good EMC test technician or engineer will be able to quickly recognize when something goes wrong with a test and when to take appropriate action. A person trained to just push buttons won't be able to recognize the difference between a good and a bad test and over or under testing. A quality check should be performed prior to the start of any test to confirm test equipment is operating correctly and that the test setup is sound. This is a very important step in the test process. While you're there, ask if they have ever had to repeat testing because they found out later that it was performed incorrectly. You can ask for training records to see how properly trained their staff is.

Look at their facilities and see if it is well-organized or cluttered. If it's a cluttered environment, most likely, they are disorganized, and you will have to spend extra effort managing the test lab and your device as it goes through testing.

Check equipment calibration certificates. If they are an accredited lab, the equipment calibration certificates should be up-to-date and come from accredited calibration service providers as well.

Some test labs subcontract out some of their testing to other test labs. Be sure to ask about this if it is important to you. You don't want to show up at one location expecting to run all tests in that one location only to find out you need to visit some other facility to witness all tests. This will especially be the case if you ask the lab to perform other types of tests besides just EMC.

Ask to see how they capture customer complaints and look at a few of them. See if they have implemented actions to correct any deficiencies. They should have a process for handling customer complaints.

Finally, if your equipment under test has unique power, size, filter, or other non-standard requirements, make sure the test lab can accommodate these unique needs. There is nothing worse than going through the entire quoting and scheduling process only to find out on the day of planned testing that the test lab does not have the correct accommodations to properly test your device. When all else fails, remember the quote from Benjamin Franklin that "An ounce of planning is worth a pound of cure."

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3. Eadie, A., "How to Choose the Best EMC Test Lab," *EMC FastPass*.
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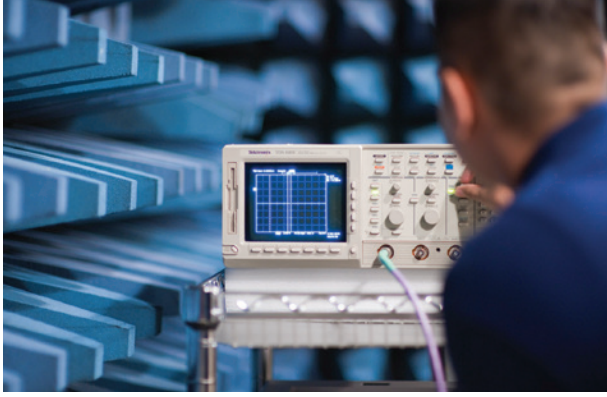

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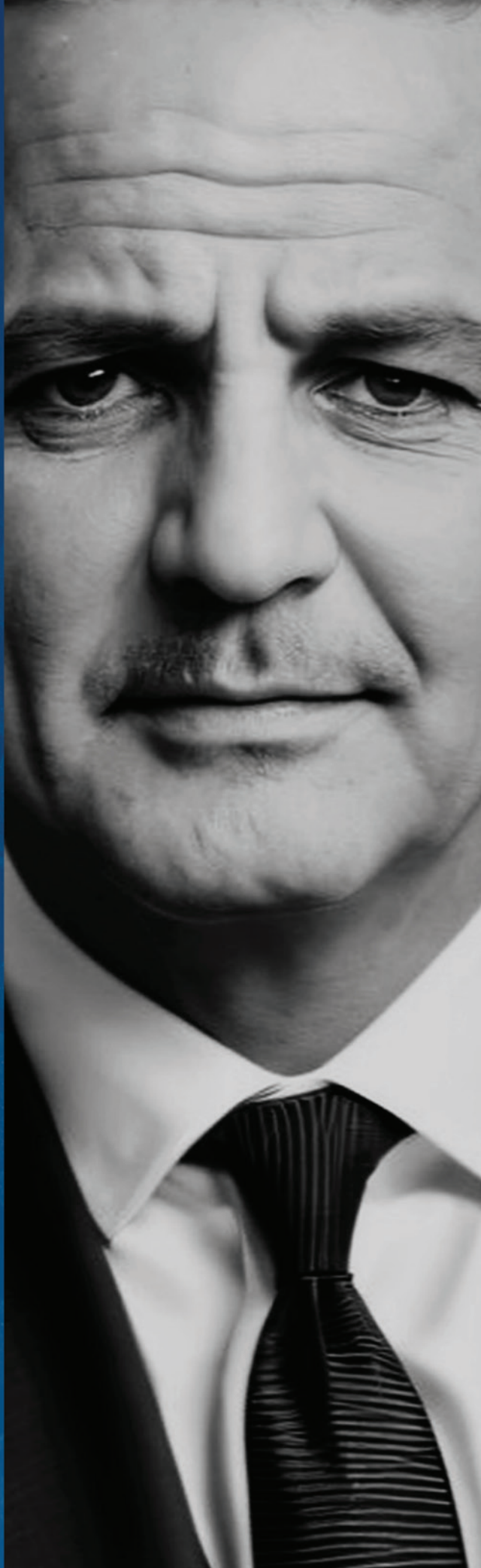

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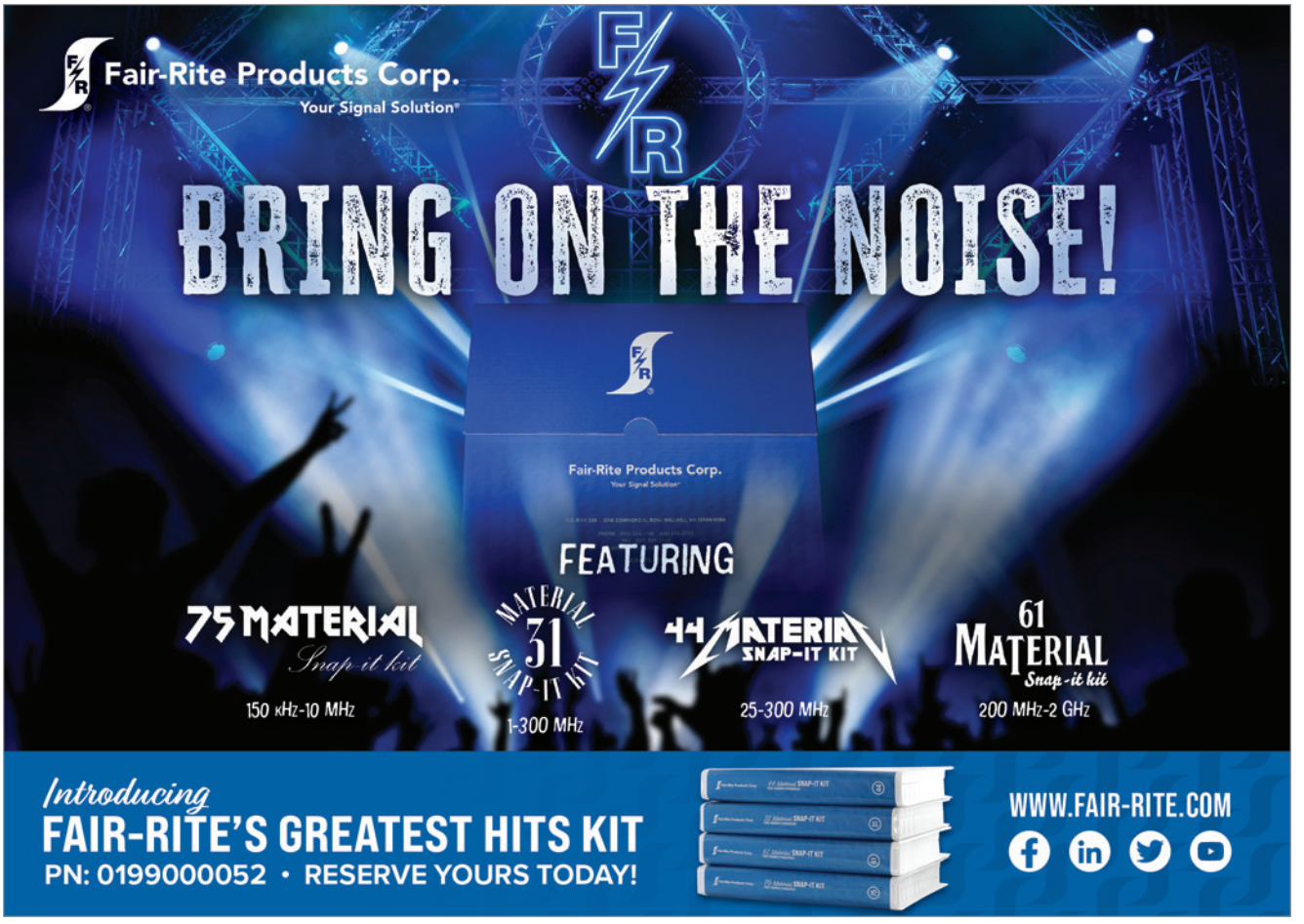

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ESD DESIGNERS' HEADACHE WITH MULTIPLE AUTOMOTIVE TEST REQUIREMENTS, PART 2

A Review of ESD-EMC Co-Design Challenges

In Part 1 of this article (see *In Compliance Magazine*, May 2023), we showed that the trend of progressively migrating both ESD and EMC immunity from the system/board level to the component level is creating unprecedented challenges for the component ESD designer. We reviewed the implications of EMC-ESD Immunity co-design, along with several case studies.

With the unavoidable re-purposing of the system-level standards to validate component-level robustness (IEC 61000-4-2 [1], ISO 10605 [2]), several gaps at the standards level place ESD engineers in the awkward position of creating their own standards. Even worse, the practice of reporting system-level performance in components datasheets is completely dependent on each ESD engineer's interpretation of the standards, hence making those specs of questionable value.

Part 2 of this article focuses on the specific ESD design challenges stemming from the fact that all relevant system-level standards were created to validate systems and not components.

By Gianluca Boselli and Hans Kunz

Dr. Gianluca Boselli is the manager of the corporate ESD Team at Texas Instruments. Boselli has authored and presented numerous papers about ESD and latch-up. He has also served in multiple leadership positions in EOS/ESD Association, as President in 2018-2019 and currently as a member of the Association's Board of Directors. Boselli can be reached at g-boselli@ti.com.

Hans Kunz is a Senior Member of the Technical Staff at Texas Instruments and is currently focused on the development of ESD verification tools and methodologies. Kunz has been a member of the EOS/ESD Symposium Technical Program Committee since 2007. He is also the co-author of multiple publications related to ESD and received the Best Presentation Award for the 2006 EOS/ESD Symposium. Kunz can be reached at hkunz@ti.com.

To rigorously assess the impact of the setup differences detailed in the previously mentioned standards, we offer the circuit analog shown in Figure 1. Each major component of the testing setup is included as a circuit element and the impact of those elements allowed variation to the entire circuit performance that can then be assessed. The specific components of the analog are the ESD generator (or, colloquially, ESD gun), the impedance coupling between the ESD gun and the target/DUT, the target/DUT, and the ground return path between the ESD gun and the target/DUT.

IEC GUN

The calibration current waveform presented in IEC 61000-4-2 [1] has become the *de facto* specification for system-level ESD (Figure 2). It defines a peak current, rise-time, and current values at 30 ns and 60 ns. However, as we will show, it is dangerous to use this as a design specification. Specifically, much work has been done showing large variations between ESD guns which are allowed under the the standard. Even with the same gun, the actual test setup drives significant variations. Some of the reasons/practical implementations are:

- Calibration method/set-up does not allow a "hand-held" gun; the gun must be mounted ("tripod or equivalent non-metal low loss support" [1]). Unfortunately, the gun is made to be "hand-held" and it is commonly used in this way.
- There are numerous reports of operator dependent variations, which are not included in the standard, and impact the calibration waveform [3]. We have experienced first-hand not only significant IEC level differences between guns from different manufacturers, but also from different gun models from the same manufacturer.
- In general, the impact of gun positioning and operator to gun coupling cannot be ignored.

SERIES ELEMENTS

While system level standards do provide expected current waveforms (and a calibration method to verify them), the test-setup for which these waveforms are produced varies significantly from the test-setup

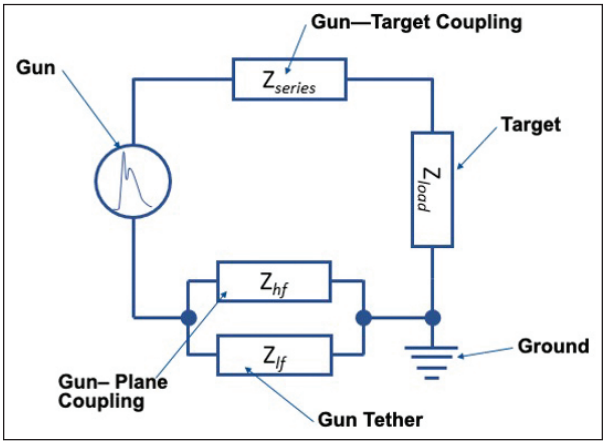

Figure 1: Circuit analogue of calibration and actual testing setups

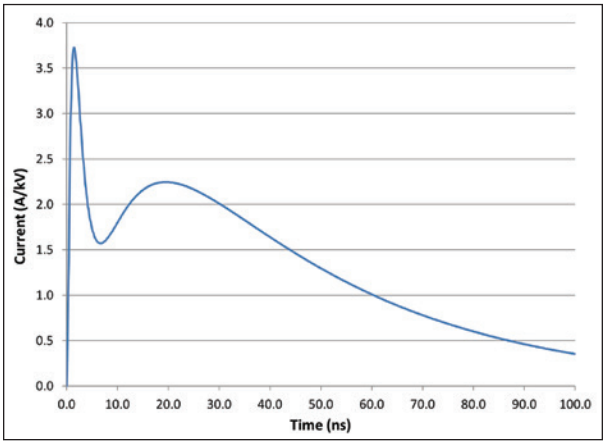

Figure 2: IEC 61000-4-2 calibration current waveform [1]

in which actual device testing is performed. As highlighted in Figure 3, the calibration setup consists of a vertical ground plane which contains a specially designed target/load. The ESD gun is mounted on mechanical holder, and the ground return (or tether) is pulled into a specific shape. When devices are tested, the special target is replaced by the actual device, placed over a horizontal ground plane, with a much more arbitrary ground connection than the vertical plane presents to the target.

The ESD gun can now be held by a human operator and the position and shape of the tether is much less stringently controlled. One should not assume that the current waveform introduced to a device under test (DUT) is exactly the same as the waveform produced in the calibration setup. In fact, significant deviations in the current waveform can result, leading to unexpected performance (both pass and fail) and unrepeatable results.

While the coupling between the ESD gun and the target/DUT (Z_{series} in Figure 1) may seem like an insignificant contributor to the overall performance of the circuit, remember that an ESD gun in direct contact with the target/DUT is not the only configuration—in fact, the coupling between the ESD gun and the target/DUT can be quite different for some configurations. Many automotive system-level test standards [4-7] apply discharge through a variety of gun-target couplings. In addition to the most common gun-target coupling (i.e., contact discharge), there are four other couplings (some used in conjunction), namely:

- Spark: air discharge
- Wiring harness/cable
- Common-mode choke
- Series resistor

Spark: Air Discharge

Air-discharge is already known to produce a large variation of current waveforms—with no single waveform being deemed as "correct." This is acknowledged in the two primary general system-level ESD Standards [1, 2]. The IEC standard describes it as:

> "*The spark is a very complicated physical phenomenon. It has been shown that with a moving spark gap the resulting rise time (or rising slope) of the discharge current can vary from less than 1 ns and more than 20 ns*" [1].

The ISO standard states it as:

> "*The air discharge method virtually replicates ESD, as it would occur in the actual environment. In effect, this means that the impulse current waveforms delivered to the DUT are allowed (and expected) to vary significantly from pulse to pulse.*" [2].

The strong relationship between the length of the air-discharge spark and the severity of the resulting current waveform means that variations in spark length translate directly into variations in current waveform. There are known factors which lead to variation in spark formation, with humidity and speed-of-approach being commonly recognized causes.

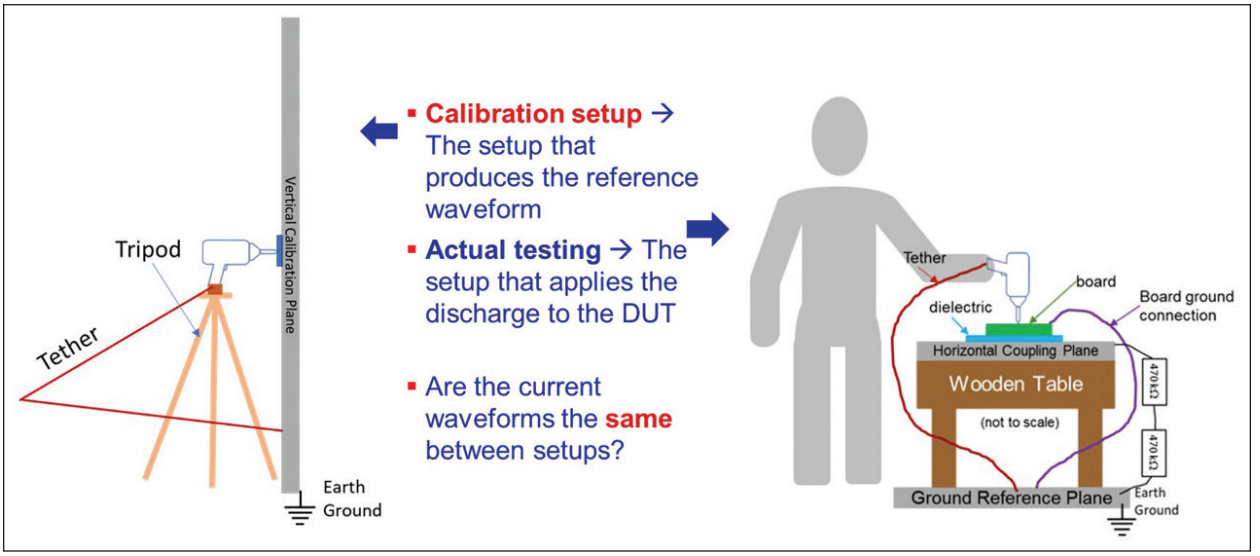

Figure 3: Comparison of the calibration setup and a typical actual testing setup

However, other factors also play a role, including the shape of the electrodes between which the spark forms, and, while the standards do closely control the shape of the electrode on the ESD gun, there is no control on the shape of the target electrode.

This becomes an extremely important factor in J2962-x automotive standards [4, 5], in which air-discharges are applied directly to the BUS signal wires in the wiring harness. But current waveforms are not generally monitored *in-situ* during system-level testing; the person applying the discharge has no reasonable gauge of the severity of the current pulse that was actually delivered.

The current waveform shown in the IEC 61000-4-2 standard consists of a fast-rise time to a peak current, followed by a drop in current and a slower rise-time to a second peak. Figure 4 shows an expectation of two clearly distinguishable peaks (for a negative discharge) in the lower left corner. This expected waveform has a green region (indicating the 1st peak region) and a blue region (indicating the 2nd peak region). To the right of Figure 4, actual measured current waveforms are shown.

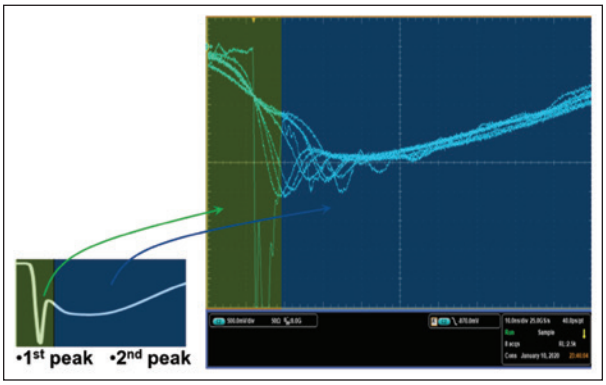

Figure 4: Possible expected waveform shape and actual waveform shapes from testing

These waveforms were all generated in the same test setup, by the same operator, at the same voltage level. The only variances were the speed and angle at which the operator approached the target with the ESD gun.

More troubling is that a single waveform in this set actually damaged the DUT, while others did not. If the exact speed and angle was not reproduced by the operator, then damaged DUT did not occur, leading to a high-level of unrepeatability in testing results. Because there is no accepted air-discharge current waveform shape, it is unclear what should be expected during design and, further, what should be allowed during testing.

Another factor in air-discharge testing is the challenge of holding the pre-charge voltage on the ESD gun before spark formation. In cases where the target is a very sharp geometry (such as a wire) it is quite possible to lose charge through corona discharge. While the ESD gun may have been programmed to deliver a 10-kV discharge, at the time of spark formation perhaps only a 5-kV equivalent charge remains. In fact, doubling the discharge voltage in this case may lead to no increase in discharge current whatsoever.

So what does it mean to apply a 10-kV air-discharge to a DUT and observe no failure? Is the DUT robust or was a "soft" current waveform delivered? If a DUT fails 10-kV, does this mean it will be weak in a different test environment (or in the actual application)? Given the lack of fidelity between the programmed discharge voltage and the actual current-waveform delivered, no meaningful conclusions can be reached about the robustness of a DUT by a simple statement that the DUT passed or failed discharge voltage-level testing.

Wiring Harness/Cable

Having established the consequences of discharging through a series spark, other series elements should also be evaluated. For example, requirements to apply the discharge through a series wire or cable are not uncommon. Just as with the spark in air-discharge, the impedance of a wire or cable is not trivial, especially when considered across the large frequency spectrum of the ESD pulse. In fact, these configurations must be evaluated as transmission-line, which is not matched on either the stimulus or the load side. Reflects should be expected, resulting in deviations from a direct contact waveform.

Figure 5 shows an example of an ESD discharge applied through 5 meters of RG-58 cable, relative to the expected waveform without a cable present. If the significant reflections demonstrated in Figure 5 are not anticipated during the DUT design phase, unexpected failures can result.

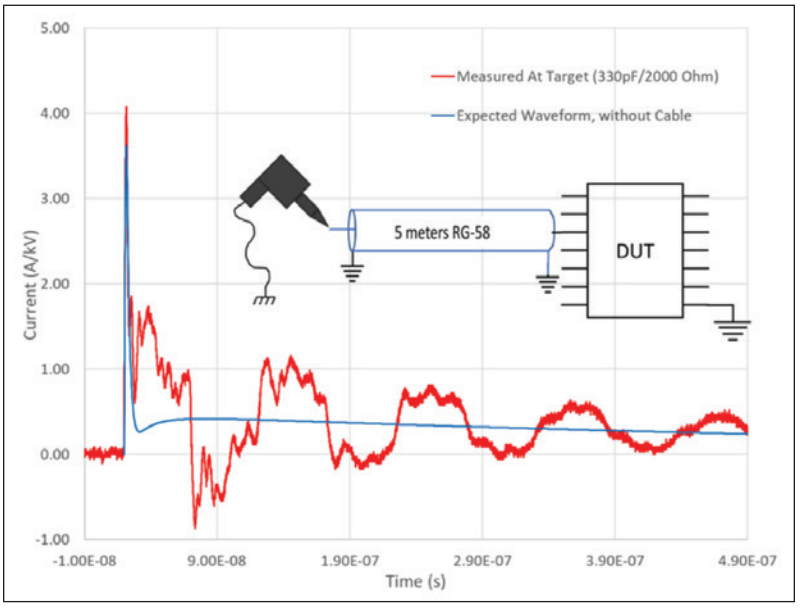

Figure 5: Example of an ESD discharge through a cable

Common Mode Choke

Common mode chokes (CMCs) are often required to meet EMC emission requirements (more on that in the next paragraph) in differential communication busses (LIN, CAN, …), with a typical inductance of 100 µH. The CMC is placed directly in the ESD discharge path and, in principle, one would expect a beneficial high-frequency damping of the ESD energy.

Unfortunately, a CMC can display a strong saturation behavior (due to the ferrite saturation [10-12]), which results in a drastic reduction of the inductance over a certain threshold current. In addition,

a CMC features an undesirable snapback characteristic for ESD current densities. This highly non-linear behavior can force the component-level ESD protection in and out of snapback multiple times, depending on the current density. Figure 6 shows the typical non-linear waveform of a CMC in response to a full IEC event.

The choke allows initial current flow, due to displacement current of the quasi-differential signal. This is followed by a "blocking" period, corresponding to the common mode signal. Eventually, the choke saturates, causing low impedance, and therefore high current flow.

This complex waveform depends on several parameters, including:

- Discharge level;
- Board parasitics; and
- Unspecified/uncharacterized choke parameters (i.e., two nominally identical CMCs will yield completely different IEC results).

Series Resistors

Some automotive system-level ESD standards require testing through series resistance. When using large resistance values, the expectation is to limit the current (Figure 7). Unfortunately, there is nothing to limit voltage build-up on discharge side of resistor. Therefore, spark-over of the resistor is likely, thereby causing a full discharge into DUT (effectively emulating an air-discharge test.)

RETURN PATH

The testing setup strongly influences the ground return path. With reference to Figure 8, the common setup for IEC61000-4-2 features:

- Board to horizontal coupling plane (HCP) capacitance inserted in the high-frequency path, and
- Added wire impedance in the low-frequency path.

The common setup for IEC62228 [8] features:

- Metal fixture between board and HCP, tether directly to grounded HCP, and
- Strong low-impedance bond between board and HCP.

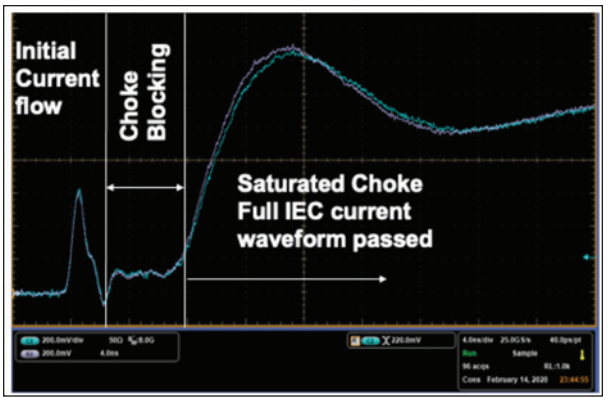

Figure 6: CMC response to a full IEC event

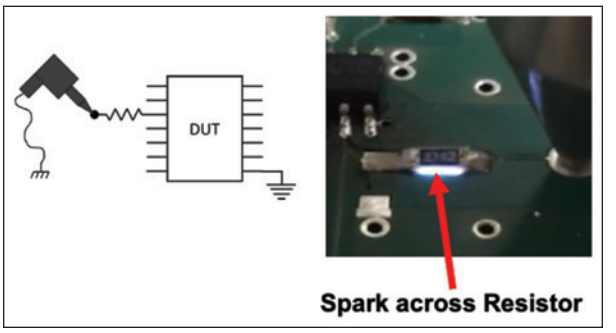

Figure 7: spark-over mechanism of contact discharge through a series resistor

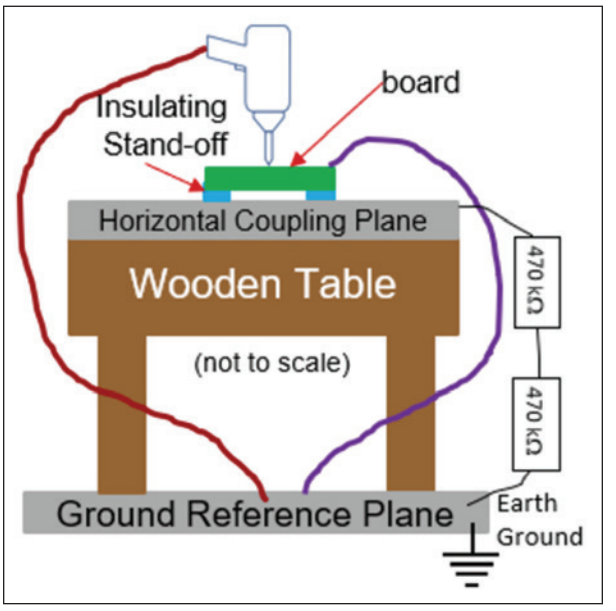

Figure 8: Common IEC 61000-4-2 implementation

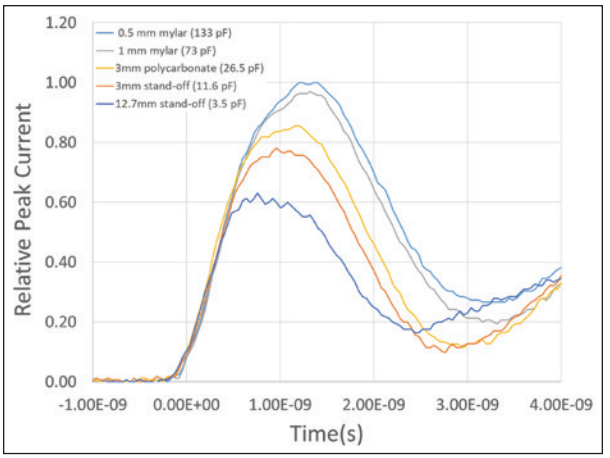

Figure 9: First peak modulation caused by different material and thickness of the dielectric between board and HCP

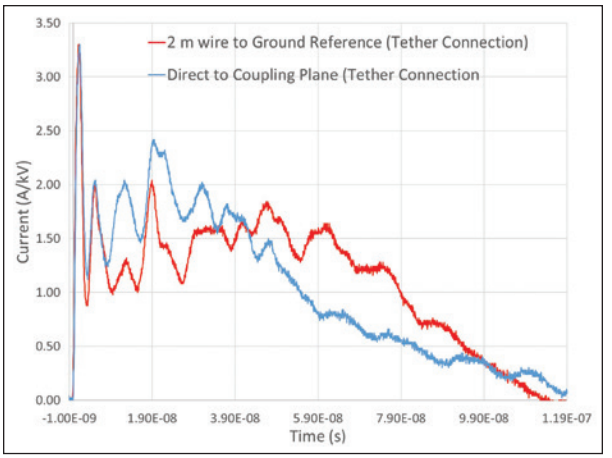

Figure 10: Effect of inserting a wire between the board and ground reference plane adds impedance in low frequency return path

If we look at the two return paths separately, the high-frequency return path is primarily a capacitive coupling, from the gun to the coupling plane. Coupling between board/plane adds series impedance, which can cause significant degradation of 1st peak (Figure 9).

If we look at the low frequency return path, it is mainly driven by the gun tether. Inserting a wire between the board and the ground reference plane adds impedance in the low frequency return path (Figure 10).

As shown, the test-setup with respect to the ground return path can have significant impact on the shape and severity of the current waveform delivered to the DUT. Seemingly subtle changes in the test-setup

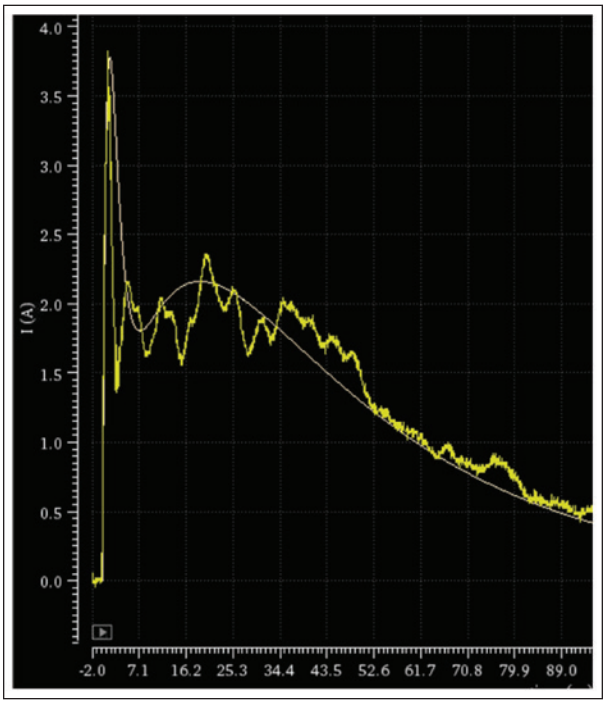

Figure 11: Model vs waveform for 2 Ohm load

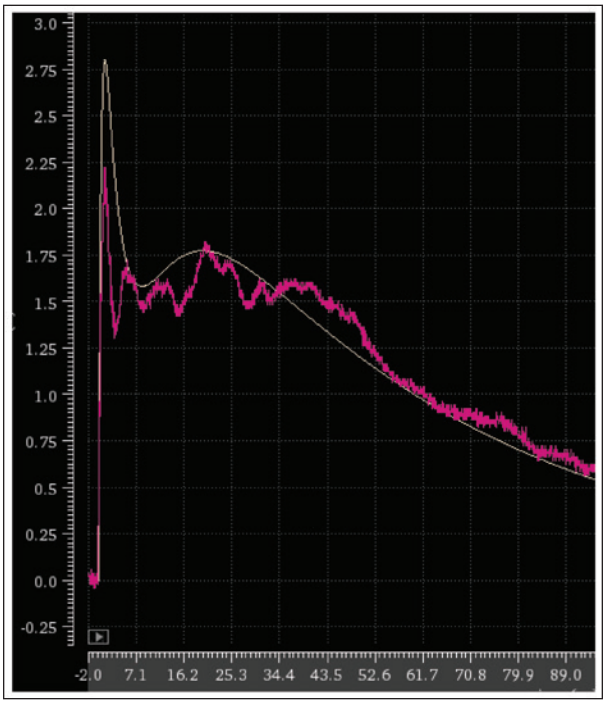

Figure 12: Model vs waveform for 100 Ohm load

can lead to consequential changes in testing results, leading to repeatability issues. Similarly, seemingly subtle differences between different test-setups can lead to differing testing results between two test facilities, leading to reproducibility issues.

LOAD

The ESD gun is calibrated to a 2 Ohm (high bandwidth) load. Specifying a single load allows significant deviation/differences between guns— this was a "painful" lesson already learned with HBM test standards. Not only do guns vary significantly, models used for pre-silicon validation vary. A large set of guns/simulation models were evaluated in [9]. From Figure 11, it can be seen that there is a good agreement between a specific model and a specific ESD gun's waveform for 2 Ohm load.

However, the agreement is not good for a 100 Ohm load (Figure 12), which begs the question of whether the gun or the model is more correct. Because the standards do not set an expectation, the question cannot be answered.

CONCLUSION

This article focuses on the specific ESD design challenges, stemming from the fact that all relevant system-level standards were created to validate systems and not components. Applying these standards to individual components requires interpretation, which leads to ambiguity in the meaning of the results. Additionally, there are poorly controlled aspects of the test standards, which can create large variations in the applied stress. Our examples place particular emphasis on the air discharge test and the shortcomings that make it a virtually unreproducible test and, hence, of questionable usefulness.

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IMPLEMENTING EMBEDDED ESD DETECTION, PART 2

By Jeffrey C. Dunnihoo, on behalf of EOS/ESD Association, Inc.

In Part 1 of this series, we introduced embedded detection technology, which augments basic protection against ESD events, and explored the opportunities for embedded ESD detection solutions.

Protection sets the fundamental thresholds for a device's robustness. In contrast, detection broadens the device's awareness around these limits, helping it identify potential issues such as data corruption, immediate damage, or the cumulative effects of ESD within these thresholds. Armed with this, the designer has an opportunity to design in recovery functionality rather than just accept a mysterious malfunction.

Here, in Part 2, we shift our focus to the practical aspects of implementing embedded ESD detection. We'll provide a step-by-step guide, discuss validation and testing methodologies, present case studies, and delve into future trends and innovations in the field.

PREPARING FOR EMBEDDED ESD DETECTION

As technology process nodes advance, the susceptibility to physical damage from a given ESD event increases, but on-chip HBM and CDM protection is also advancing to protect these delicate nodes. However, these advanced on-chip ESD protection devices are typically designed to protect the chip when powered off, during PCBA assembly and only under factory ESD controls. As these protection circuits clamp harder and faster, they can even prevent the off-chip discrete protection from triggering, making the whole system counter-intuitively less robust.[1] Protection circuits that are designed to clamp VDD to VSS can cause extensive data corruption and state incoherence inside the running chip. This leaves device registers, oscillators, and logic in unpredictable and unknown states at worst and in a sudden and unexpected Power-on-Reset (POR) vector at best.

Jeffrey Dunnihoo is the founder of Pragma Design in 1997, specializing in interface design architecture and ESD, EOS, and other transient analysis technologies. He has presented at IEEE EMC Society, the EOS/ESD Association, and ISTFA, and has co-authored a new textbook with other ESD experts on ESD co-design fundamentals, as well as a children's book series on technology and microelectronics. He has also been a contributor to industry groups and standards bodies, such as USB, IEEE 802.11, VESA/DisplayPort, ESD Industry Council, and has served on ESDA working groups.

BALANCING ESD PROTECTION WITH ESD DETECTION

External system-level ESD protection devices are typically not (yet) super-conducting, and so there is some residual current sharing with the Device Under Protection (DUP) ASIC or SoC, etc.

This residual pulse is not necessarily shaped like the CDM or HBM standards the chip has been designed for, and typically, these protections are intended for activation during assembly when no power is applied. Complaining to the IC manufacturer that their chip does odd things when exposed to ESD brings to mind the old story of a man telling his doctor, "It hurts when I do this." To which the doctor replied, "Then don't do that." The reality is there is no standard for validating chip-level functionality after an ESD strike, and so the system designer is left to manage it or, worse, to blame the susceptibilities on firmware. "Here be dragons," they say.

1. **Soft-Reset**: When a system successfully survives an ESD zap, the HBM or CDM on-chip

protection may trigger its on-board power supply clamps that short VDD to VSS to minimize voltages throughout the chip. (See Figure 1.) Once the pulse has dissipated, the power rails will return to their pre-zap levels and may trigger Power-on Reset (POR) circuits, resetting the system. If the firmware is aware that an ESD event has been detected just before POR has occurred, then the software can take additional remedial and recovery actions.[2]

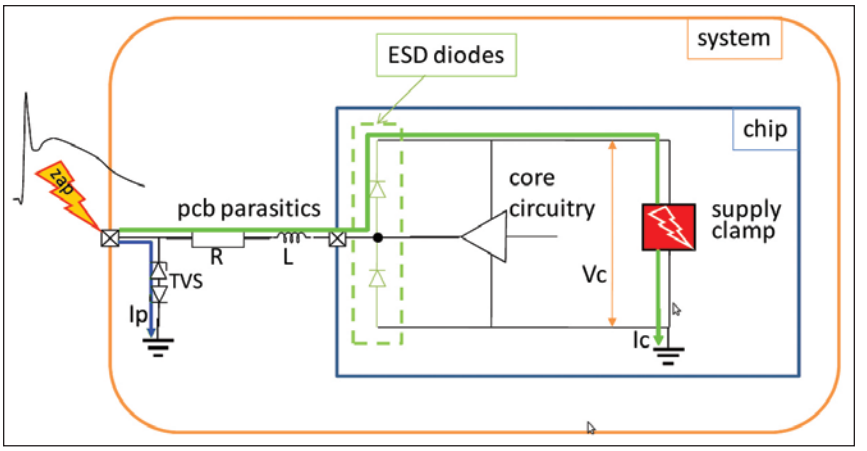

Figure 1: VDD-to-VSS Power Clamp Shorts power supply out internally and causes Power On Reset (ESD Industry Council WP3 Part I)

2. **System Lockup**: As with a soft reset, when the on-chip protection occurs, the logic state and coherency cannot be trusted. In fact, the MCU or Crystal Oscillator may run "off into the weeds" and require a hard power cycle, which may not be possible in mission-critical and medical devices. However, embedded ESD detection logic can recognize the event and "kick start" the device back to life. If the software is written in such a way that the user does not notice this disruption, then such an upset has been effectively eliminated from an IEC qualification failure list without board spins, etc.
3. **Data Corruption**: Any software programmer assumes that when a value is written to a location, it will be there when it is read back. However, after an ESD event, memory and registers, program counters, and stacks can be altered slightly or obliterated. This can sometimes create a latent "soft error," which might not manifest itself for days or operation. An ESD event detector can alert the program to recheck the system state and restore corrupted areas or at least throw an error alert.
4. **Latent Circuit Damage**: Even a survivable strike may significantly degrade component lifetimes.[3] A system that has weathered 10,000 pulses is not necessarily as healthy over time and temperature as a system that has never been struck.
5. **TVS Optimization:** By recording and perhaps transmitting ESD event telemetry back to the manufacturer, system designers can fine-tune the protection levels, potentially reducing cost by optimizing for the actual ESD levels the products are seeing in the field.

EMBEDDED DETECTOR TECHNOLOGIES

The application of ESD detectors to characterize system-level pulses and enhance robustness is relatively new, but ESD detector types and functionality have been under development for years. Here are some early examples that bracket the simple-to-complex options for implementation in between.

BASIC ESD DETECTOR: PEAK-HOLD CIRCUIT

In 2011, Nathan Jack and Elyse Rosenbaum presented an on-die detector that could be probed at the wafer level.[4] The node to be monitored is connected to a diode which dumps some of the incident ESD current into a capacitor which can be monitored by a buffer circuit. (See Figure 2.) This concept can be expanded to include multi-level detection and long-duration pulse memory.

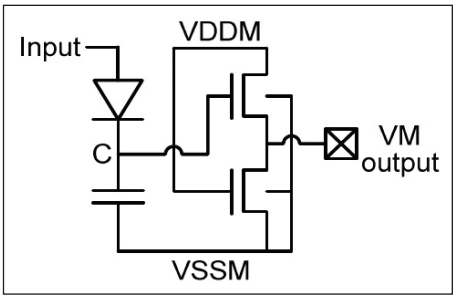

Figure 2: On-die ESD detector, Jack, et al, 2011 (ESDA)

EXTREME ESD DETECTOR: ON-CHIP OSCILLOSCOPE

In 2013, Fabrice Caignet et al. demonstrated a 20 GHz on-chip oscilloscope detector circuit to reconstruct residual ESD voltages and analyze the pulse in more detail to help optimize the requirements for protection circuitry on a particular technology node going forward.[5]

As opposed to the simple level detector in [4], this circuit allows the reconstruction of the actual shape and spectral content of ESD pulses entering a chip.

These early examples of embedded detection have been complimented by the ongoing innovation and development in embedded on-chip ESD detection applications. As ICs continue to evolve and geometries shrink, these technologies may play an active role in preventing further technology nodes from becoming almost unusable due to ESD soft errors and upsets.

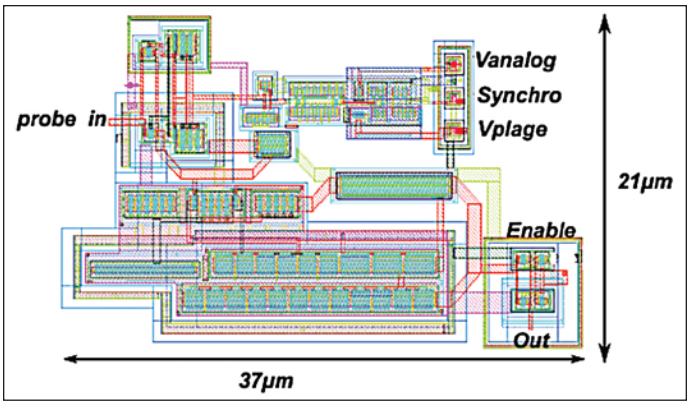

Figure 3: 20GHz On-Chip Oscilloscope, Caignet, etal, 2013 (ESDA)

SYSTEM-LEVEL ESD DETECTOR: DISCRETE TEST MODULE

In some cases, a discrete detector may be adapted to an existing system with small PCBs or Flexible Attach Rework (FAR) modules (See Figure 4.) These "dead-bug" detectors can be used to record and transmit ESD events in a system to isolate entry/exit vectors and problematic nodes instead of adding probe cables which can alter the nature of the ESD pulse paths. Obviously, if the ESD detection capability is already integrated into the system, then gathering such data is faster, more reliable, and more convenient.

CONCLUSION

In Part 1 of this article series, we explored the critical need for embedded ESD detection in the context of advanced semiconductor nodes. The vulnerabilities of advanced ICs to ESD damage have necessitated the development of innovative solutions, such as embedded detection technology, to augment protection schemes. Embedded detection's real-time monitoring and response capabilities offer a new level of overall robustness and reliability by expanding the visibility of ESD events and effects. In Part 2, we reviewed the basics of detection implementation in a system, along with a few examples to consider. In Part 3, we will outline practical aspects of implementing embedded on-chip or system-level ESD detection, providing engineers and designers with guidance on integrating these technologies into their semiconductor designs and ensuring the robustness of their electronic devices.

ENDNOTES

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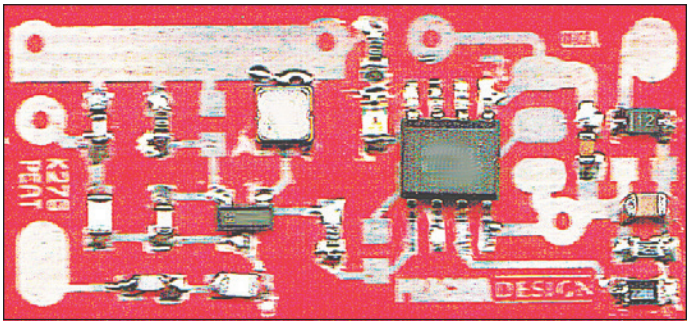

Figure 4: Discrete "dead-bug" system-level detector with 433MHz ASK data link telemetry (Pragma Design)

CORRELATION BETWEEN INSERTION LOSS AND INPUT IMPEDANCE OF EMC FILTERS

Part 3: Cascaded LC and CL Filters

By Bogdan Adamczyk and Jake Timmerman

This is the third article of a three-article series devoted to the correlation between the insertion loss and input impedance of passive EMC filters. In the first article, [1], *LC* and *CL* filters were discussed, while the second article, [2], was devoted to the π and *T* filters. This article focuses on *LCLC* and *CLCL*, or cascaded *LC* and *CL*, filters. Analysis, simulation, and measurement results show that the frequencies at which the insertion losses of these filters are equal are the same frequencies at which the input impedances are equal. These frequencies define the regions where one filter configuration outperforms the other (with respect to the insertion loss). To determine these regions analytically, we compare the input impedances of the two filters.

INPUT IMPEDANCE TO THE CASCADED LC FILTER

The input impedance $\hat{Z}_{IN}$ to the cascaded *LC* filter is calculated from the circuit shown in Figure 1.

The input impedance of this filter can be obtained by using the input impedance of the π filter [2] and combining it in series with the impedance of an inductor.

$$\hat{Z}_{IN}(s) = \mathrm{sL} + \frac{s^2LRC+sL+R}{s^3LRC^2+s^2LC+s2RC+1} \quad (1)$$

or [3]

$$\hat{Z}_{IN}(s) = \frac{s^4L^2RC^2+s^3L^2C+s^23LRC+s2L+R}{s^3LRC^2+s^2LC+s2RC+1} \quad (2)$$

or in terms of the frequency

$$\hat{Z}_{IN}(j\omega) = \frac{(\omega^4L^2RC^2+R-\omega^23LRC)+j(\omega2L-\omega^3L^2C)}{(1-\omega^2LC)+j(\omega2RC-\omega^3LRC^2)} \quad (3)$$

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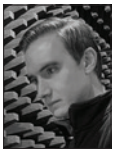

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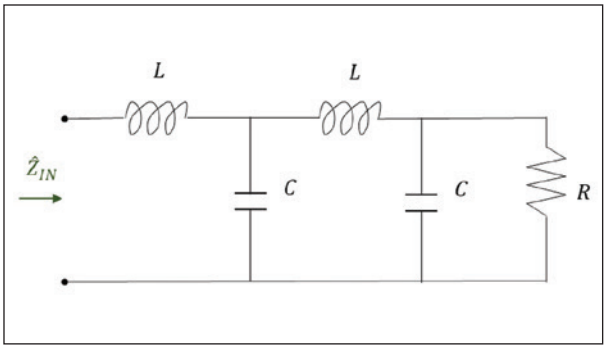

Figure 1: Input impedance to the cascaded *LC* filter

The magnitude of the input impedance is

$$Z_{IN} = \frac{\sqrt{(\omega^4L^2RC^2+R-\omega^23LRC)^2+(\omega2L-\omega^3L^2C)^2}}{\sqrt{(1-\omega^2LC)^2+(\omega2RC-\omega^3LRC^2)^2}} \quad (4)$$

INPUT IMPEDANCE TO THE CASCADED CL FILTER

The input impedance $\hat{Z}_{IN}$ to the cascaded *CL* filter is calculated from the circuit shown in Figure 2.

The input impedance of this filter can be obtained by using the input impedance of the *T* filter [2] and combining it in parallel with the impedance of a capacitor.

$$\hat{Z}_{IN}(s) = \left(\frac{s^3L^2C+s^2LRC+s2L+R}{s^2LC+sRC+1}\right) \Big\| \left(\frac{1}{sC}\right) \tag{5}$$

or [3]

$$\hat{Z}_{IN}(s) = \frac{s^3L^2C+s^2LRC+s2L+R}{s^4L^2C^2+s^3LRC^2+s^23LC+s2RC+1} \tag{6}$$

or, in terms of the frequency

$$\hat{Z}_{IN}(j\omega) = \frac{(R-\omega^2LRC)+j(\omega2L-\omega^3L^2C)}{(\omega^4L^2C^2-\omega^23LC+1)+j(\omega2RC-\omega^3LRC^2)} \tag{7}$$

The magnitude of the input impedance is

$$Z_{IN} = \frac{\sqrt{(R-\omega^2LRC)^2+(\omega2L-\omega^3L^2C)^2}}{\sqrt{(\omega^4L^2C^2-\omega^23LC+1)^2+(\omega2RC-\omega^3LRC^2)^2}} \tag{8}$$

CASCADED LC FILTER VS. CASCADED CL FILTER – INPUT IMPEDANCE – SIMULATIONS AND CALCULATIONS

Let's look at the input impedances of the two filters. The simulation circuit for this comparison is shown in Figure 3.

The input impedances of the two filter configurations are shown in Figure 4.

Note that the two input impedances are equal at three frequencies: 561.04 kHz, 1.04 MHz, and 1.36 MHz.

Next, let's calculate the frequencies at which the input impedances of the two filters are equal. Equating the expressions in equations (4) and (8) produces

$$\frac{\sqrt{(\omega^4L^2RC^2+R-\omega^23LRC)^2+(\omega2L-\omega^3L^2C)^2}}{\sqrt{(1-\omega^2LC)^2+(\omega2RC-\omega^3LRC^2)^2}} = \frac{\sqrt{(R-\omega^2LRC)^2+(\omega2L-\omega^3L^2C)^2}}{\sqrt{(\omega^4L^2C^2-\omega^23LC+1)^2+(\omega2RC-\omega^3LRC^2)^2}} \tag{9}$$

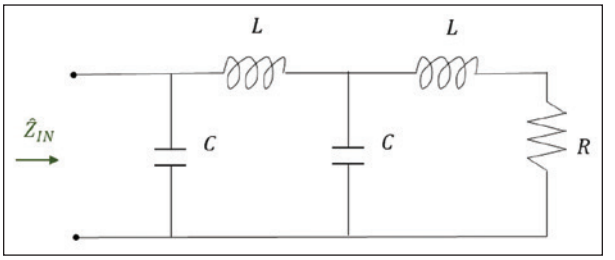

Figure 2: Input impedance to the cascaded *CL* filter

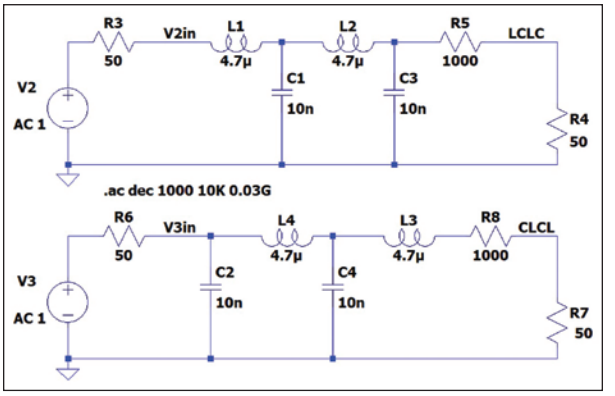

Figure 3: Simulation circuit for comparison of input impedances

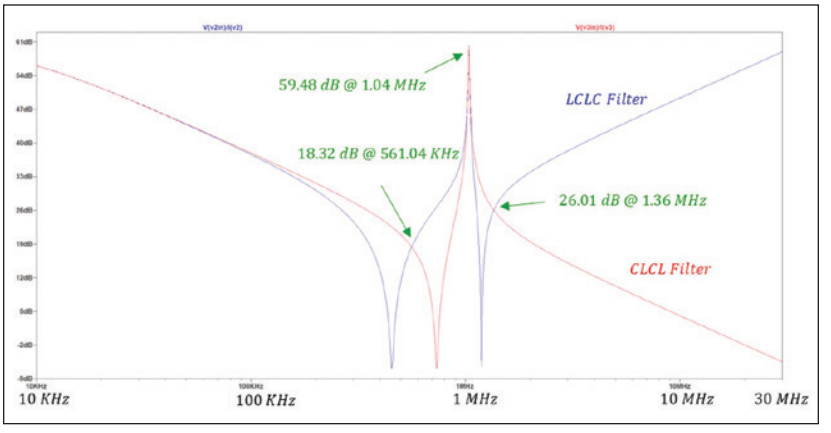

Figure 4: Simulation results: Input impedance – cascaded *LC* filter vs. cascaded *CL* filter

This equation can be solved for ω [3] resulting in

$$\omega_1 = \sqrt{\frac{2-\sqrt{2}}{LC}} \quad (10a)$$

$$\omega_2 = \sqrt{\frac{2}{LC}} \quad (10b)$$

$$\omega_3 = \sqrt{\frac{2+\sqrt{2}}{LC}} \quad (10c)$$

The corresponding frequencies in Hertz are

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{2-\sqrt{2}}{LC}} = \frac{\sqrt{2-\sqrt{2}}}{2\pi\sqrt{4.7\times10^{-6}\times10\times10^{-9}}} = 561.8\ kHz \quad (11a)$$

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{3}{LC}} = \frac{\sqrt{2}}{2\pi\sqrt{4.7\times10^{-6}\times10\times10^{-9}}} = 1.038\ MHz \quad (11b)$$

$$f_3 = \frac{1}{2\pi}\sqrt{\frac{2+\sqrt{2}}{LC}} = \frac{\sqrt{2+\sqrt{2}}}{2\pi\sqrt{4.7\times10^{-6}\times10\times10^{-9}}} = 1.356\ MHz \quad (11c)$$

These results are consistent with the values obtained from the simulation in Figure 4.

CASCADED LC FILTER VS. CASCADED CL FILTER – INSERTION LOSS – SIMULATIONS AND MEASUREMENTS

Figure 5 shows the simulation circuit used for the comparison of insertion losses.

The simulation results are shown in Figure 6.

The insertion losses are equal at the frequencies of 561.05 kHz, 1.04 MHz, and 1.358 MHz. These are the same frequencies at which the input impedances of the two filters were equal!

Note that up to the frequency of 561 kHz, the insertion loss of the *CLCL* filter is larger than that of the *LCLC* filter. Between the frequencies of 561 kHz and 1.04 MHz, the insertion loss of the *LCLC* filter is larger. Between the frequencies of 1.04 MHz and 1.36 MHz, the insertion loss of the *CLCL* filter is larger. Beyond the frequency of 1.36 MHz, the insertion loss of the *LCLC* filter is again larger.

Once again, [1,2], we have arrived at a very important observation: once the filter components values *L* and *C* are chosen, we can determine the frequencies at which the insertion losses of the two filters are equal. These are the frequencies at which the input impedances are equal, given by Equations (11).

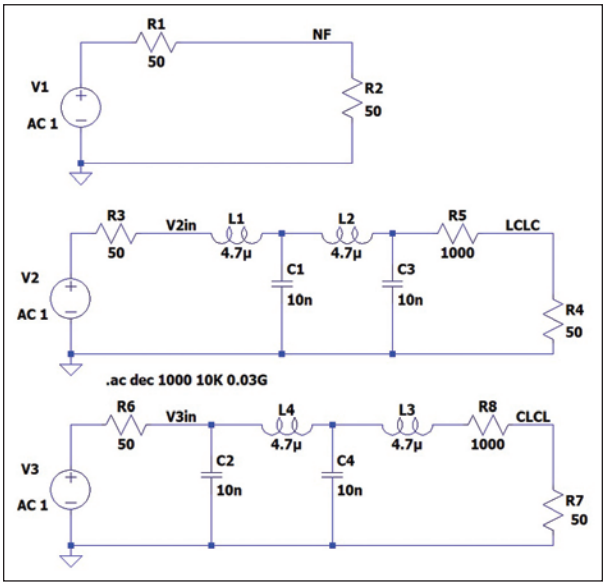

Figure 5: Simulation circuit for comparison of insertion losses

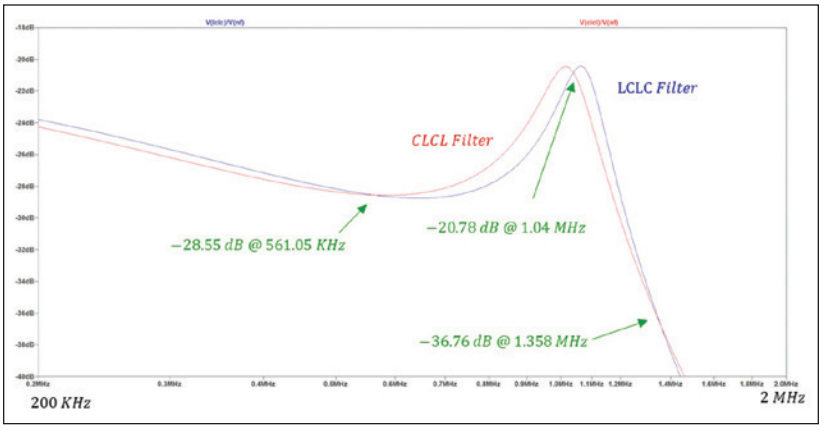

Figure 6: Simulation results: Insertion loss – cascaded *LC* filter vs. cascaded *CL* filter

To verify the simulation results of the insertion loss, the measurement setup shown in Figure 7 was used.

The measurement results are shown in Figure 8.

Note that the measurement results agree with the calculated and simulated results.

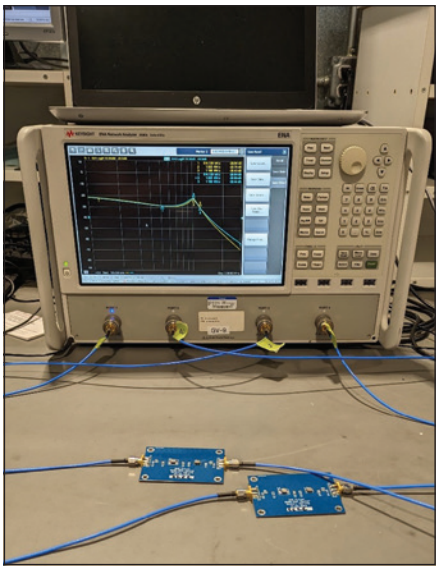

Figure 7: Measurement setup: Insertion loss – cascaded *LC* filter vs. cascaded *CL* filter

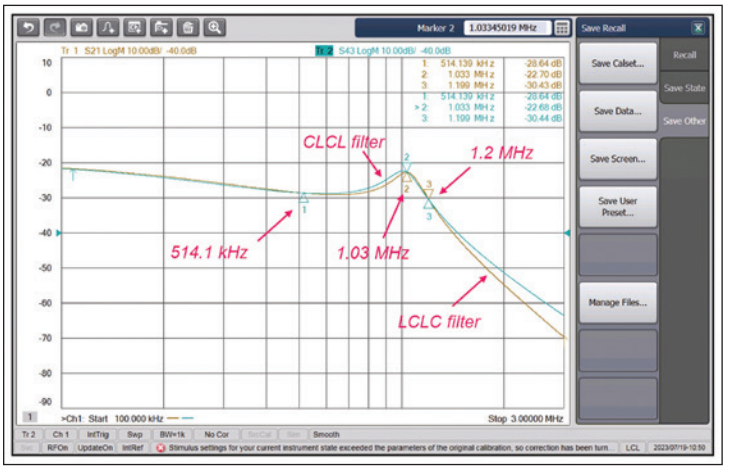

Figure 8: Measurement results: Insertion loss – cascaded *LC* filter vs. cascaded *CL* filter

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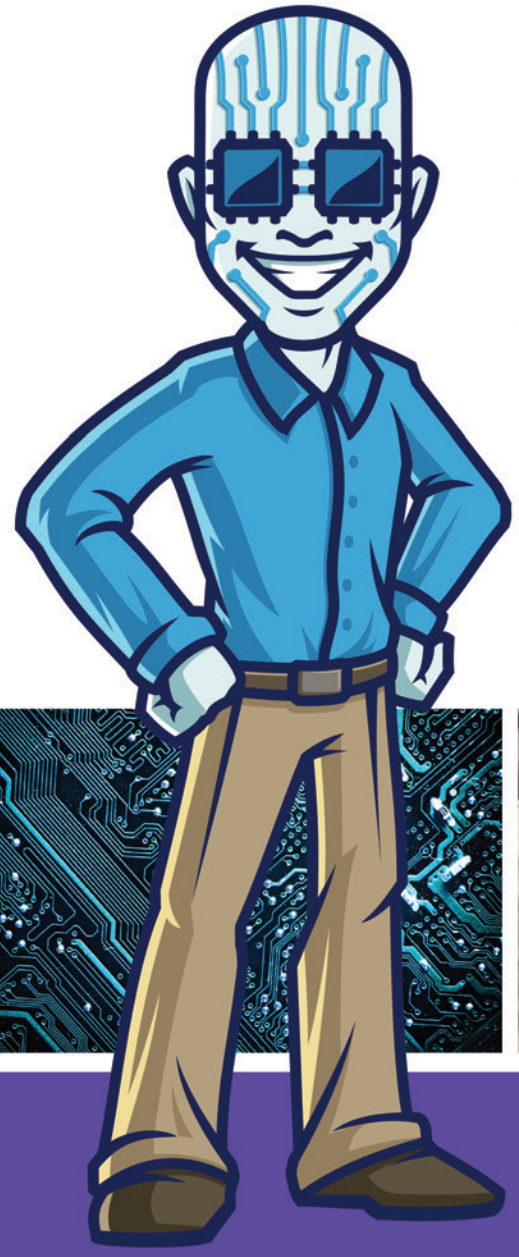

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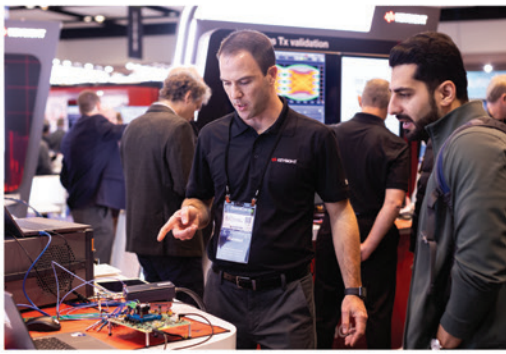

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