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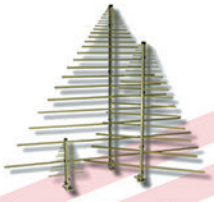

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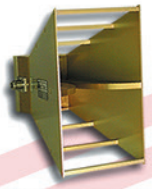

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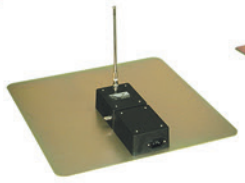

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New Solder Composition Could Extend Life of EV Electronics

A group of international researchers has reportedly developed a new formula for solder that could help to reduce cracking and premature wear in vulnerable electronics used in electric vehicles (EV).

According to a recent posting to the website of *The Engineer*, the new solder mix replaces common, lead-free replacements for lead that are more prone to degrade in the high-temperature environment found in EVs. Instead of using tin, silver, or copper, the new formula includes nanoparticles and other microalloying elements that enhance the properties of solder and the reliability of solder joints. These changes are reportedly sufficient to help reduce the incidence of cracking and premature degradation.

The research leading to the potential solder formula was conducted at the General Engineering Research Institute at Livermore John Moores University in the United Kingdom and researchers at partner organizations Gunma University in Japan and Universiti Malaysia Perlis in Malaysia. The research is being funded by the British Council's COP26 Trilateral Research Initiative, which is intended to promote collaborative research in the field of climate change.

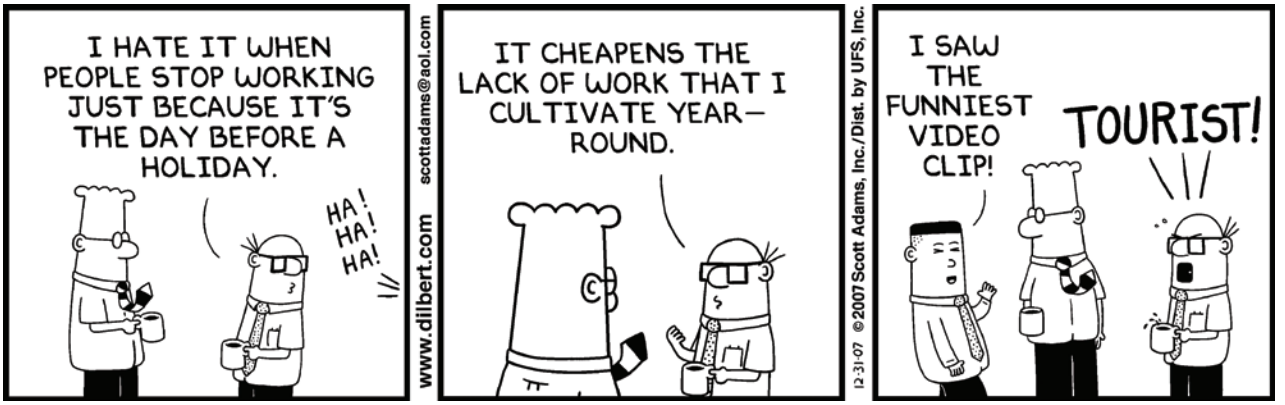
EU Task Force Offers Clarification of Surveillance Requirements for Legacy Medical Devices

A European Union (EU) task force has issued a document intended to clarify the application of the EU's Medical Device Regulation (2017/745, also known as the MDR) post-market surveillance requirements to legacy medical products.

Published by the Medical Device Coordination Group (MDCG), the document, MDCG 2021-25 is intended to provide a "legally defendable and pragmatic" position on requirements applicable to medical devices placed on the market prior to May 26, 2021, the date on which the requirements of the MDR came into full effect. The document is intended to address a large number of products that were placed on the market prior to that date in accordance with the EU's Medical Device Directive (90/385/EEC).

In brief, the document concludes that all relevant MDR requirements related to post-market surveillance, market surveillance, and vigilance are equally applicable to legacy devices and that manufacturers of legacy devices must continue to issue periodic safety update reports (PSURs) in connection with their products.

The MDCG was established under Article 103 of the MDR and is comprised of representatives from all EU Member States. However, the document and its findings do not reflect the official position of the European Commission and are not binding under EU law.



FCC Commits Additional $1 Billion for Connectivity in Schools, Libraries

The U.S. Federal Communications Commission (FCC) has committed an additional $1 billion in funding for U.S. schools, libraries, and education consortia to increase student access to devices and broadband connectivity in support of remote learning.

According to a press release, a total of $1.159 billion has been committed to 2471 schools, 205 libraries, and 26 consortia under the Commission's Emergency Connectivity Fund Program. The commitment brings to $2.362 billion the total amount allocated to date by the FCC, out of a total of over $7 billion earmarked for the program.

Funding under the Emergency Connectivity Fund Program can be used for the purchase of laptops and tablets, Wi-Fi hotspots, modems, routers, and broadband connections for use by students, school staff, and library patrons needing these technologies.

To date, the FCC estimates that nearly 8 million students have been afforded connectivity access benefits under the program.

Biden Nominates FCC's Rosenworcel to Another Term

President Joe Biden has formally nominated Jessica Rosenworcel for another five-year term as a Commissioner of the U.S. Federal Communications Commission (FCC) and has designated her to formally serve as Chair of the Commission.

Rosenworcel's nomination for an additional term is subject to review by the U.S. Senate. If confirmed, Rosenworcel would be the first woman to serve in the role of Commission Chair.

Rosenworcel has served as an FCC Commissioner since 2012 and as Acting Chair of the Commission since the beginning of the Biden administration. Prior to joining the FCC, she served as the Senior Communications Counsel for the Senate Committee on Commerce, Science, and Transportation. Before her service in the public sector, Rosenworcel practiced communications law.

APPLICATION OF THRIFTY TEST EQUIPMENT FOR EMC TESTING

Low-Cost Instruments and Procedures to Troubleshoot EMC Issues

Arnold Nielsen is an iNARTE-certified EMC design engineer with decades of experience in the automotive electronics industry. He currently consults on a wide variety of products and can be reached at arnienielsen@gmail.com.

By Arnold Nielsen

Issues related to electromagnetic compatibility (EMC) are often identified during qualification testing in an accredited EMC test lab which typically occurs late in the product design cycle. Obtaining a cost-effective solution to these EMC issues may be time-consuming, and many EMC labs can be fully booked or have limited availability, have long lead times, or involve significant costs. But inexpensive test equipment and procedures (let's call them thrifty methods) used for helping to solve these EMC issues outside an EMC lab are very desirable, especially if no in-house EMC facilities are readily available.

There are several excellent resources for troubleshooting methods and building a low-cost EMC toolkit.[1] This article offers some other test equipment options that have different capabilities and which can be even less costly. Although the thrifty method is mainly used to compare results before and after implementing a fix (not meeting a specification limit), with some experience, it can also be used in the pre-qualification development stage early in the design cycle to identify potential issues before formal lab testing. Identifying issues early allows maximum flexibility to experiment and provides sufficient time to make cost-effective changes before a design is frozen and difficult to change.

THRIFTY TEST EQUIPMENT

Vector Network Analyzer

One of the low-cost instruments discussed in this article is a vector network analyzer (VNA). Figure 1 shows an example of such an instrument (the NanoVNA[2]). Even though this VNA typically costs less than $150, it is useful from 50 kHz to 3 GHz and comes with cables and calibration terminations. It can be used as a standalone unit via touchscreen, but it is best used with free software QT and Saver. Although this VNA has a lot of capability, I used it for input impedance (S11) and VSWR measurements in the testing on which this article is based.

Software Defined Radio

Figure 2 shows another low-cost instrument, a software defined radio (the SDRplay[3]). Also, typically less than $150, most SDRs also offer lots of capabilities. For the purposes of this article, we'll use the SDR as a spectrum analyzer with the addition of another free software program (Spectrum Analyzer 1.1). While this software may have limitations, such as only fixed frequency spans, it can still be very effective.

Figure 1: Vector network analyzer

Figure 2: Software defined radio

RF Signal Amplifier

A radio frequency (RF) signal amplifier is required for radiated emissions measurements. Figure 3 shows one low-cost example. This particular unit uses a monolithic microwave integrated circuit (MMIC) amplifier and is useful from 50 kHz to at least 2 GHz, Gain = 20-30 dB, and only costs about $30. For a device under test (DUT) with very low emission limits, two amplifiers in series may be required.

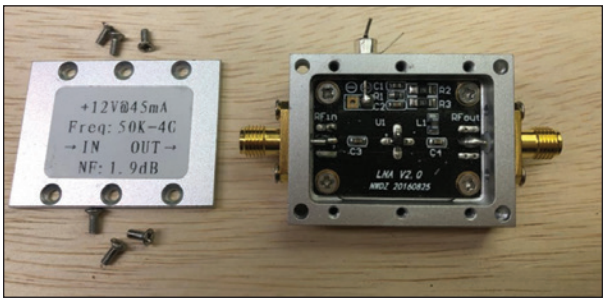


Figure 3: RF signal amplifier

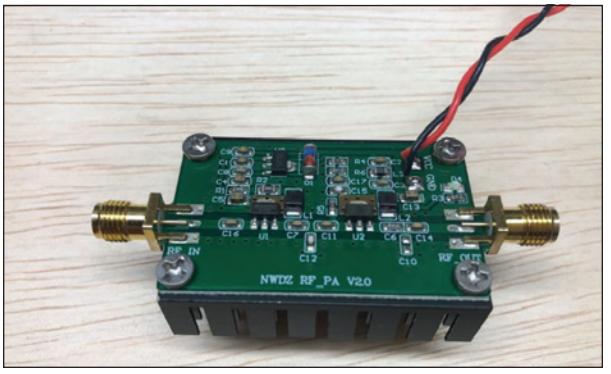


Figure 4: RF power amplifier

Figure 5: RF signal generator

RF Power Amplifier

For radiated immunity (e.g., in this article, bulk current injection, or BCI), an RF power amplifier is required. Figure 4 shows one example (NWDZ-RF-PA) that covers 2 - 700 MHz and is about $25. This particular unit uses a SBA5089Z amplifier IC and RD01MUS1 MOS FET. However, the MOS FET overheats which, can be corrected by changing the bias on its gate (R6 changed from 5k ohms to 3.3k ohms).

RF Signal Generator

Another tool in our thrifty set is an RF signal generator. The example shown in Figure 5 (TinySA[4]) has an amazing set of capabilities and only costs about $85. Although its main function is that of a spectrum analyzer, we'll use it in testing described in this article as an RF signal generator. The unit has two outputs. The high output is a square wave, which covers 240 - 960 MHz, and the low output is a sinewave and covers 0.1 - 350 MHz. This low output is the one to be used here and is easily configurable by the touchscreen for amplitude (up to -7 dBm, 1 or 10dB steps), frequency, CW, sweep, and modulation.

TEM Cell Variant

Radiated emissions are often the most common issue. In general, near-field probing correlation with EMC lab testing can be poor. Even if near-field probing indicates the potential source of the emissions and a fix is implemented, lab chamber radiated emissions testing may not show any improvement. This is due to the many coupling mechanisms involved from the noise source to the PCB, housing, and wiring harness.

To evaluate radiated emissions, I've used a variation of a TEM cell (see Figure 6a-c) for over a decade. Such an enclosure is required to keep out ambient radiation

Figure 6a: DIY TEM cell variant (front door removed)

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such as AM/FM radio. Although you cannot compare results on an absolute level as those obtainable in an EMC lab anechoic chamber, the use of a TEM cell shows similar trends. For example, if the improvement for a particular fix is x dB, there will be similar improvement in an EMC lab chamber.

This homemade cell is made from HVAC sheet metal ducting available at many home improvement stores. The dimensions are 16 x 16 x 37 inches, with a center plate (without end tapers) of 32 x 13.5 inches. The center plate height is adjustable to accommodate different DUT sizes (default is in center between top and bottom). Figure 6b shows a small opening in the door. This opening is to help isolate the source of the noise (DUT, harness, or both) by allowing placement of the harness outside the TEM cell.

In Figure 6d, looking at the S11 and voltage standing wave ratio (VSWR), it appears that this TEM cell is only useful for frequencies less than about 200 MHz. However, it has been used with success in finding fixes for frequencies greater than 1 GHz. Since we are only using the TEM cell to assess "before and after" results from any fixes, any discrepancies can usually be ignored as long as the DUT and harness locations are controlled (i.e., consistency in DUT positioning and orientation). In an anechoic chamber, the antenna is much farther from the DUT and harness than in this homemade chamber, and proximity coupling with DUT variation is less of an issue.

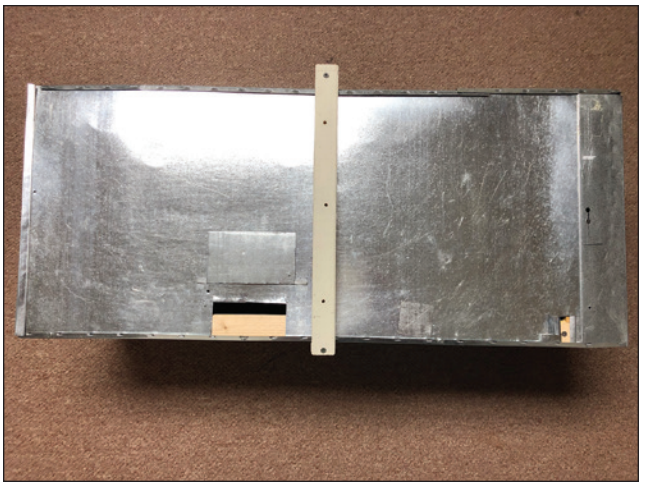

Figure 6b: DIY TEM cell variant (sliding door in place)

Figure 6c: TEM cell variant, end taper and BNC connection detail

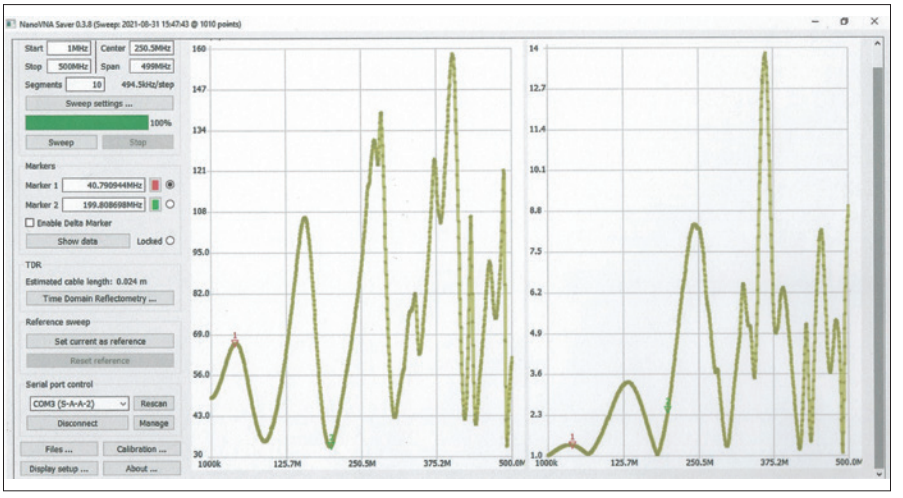

Figure 6d: VNA results for TEM cell (Saver software)

Bulk Current Injection (BCI) Probe

If issues have been identified in EMC lab testing for bulk current injection (BCI), a thrifty method of investigating and possibly solving these issues can be of great value. A low-cost version can be made from a ferrite current clamp as shown in Figure 7a.[5] Using

the VNA mentioned previously in this article, I was able to determine that anything over one turn was detrimental. Figure 7b for one turn shows a reasonable impedance and VSWR, but Figure 7c illustrates how these values get much worse even after just two turns.

Figure 7d shows a calibration setup using a signal generator feeding an RF power amp whose output feeds a 3 dB attenuator and the BCI probe. The induced current is measured with a cheap version of the BCI calibration jig. The voltage is measured across a 50-ohm, 10 dB attenuator leading to the spectrum analyzer. Induced current was measured at over 2 - 350 MHz, and the maximum is about 100 mA rms which is similar to what is required to meet most automotive EMC specifications.

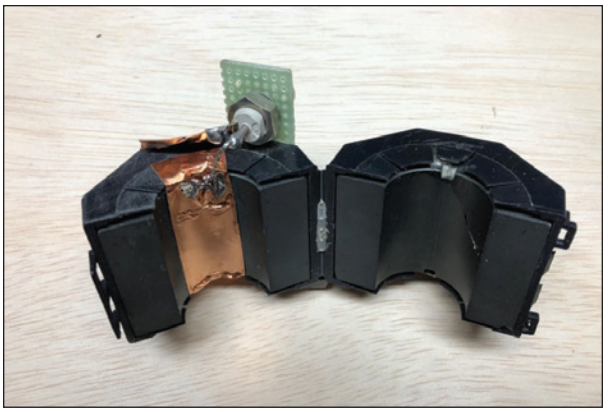

Figure 7a: DIY bulk current injection probe (single turn) for radiated immunity

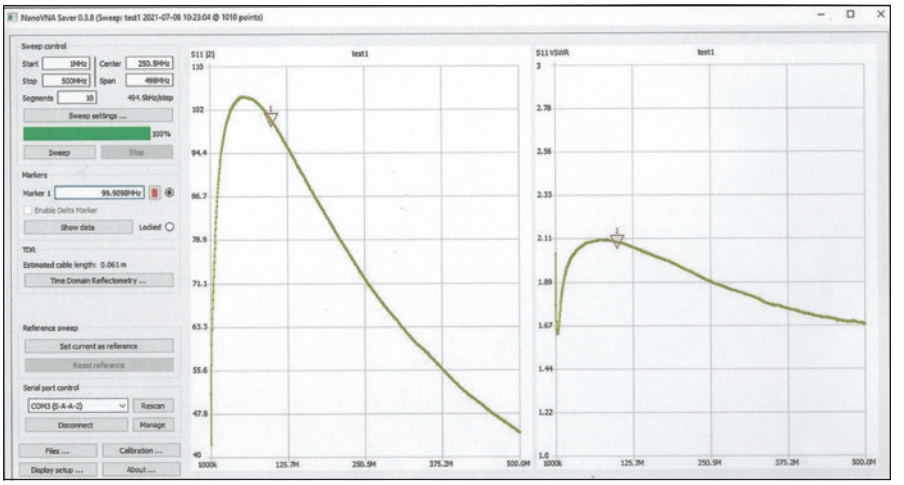

Figure 7b: BCI injection probe (single turn, Figure 7a) VNA measurements

ESD Simulator

A piezoelectric barbecue lighter like that shown in Figure 8a has been suggested as a low-cost ESD simulator. However, based on verification testing I conducted in a commercial EMC test lab, this lighter has much lower energy than a commercial

ESD gun like that shown in Figure 8b, I compared both the piezoelectric simulator and an ESD gun with a calibration target (e.g., IEC 61000-4-2) and high frequency scope. The piezoelectric simulator has no control for magnitude and repeatability. The ESD example in the next section of this article shows that it is important to quantify ESD parameters. Unfortunately, there is no low-cost version of a commercial ESD gun in this case.

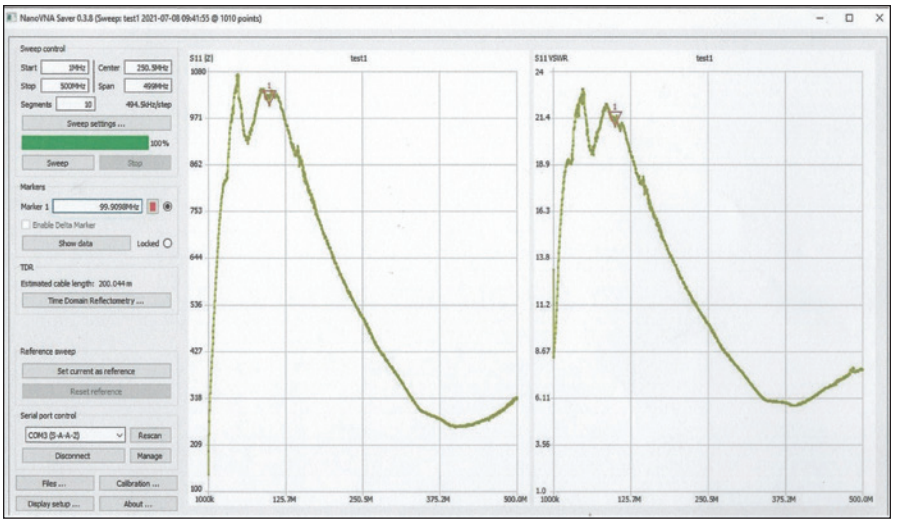

Figure 7c: BCI injection probe (two widely spaced turns) VNA measurements

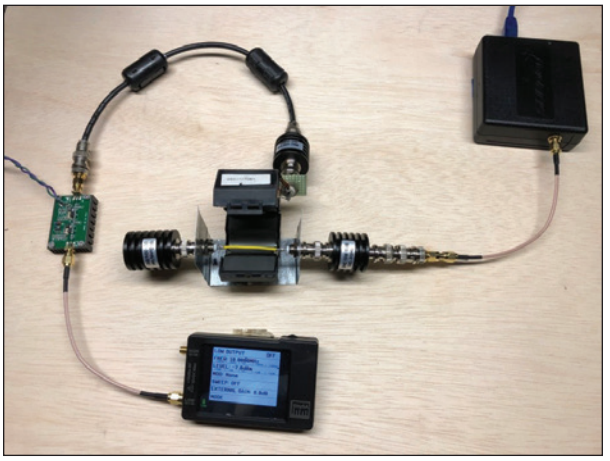

Figure 7d: BCI calibration setup

Figure 8b: ESD gun example

Figure 8a: ESD low-cost simulator

Figure 9a: Example 1—Module A, TEM cell setup

PRODUCT APPLICATION EXAMPLES

Figures 9a-c and Figures 10a-b illustrate thrifty TEM cell results before and after fixes were applied to two different automotive devices. These examples illustrate that the TEM cell setup is valid for a wide frequency range. Before the fixes, neither meet the auto manufacturers' EMC specification limits. But after, they both did as verified in an EMC lab. Figure 9a shows a typical setup with the DUT, wiring harness and battery within the TEM cell.

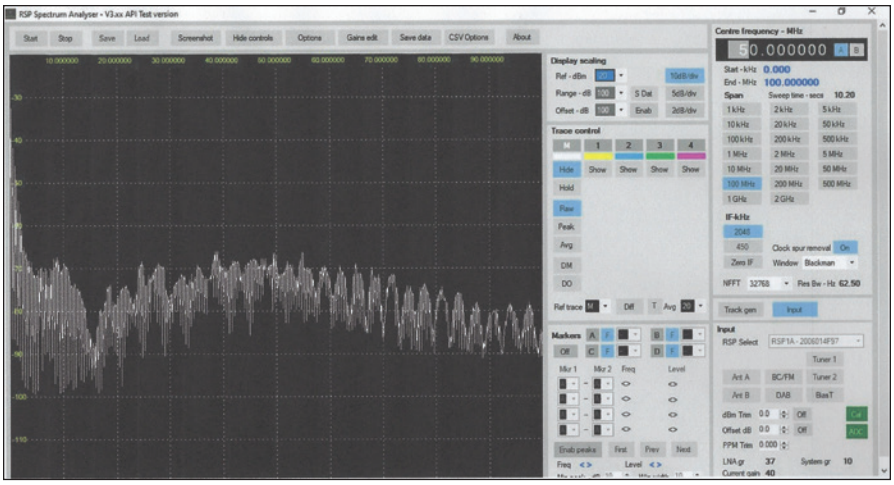

Figure 9b: Example 1—Module A, without fixes, 0 - 100 MHz (20 dB external amp)

Automotive LED Taillight, ESD

This example is based on an actual case in the field. It was originally thought that power line voltage transients were the cause of the issue. We conducted testing using transients specified in SAE J2628.[6,7] These transients are very realistic and severe but could not precipitate the issue.

The next potential culprit was thought to be due to ESD. Testing as shown in Figure 11 (PCB over ground plane) showed that this was indeed the root cause problem. The ESD gun was applied directly to each pin of the suspect IC (air discharge not repeatable). The IC had one pin that had much lower immunity (< 2 kV, one discharge) than the other pins (> 6 kV, multiple discharges). To determine this immunity, many PCBs were *sacrificed*.

SUMMARY AND CONCLUSION

In this article, we've presented a number of effective low-cost (thrifty) test instruments that can be used for EMC testing for both pre-qualification and troubleshooting, along with application examples that validate their usefulness. These options can enable you to resolve design potential issues efficiently without the time and cost constraints of an EMC test laboratory.

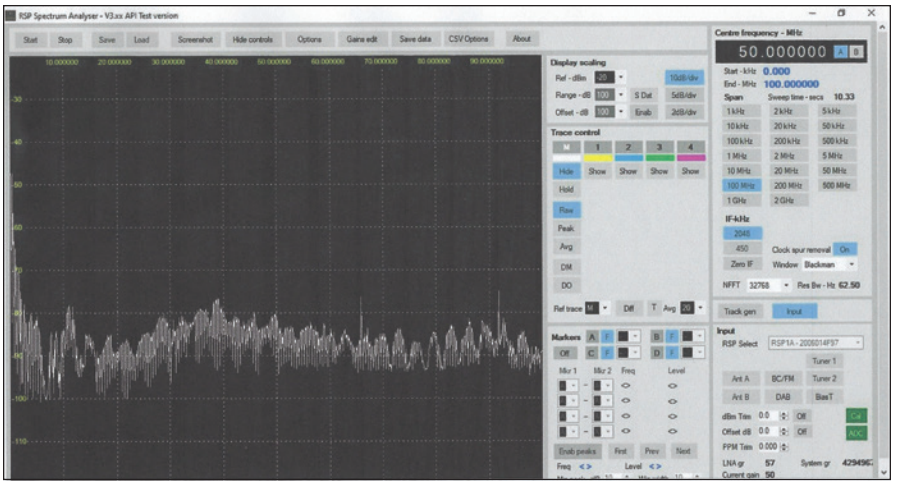

Figure 9c: Example 1—Module A, with EMC fixes

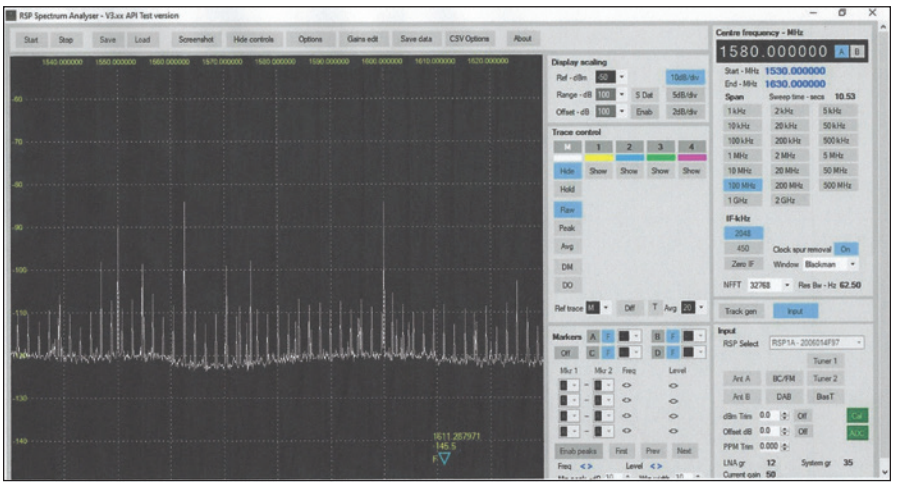

Figure 10a: Example 2—Module B, without fixes, 1530 - 1630 MHz (2 x 20 dB external amps)

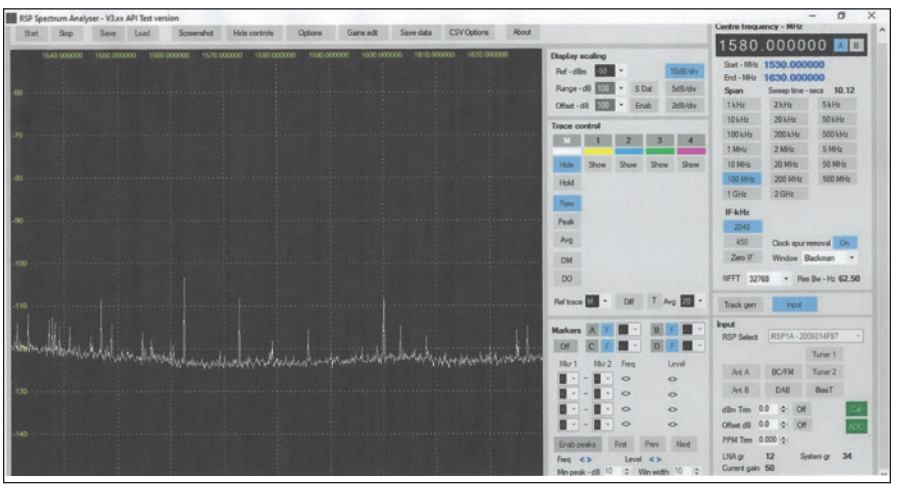

Figure 10b: Example 2—Module B, with EMC fixes

ENDNOTES

1. See, for example, *EMI Troubleshooting Cookbook for Product Designers* by Patrick G. Andre and Kenneth Wyatt.

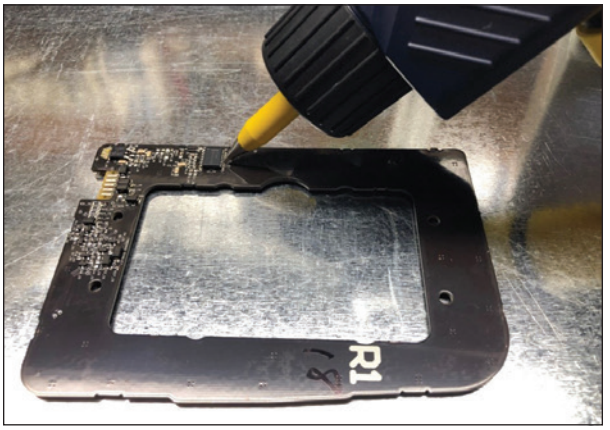

Figure 11: ESD gun applied to IC pins

2. Detailed information about the NanoVNA is available at https://nanorfe.com.
3. Detailed information about the SDRplay is available at https://www.sdrplay.com.
4. Detailed information about the TinySA is available at https://www.tinysa.org/wiki.
5. See "Injection Probe Modeling for Bulk Current Injection Test on Multi Conductor Transmission Lines" by Frédéric Lafon, Younes Benlakhouy, and François de Daran for a cut-away of the BCI probe shown in Figure 7a.
6. SAE J2628, *Characterization, Conducted Immunity.*
7. For a detailed comparison of these transients and ISO 7637-2, see "Comparison of ISO 7637 Transient Waveforms to Real World Automotive Transient Phenomena" by Keith Frazier and Sheran Alles, 2005 IEEE EMC Symposium.

INTRODUCTION TO VALIDATION TEST CONCEPTS IN A MIXED SIGNAL ASIC

Adopting tried and true digital verification techniques to the validation of a mixed-signal power management device

Hang around embedded software engineers long enough and the words design for test or test-driven development will become commonplace. This is because in a world where functionality is ever-increasing in complexity, you need to be able to both verify and validate your device's functionality such that it matches the requirements. And, while these design practices are well understood in digital systems made up of microcontrollers (MCUs) or system-on-chip devices (SoC) with functional safety driving extremely distributed systems, they are just as applicable in low level mixed-signal devices.

Gone are the days where the main MCU of the embedded module is trusted to do everything; in industrial and automotive systems where safety is critical, there now exist other devices to help test the main microcontroller to aid in the safety integrity level (SIL) of the device. These functions vary in complexity and range from helping the MCU toggle pins to ensure stuck at faults are mitigated, to helping verify complex question and answer watchdog issues, and voltage monitoring functionality.

Often the next *smartest* device in the system is either another low-level MCU or, in the quest to simplify a bill of material (BOM), a power management device (a PMIC) with dedicated safety functions. And since these devices don't have flash memory and are traditionally analog in nature, it makes the validation of these devices somewhat challenging for engineers who traditionally focus mostly on transient load responses.

To aid in helping an engineer develop a test philosophy for such a device, we will focus on a distributed system made up of both MCU and

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By Christopher Semanson

PMIC. The article will use this system to demonstrate validation concepts that system designers have been employing for quite some time, the simplest of which is an open loop test philosophy and its strengths and weaknesses. The closed or in-the-loop based test philosophy will address those weaknesses and demonstrate how one can easily expand upon their test setup by including an MCU to model the system or system device. Taking these two test philosophies together will shed light on how exactly a design-for-test philosophy can be adopted for a traditional analog-based device such as a PMIC.

In both these examples, we'll introduce languages and methods needed to be able to easily implement and address. We'll also introduce simple yet effective constructs in C that can be implemented to help with test flow and modularity. In the end, the goal is to help you come up with design patterns that not only focus the validation of basic functionality of the application specific integrated circuit (ASIC) but help emulate the system integration tests during validation to address complexity.

MODELING THE SYSTEM

To best approach how to create a scalable test architecture for an embedded ASIC, an example system needs to be defined. After definition, we then address requirements that are applicable to both the MCU and the PMIC individually and the requirements that are applicable to both devices which ultimately make up the core of the system.

This system is outlined in Figure 2, made up of a high-end MCU, a power management device, along with an external sensor that will monitor throttle position.

The MCU is responsible for sampling the throttle position sensor and then managing the air, fuel, and spark of the engine to ensure acceleration is kept

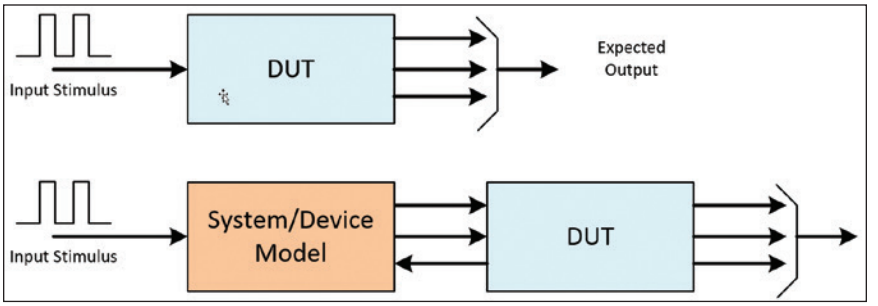


Figure 1: Example of open loop (top) and closed loop (bottom) test setups

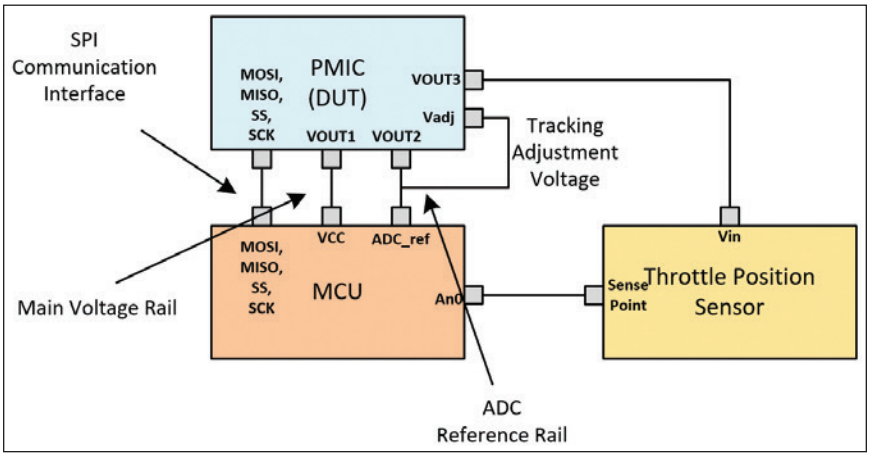


Figure 2: Our example throttle by wire system, with some simple interfaces

constant and smooth; this is defined as a simplified but typical throttle by wire system. The power management device needs to deliver monitored power to both the MCU and the throttle position sensor, assist in monitoring the MCU and system voltages, and alert the system when it is unable to do so reliably.

Each active device in this example, the MCU and PMIC, needs to go through two types of testing prior to starting their task. The requisite testing includes:

1. Internal self-testing - each device undergoes a self-diagnosis to ensure proper operation (typically resulting in an external pin being toggled to let other devices know the state of these tests). This type of test is usually defined as a built-in self-test (BIST).
2. External system requirements - a wide variety of systems tests requiring different devices to properly diagnose interfaces and different peripherals of the microcontroller. These tests are more complex, typically requiring a communications interface between devices which allow the devices to signal when and how a test is to occur.

Taking these two points into account, we'll modify Figure 2 by identifying the critical interfaces that will be used to help validate not only the PMIC but any system requirements that the PMIC must perform to help test the MCU.

In summary, our example system functionality includes requirements such as the ability to:

- Verify pins at startup to ensure critical low voltage pins are not shorted;
- Verify analog to digital converter (ADC) functionality; and
- Verify that the serial interface and internal registers are working properly.

At first glance, this seems like quite the task, as the PMIC is normally focused with only one goal, that is, designing a high-performance regulation loop with a focus on power integrity and not on the validation of embedded functions. Because of this, things like loads and specialized power supplies are the norm for these engineers, but not digital devices such as digital to analog converters (DACs) or MCUs.

When it comes to testing these embedded functions, the focus must be on developing a test setup that allows the PMIC team to ensure that these functions work properly by exercising their pass-fail criteria. Because of the variety of functionality to test, validation can be done in one of the following two ways with low-cost devices that are easy to implement and program:

- Open loop testing, in which the device is commanded to perform a required action and the device demonstrates the acceptance or failure of that test. This is often done without a 'plant' in the system.
- Closed, or in-the-loop, testing, in which the device is commanded to perform an action, such as toggle a pin, and a receiving device confirms the action. This is often done with a *plant*, acting as a model of the system.

We'll start first by explaining some methods for working with the PMIC device in an open loop fashion, where there's no plant device that the PMIC will work with.

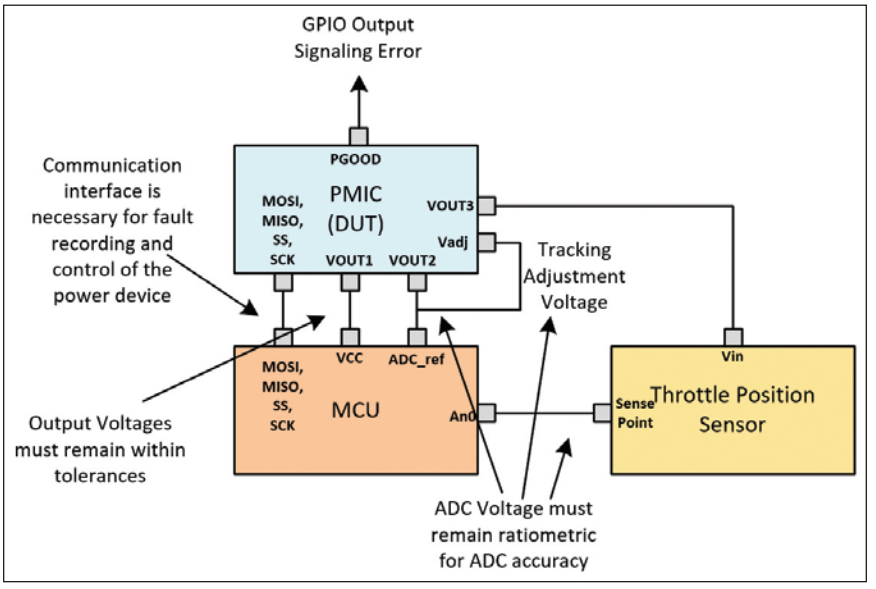
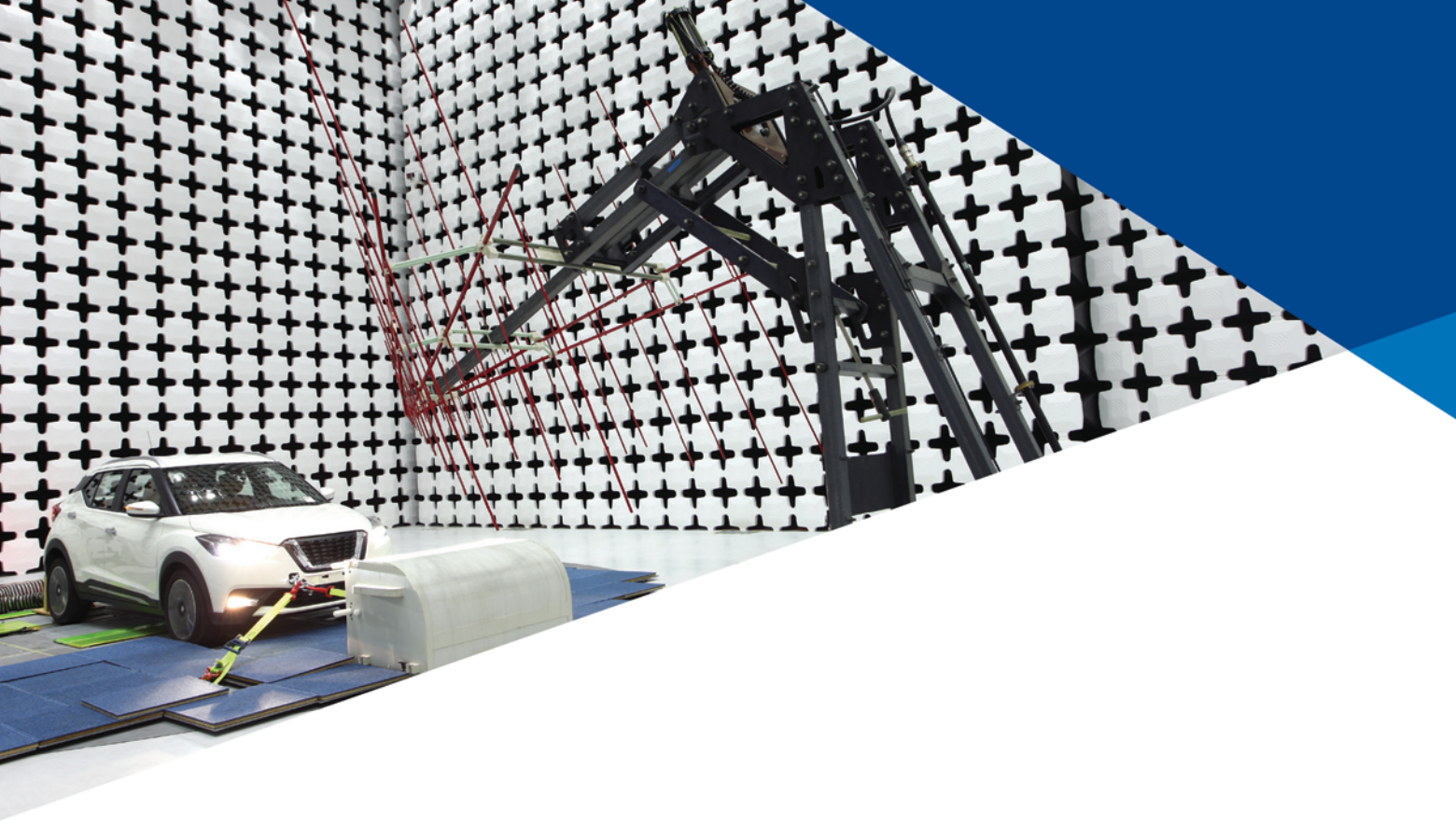


Figure 3: Our example throttle by wire system, with critical interfaces



GOING BEYOND THE STANDARDS OF EMC COMPLIANCY.

The future is here! From driverless vehicles to pizza-delivering drones to ear buds that act as virtual mixing boards for real-world audio, our lives are increasingly dominated by EMC. So, too, is ETS-Lindgren's work in compliance testing and measurement, transcending the standards of EMC performance – Beyond Measure.

As an international manufacturer of market-leading components and systems that measure, shield, and control electromagnetic and acoustic energy, ETS-Lindgren is the driving force allowing some of the biggest industry names, and latest technological advances, to meet compliance standards. From chambers to test cells, absorbers, positioners, antennas, and software, ETS-Lindgren's EMC solutions are designed for reliability, diversity, scale, and precision.

More importantly, our ability to create real-world test scenarios, troubleshoot potential failures, and maximize the chance of passing standards within the allotted time and budget helps our customers bring life-changing products to market – faster.

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INTRODUCTION TO AN OPEN LOOP SETUP

A simple open loop test setup is a valuable tool in an engineer's toolbox, since it allows them to validate communication through an external interface, such as a:

- Input/output pin level, or
- A serial communications interface, such as a I2C or serial peripheral interface (SPI).

Overall, the goal of an open loop setup is to be able to communicate not only to the device under test (DUT, in this case, the PMIC) but to trigger measurement devices to automate as much of the test sequencing as possible. An example setup is found in Figure 4.

Traditionally, higher-end test setups will utilize LabVIEW or MATLAB, but Python (a relatively new, very powerful scripting language) and lab equipment capable of receiving digital commands over a standardized interface is perfectly usable. Regardless of how you set this up, creating an environment that allows a user to communicate and control various devices in sequence is crucial in an open loop setup for automation and repeatability.

In order to demonstrate how to evaluate the effectiveness of our open loop test setup and its ability to interface, we'll examine two system test cases denoted by our example system; they are:

- *Test Case 1:* A fault reaction and accuracy test, where the DUT is cycled through internal codes which correspond to a limit read by the ADC, and the fault reaction is measured via a GPIO pin.
- *Test Case 2:* An external reset command that allows an external device to trigger an internal function inside of the PMIC. In this case, we're validating to ensure that at least one of the three PMIC rails can be reset via SPI.

Test Case 1: Assessing Fault Reaction and Accuracy of the PMIC Device

This test case focuses on the ability of the PMIC to monitor a voltage and issue a fault reaction within a certain time. The example requires the device to react properly under a swept VIN and load to ensure the

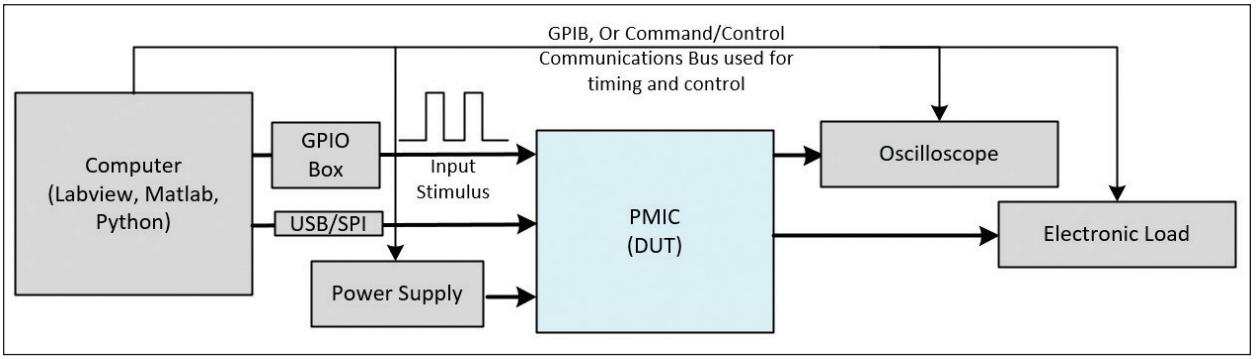


Figure 4: A common open loop bench setup for evaluating a PMIC

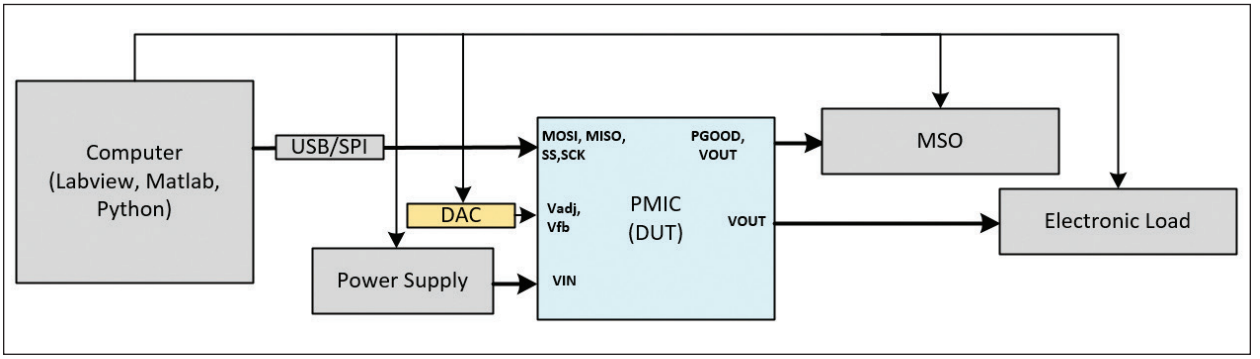


Figure 5: A bench setup used for evaluating ADC accuracy and fault response

accuracy of the converter. To execute this test case, the open loop setup makes use of the following hardware:

- An SPI addressable digital to analog controller (DAC)
- A triggerable mixed signal oscilloscope (MSO)
- A USB to SPI converter
- An addressable power supply
- A programmable load

The sample system is outlined in Figure 5.

While this may seem like a simple setup, the power that comes from this is using them together to run and rerun a test setup using our Python scripting language. With just a few commands in Python, you can program this test setup to:

- Set the MSO to send a specific SPI message to the DAC.
- At the same time, sweeping the VIN voltage with the power supply, and
- Later, command the load to move in and out of the allowable range as you sweep the DAC voltage.

With this setup, we can easily swap in and out different versions of the PMIC or a new board to perform regression testing and to make sure that the design functions from revision to revision.

Case 2: Assessing Internal Behavior of the DUT

As is the case with many PMIC devices that sit in systems that adhere to functional safety standards, most DUTs have internal sensors to monitor various reference points inside the device and a dedicated GPIO to alert the system of an error in one of those sensors. In this case, we assemble the following equipment:

- An MSO capable of triggering off an SPI message from the computer to the DUT, and
- A USB to SPI converter.

The setup is found in Figure 6.

In both of these simplified cases, the validation engineer gains the ability to create an open loop regression test suite that allows them to test new devices and boards with a common test setup. A computer can script these sequences, take screen shots, and log data simultaneously. It is relatively simple to set up, provided your lab equipment includes addressable devices, your validation group opts for a suitable software license, or opts to control these devices via Python.

However, where this setup falls short is in the modeling of an actual embedded system. The assessed functionality is limited to just the DUT and the actions of the DUT in response to directed stimuli and does not include the interaction of the DUT with the accompanying MCU in response to those stimuli. For that, we turn to a closed loop setup or a system model.

INTRODUCING A CLOSED, IN-THE-LOOP SETUP

Traditionally, validation engineers of ASIC type devices focus on simply validating the device in an open loop fashion. For example, for a simple regulator, they are most likely concerned with:

- How does the control loop function in the presence of a load step? Or,

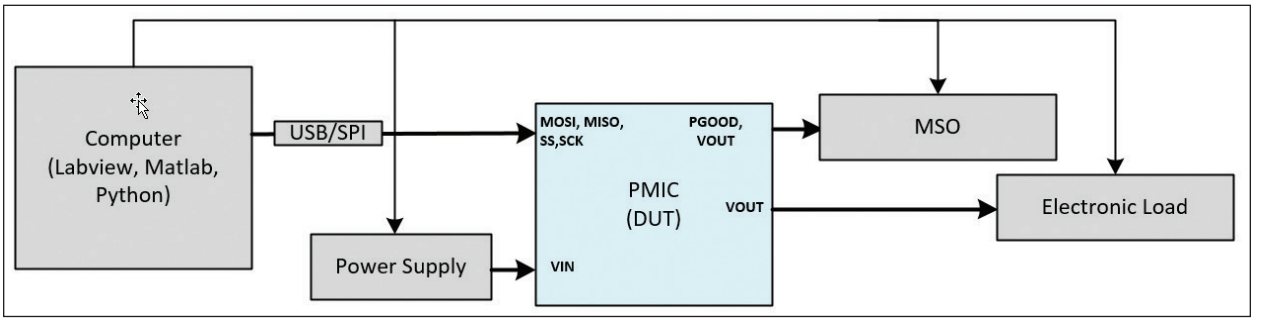


Figure 6: A bench setup used for evaluating fault reaction and response

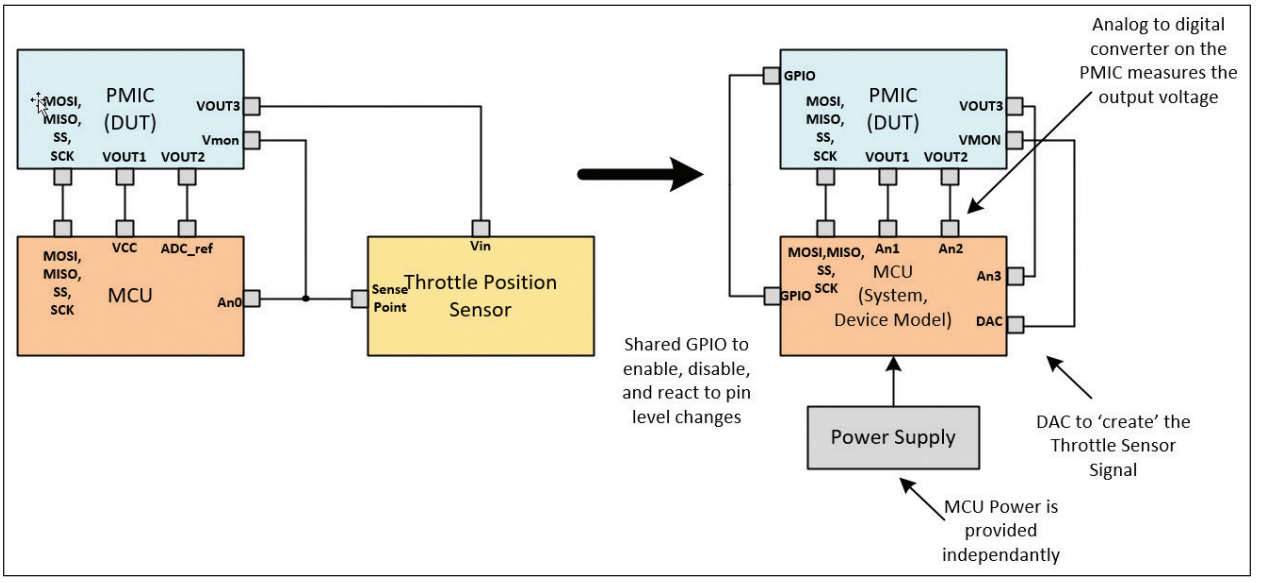


Figure 7: Modeling our system using a PIL method

- How does the controller function with a varying input voltage?

Both of these examples employ a simple oscilloscope and power supply, with an engineer performing a manual evaluation of the setup. However, in a mixed signal design that is highly integrated with a microcontroller, this approach is limited. To address this, we turn to a model of the system with the MCU in it. There is a wide variety of ways to accomplish this, including:

- Model in the loop (MIL) or software in the loop (SIL), in which a software model of the system is made and exercised based on requirements;
- Processor, or MCU in the loop (PIL), in which a processor is used to create stimulus and measure reactions, based on the requirements to the system; or
- Hardware in the loop (HIL), in which the actual target hardware used is similar to that of the end system.

In the rest of this article, we'll consider a closed loop PIL approach which is typical of a system validation that is now becoming more commonplace at the device level.

An MCU offers the example test system a lot of freedom in how to evaluate. Among the many advantages are:

- It can offer breakpoints in the code execution, meaning that you can look for complex interactions and break when the MCU encounters them. These can come in the form of common hardware breakpoints or test assertions.
- It has built-in peripherals such as high-speed timers, DACs, analog to digital converters, and a wide variety of communications interfaces to help exercise the DUT.
- It offers memory that allows the device to sit and buffer results and store them or print them to a UART for easy data logging.
- It is largely independent of user interaction, meaning that once programmed, it can run without being monitored for long periods of time and sometimes even indefinitely.

Quite possibly, the most attractive part of an MCU is that evaluation boards that allow access to the functionality do not necessarily need to be the end target hardware and thus can be much less expensive and easier to program.

In our example throttle-by-wire system, the addition of the microcontroller allows us to introduce more complex test scenarios. Two examples of these more complex scenarios are:

- Like our open loop fault reaction test, we can now interact with the microcontroller and test fault reaction and recovery of the PMIC/MCU system to an externally triggered fault, while varying the input voltage to the system.
- We can also test the interaction between the MCU's internal watchdog and the PMIC's ability to reset the MCU in the case of a watchdog error.

Now that we have the microcontroller and a concept of what a closed loop evaluation system can offer us, we need to discuss some strategies that go into creating firmware to facilitate a state driven test environment.

HOW TO EXPAND UPON A CLOSED LOOP SETUP WITH A PROGRAMMABLE DEVICE?

Now that we've defined what a closed loop validation system is, our MCU firmware needs to be written so that it takes full advantage of the environment. This means that the validation engineer needs to implement design patterns for testing that influence:

- How the MCU/PMIC interaction controls execution order (here we introduce a concept called state driven testing); and
- How the MCU/PMIC interaction can implement modularity in terms of testing modularity such that we're able to take different execution paths in the same function. This specifically addresses requirements of ensuring that a mechanism or function demonstrates pass-fail functionality.

Taking these into account, we'll now discuss some embedded C-level constructs that can be used in order to control execution and to address our modularity requirement. Together, these will give us a great amount of flexibility in debugging and regression testing.

State Driven Test Environment

First, we introduce the concept of a state driven test environment through the use of a common design

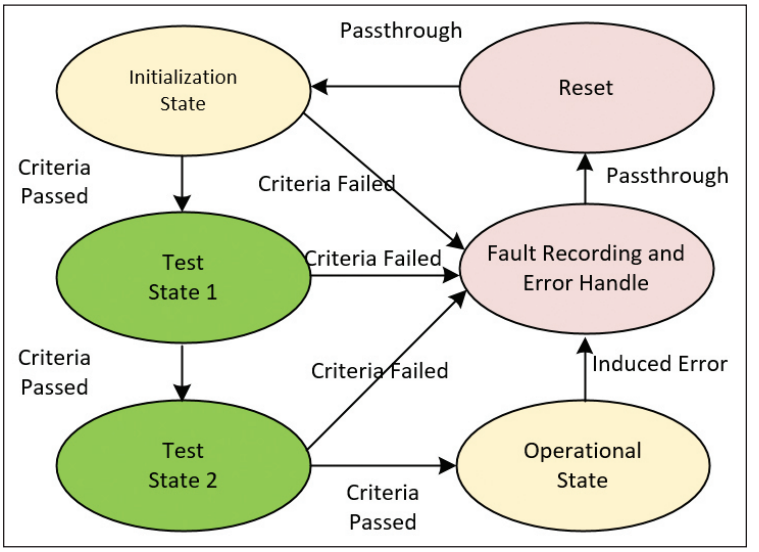


Figure 8: A state diagram depicting initialization tests ran on the MCU in a closed loop model

```
switch (test_state_hdl.next_state) {

        case D_TEST_STATE_INITALIZATION:
                v_state_initialization(&test_state_hdl);
                break;

        case D_TEST_STATE_TEST_1:
                v_state_test_1(&test_state_hdl);
                break;

        case D_TEST_STATE_TEST_2
                v_state_test_2(&test_state_hdl);
                break;

        case D_TEST_STATE_DEVICE_ACTIVE:
                v_state_device_active(&test_state_hdl);
                break;

        case D_TEST_STATE_DEVICE_FAULTED:
                v_state_fault_record(&test_state_hdl);
                break;

        case D_TEST_STATE_DEVICE_RESET:
                v_state_device_reset(&test_state_hdl);
                break;

}
```

Figure 9: An example design pattern of a state machine in C

pattern found in digital and embedded systems, the state machine. A state machine is a design pattern that allows the designer to organize functions and behavior by defining and tightly controlling the states of a system. It is commonly found in the negotiation of ethernet handshaking, or the internals of a CPU.

An example, depicted in Figure 8, is a state diagram that outlines the startup and initialization tests between the two devices in our example system, the PMIC and the MCU.

The diagram conceptually organizes the execution pattern into individual functions, with pass-fail criteria that allow us to control the flow of execution. This concept is extremely powerful in our validation environment because of how the system's functionality is distributed between the PMIC and MCU. Otherwise, it would be difficult to understand where the PMIC (or any other ASIC, without a debugging environment) is in its internal processes.

This design pattern is borrowed from a universal verification methodology (UVM). With this context, we can define a finite state machine as a computational model used to simulate sequential logic in a 'stateful' means. It allows abstraction of a complex series of events to a series of states to control execution flow.

The implementation is usually done in C and follows a design pattern similar to that in Figure 8. An example of its instantiation is shown in Figure 9.

The state machine is in control of the order of execution and driving a test to a specific operating point, an approach best suited for forcing the PMIC/MCU interaction through a series of defined steps with each state transition gated by a test assertion.

For example, for the system to move from the initialization state to a communications interface state, the combination has to match the expected behavior. If it does, this successfully satisfies the *pass* case. Otherwise, the test would signify a failure and the *fail* case would be able to be validated.

Another example, shown in Figure 10, demonstrates how the state machine can control the order of execution to a finite end.

The MCU needs to command the PMIC to dynamically change voltages (this is commonly referred to as DVFS), require the PMIC to detect a fault which would then reset the system, and then allow it to recover from a faulted state.

By implementing this concept as a state machine, depicted in Figure 11, the system can easily validate both the *pass* case, in which the system recovers, as well as the *fail* case in which the system goes to an error state.

However powerful state machines are in controlling execution, the validation of these requirements often require the need for a pass and fail case to be tested. And while an individual can copy their firmware, if they adopt modularity in the design of their test cases, they would easily be able to reuse work need to address both the concepts of modularity and program control.

How to Simplify the Test Case Implementation in a State Machine

As we alluded to in the previous section, our validation setup will often need to validate both the pass and fail paths. And while there are several different ways to address this, one overlooked function in C is compile time build options.

In production environments, build options (sometimes referred to as compile switches) are a powerful tool to create modularity in firmware for building various embedded targets or multiple applications. Inside a disciplined organization, multiple people using the same compile switch can reconfigure an entire application by compiling large sections of data in and out instead of creating, tracking, and supporting new firmware variants.

However, in a state driven test environment, the goal is not to be memory efficient but to be able to support a wide variety of test cases in a single design pattern to take advantage of the software architecture choice. To demonstrate how powerful these test cases can be, we present two test cases in which our embedded system model needs to perform a test of:

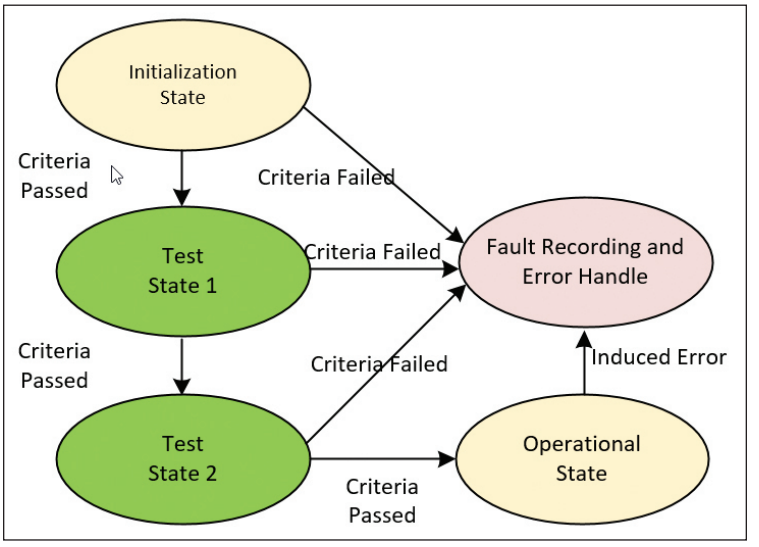


Figure 10: A state diagram depicting the startup sequencing of a PIL based system

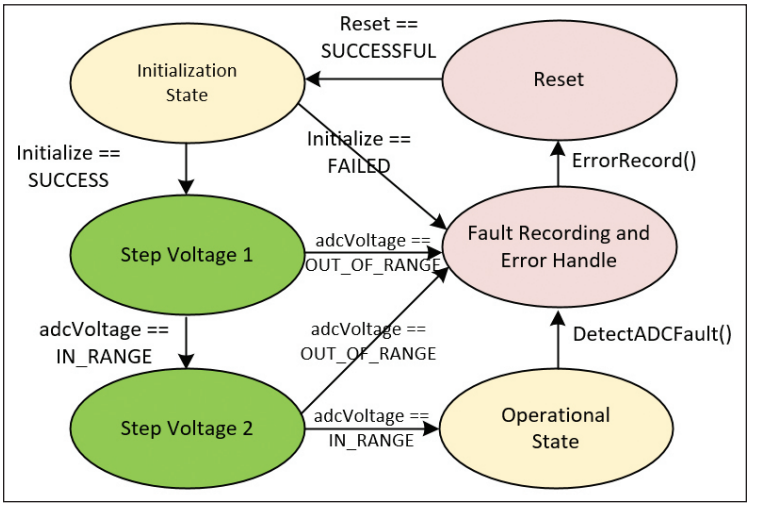


Figure 11: A state diagram depicting the startup sequencing of a PIL based system

- The watchdog (WDT), including both a simple window watchdog function and a challenge-response watchdog; and
- An external pin toggle, in which the MCU commands the PMIC to toggle a GPIO and the MCU would be forced to acknowledge it.

In the case of the watchdog, the state diagram is depicted in Figure 12. We can easily reuse our main, non-finite state machine to step the system to the watchdog interface validation test, and then use compile switch to examine the simple window watchdog case, followed by the challenge-response watchdog case.

Additionally, we could create a pass/fail compile time switch that would validate the *pass* test case and the *fail* test case inside of each function.

In the case of the external pin, we simply create three functions:

- We toggle the pin high, then low, and observe the expected response.

```
      case D_TEST_STATE_WDT_TEST
#if ENABLE_4QA_WDT
            v_test_state_4qa_wdt (&test_state_hdl);
#elif ENABLE_16QA_WDT
            v_state_state_16qa_wdt(&test_state_hdl);
#elif ENABLE_WWDT
            v_state_state_wwdt(&test_state_hdl);
#else
            v_state_wdt(&test_state_hdl);
#endif

      break;
```

Figure 12: Pseudocode for a WDT test with conditional compilation

```
2     case D_TEST_STATE_TOGGLE_PIN1:
#if TOGGLE_PIN_1_PASS
            v_state_test_1_high_low(&test_state_hdl);
#elif TOGGLE_PIN_1_FAIL
            v_state_test_1_simulate_stuck(&test_state_hdl);
#end
            v_perform_pin2_fault_reaction();
            break;

      case D_TEST_STATE_TOGGLE_PIN2:
#if TOGGLE_PIN_2_PASS
            v_state_test_2_high_low(&test_state_hdl);
#elif TOGGLE_PIN_2_FAIL
            v_state_test_2_simulate_stuck(&test_state_hdl);
#end
            v_perform_pin2_fault_reaction();
            break;
```

Figure 13: A state diagram depicting the startup sequencing of a PIL based system

- We do not toggle the pin at all, simulating a pin stuck fault due to a solder short, and observe the expected response.

In each of these toggleable situations, demonstrated in Figure 13, the reaction to the fault is organically used, and the compile switch is used to create a fault.

However, this C construct is not without risk. The main dangers of overuse of these build switches is their complexity and the ability to document them, especially when they appear in various sections throughout the validation application. Overuse and poor discipline can create a complex set of decisions that are difficult to maintain, let alone pass to another validation engineer. To combat these, we suggest to:

- Refactor the code often as new test cases and functionality are created, with a focus on making each function and test atomic so each compile switch is localized.
- Document the flow of the test as you develop your validation firmware. Something as simple as a test flow chart, for example, can be invaluable when ensuring the firmware is designed properly.

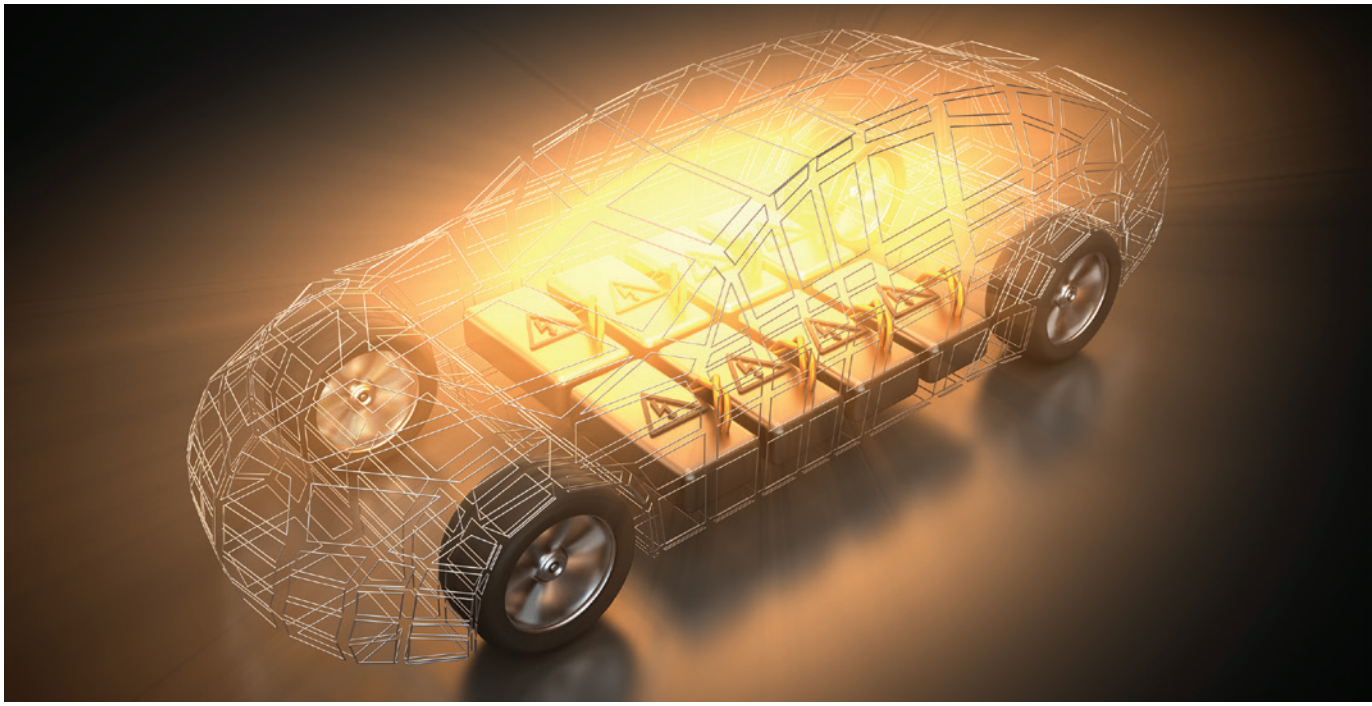
CONCLUSION

Validation of traditional, analog-based devices is becoming much more complex with the advent of highly integrated systems. Digital functions like watchdog timers, pin checking, and ADCs are finding their way into mixed signal devices and their functionality needs to be exercised as rigorously as the analog control loop. Using an open loop test setup, an engineer can get a jump on the validation using some simple scripting tools or more expensive, off-the-shelf ones. But quickly, they may find limitations in that approach, depending upon how deep their validation plan takes them.

By implementing a state driven test concept in a closed loop system with a model of the target embedded device, you can achieve higher validation coverage and create a method to help identify and fix those hard-to-catch bugs before release!

EMC DESIGN TECHNIQUES FOR ELECTRIC VEHICLE DC-DC CONVERTERS

Three Important Design Aspects You Must Get Right Before Designing a Converter



When helping clients in the automotive industry with their DC-DC converters to meet the stringent automotive EMC standards, I often find problems that share some common mistakes. For a start, 90% of the EMI issues are associated with a *grounding* issue. Poor DC link design contributes to poor conducted and radiated emissions. Another commonly seen mistake is a bad choice of switching devices, which often requires adding more filters later in the design process, significantly increasing costs and potentially jeopardizing the project.

When it comes to designing an electromagnetic (EM) compliant product, some planning is crucial to help ensure product performance and keep costs under control. In this article, we offer three recommendations addressing design aspects of DC-DC converters that will make a huge difference in their EMC performance.

THE ROLE OF DC-DC CONVERTERS IN ELECTRIC VEHICLES

If powertrain modules determine the performance of an electric vehicle (EV) [1], DC-DC converters then play an important role in the stability and reliability of an EV. Their primary function is to transfer energy from a source (e.g., battery pack) to systems and devices that consume that energy (all electronics loads, particularly in the low voltage distribution network of a vehicle). Because of this, the safety and functional safety aspects of a DC-DC converter are also critical. Redundancy design can also be seen for fault tolerance purposes.

Dr. Min Zhang is the founder and principal EMC consultant of Mach One Design Ltd, a UK-based engineering firm that specializes in EMC consulting, troubleshooting, and training. His in-depth knowledge in power electronics, digital electronics, electric machines, and product design has benefitted companies worldwide. Zhang can be reached at info@mach1desgin.co.uk.

Dr. Min Zhang

There are generally two types of DC-DC converters for automotive applications. As shown in Figure 1(a), for a pure battery electric vehicle (BEV), a DC-DC converter replaces the alternator typically used in an internal combustion engine (ICE) vehicle. It steps down high voltage (HV) to low voltage (LV). The power rating of such converters is often around 3 kW.

For a hybrid vehicle or a plug-in hybrid vehicle (PHEV), a smaller power DC-DC converter (often below 1 kW) transfers power between the 48V and 12V power rails. This type of converter is often bi-directional, enabling power to go in both directions. A 48V power rail is needed for functions such as power steering, power braking, jump start, etc. Often on the 48V power rail, supercapacitors can be used to provide extra power for a very short period. This can be seen in Figure 1(b).

Due to the nature of high voltages and their associated safety requirements, isolation is required for HV-LV DC-DC converters. Such converters are often used with transformers since the transformer provides the isolation required. Popular topologies include phase-shift full-bridge converters and LLC resonant converters. For 48V-12V DC-DC converters, often due to the cost and size requirements, simple converter topology such as a bi-directional buck-boost converter is a popular option. In order to share the power of components, interleaving is commonly seen for both types of converters. Schematics of a phase-shift full-bridge converter and a bi-directional buck-boost converter can be seen in Figure 2 on page 32.

The EMC challenges associated with high voltage, high switching frequency, and fast rise time are introduced in [1]. An EMC design guide for automotive DC-DC converters can be found in [2]. In this article, we will look at the three most important design aspects that design engineers must get right in the first place to avoid the financial impact of multiple iterations of the design.

GROUND PLANNING – FIRST STEP OF A GOOD EMC DESIGN

For years, EMC experts have been emphasizing the importance of having one *ground* [3]. D. Beeker jokingly said that "when an EMC expert sees

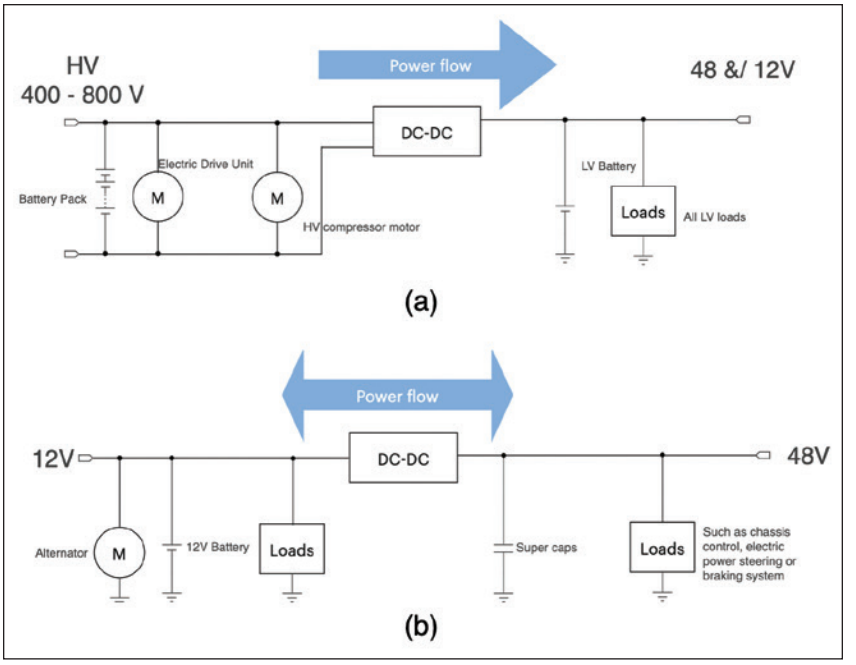


Figure 1: Two types of DC-DC converters for automotive applications

schematics of more than one ground symbol, he/she knows that there's money to make." [4]. Still, in the field, we have seen so many designs that have multiple ground symbols. They are sometimes wrongly connected or not connected to anything (as an islanded plane). But most of the time, they have connections to a reference point through a very high impedance path. Statistics drawn from our own research suggest that over 90% of the EMI issues in the automotive world are related to bad grounding design [5].

Here is a list of some commonly seen ground-related issues, which sometimes have been wrongly referred to as *black magic*.

- When adding more capacitors between the chassis reference and the 0V reference, the conducted/radiated emissions become worse;
- The converter is subject to transient immunity test, including ESD; and/or
- The converter is subject to bulk current injection (BCI) failure.

There is no such thing as a *clean* or *quiet* ground. But there's an RF reference where the EMC measurement is taken. For an automotive DC-DC converter, it's the chassis reference. Ideally, the filters (input and output) need to be designed using this reference. However, this cannot be achieved for many reasons, such as galvanic isolation, leakage current, and other requirements from the OEM, etc. Therefore, connections to this reference will need to be a low impedance path for the EM noise of concern.

To avoid confusion, the use of terms such as *ground* or *earth* are not encouraged for design. Rather, we use 0V reference (or low voltage return), chassis reference, HV (–) to name our design reference. Apart from a solid continuous ground plane for the 0V reference, using a chassis reference on the PCB is a good practice. However, the chassis reference needs to be a solid continuous plane rather than a thin trace labelled as *chassis*.

In Figure 3, a ceramic capacitor is connected between a 0V reference (or what we call low voltage power return) and a thin trace on the PCB called 'chassis,' that same trace runs to a mounting hole that is connected to the metal enclosure via a stand. The problem of this is that long connections increase the current loop area; hence the inductive part of the connection begins to dominate as the frequency increases [6]. What seems to be a low impedance path becomes a high impedance path, potentially occurring at exactly the frequency point where one would like to achieve good attenuation, thereby defeating the purpose of the common-mode capacitors.

Using a large number of filter components to achieve EMC compliance is never a good option. For one

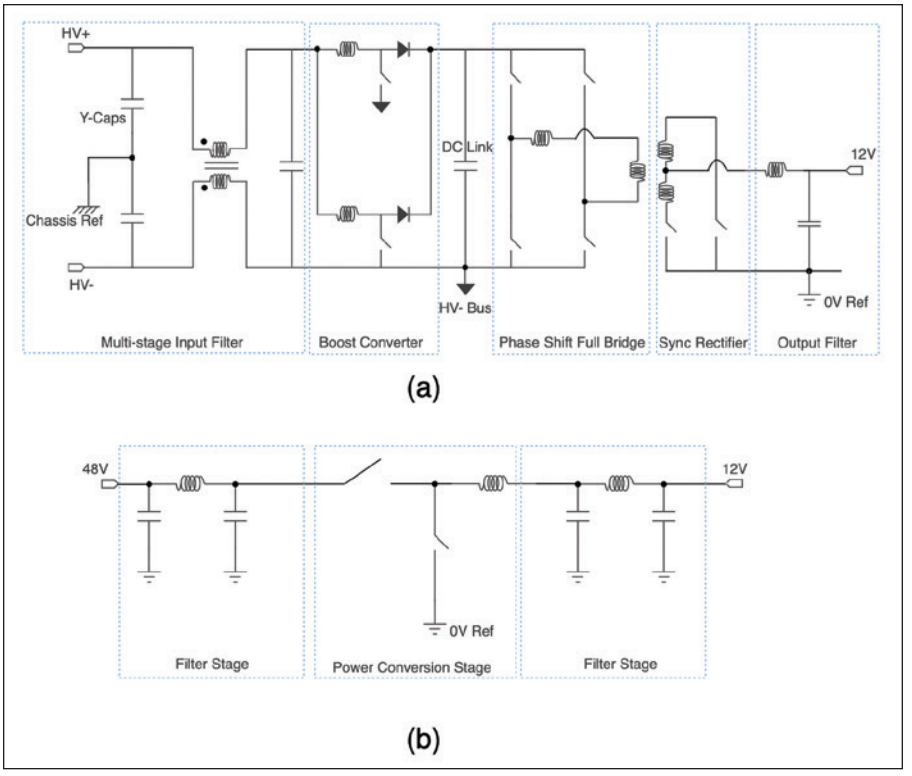


Figure 2: Simplified schematics of (a) a phase-shift full-bridge converter (b) a bi-directional buck-boost converter

thing, it increases the size and cost of the system. It could also increase the instability due to an undamped filter. If the 0V reference and/or the chassis reference are not designed properly, adding filters can also cause an imbalance in a transmission line, particularly when a ferrite bead is used to join two reference planes. For a compact design, a quiet zone for reference plane (such as 0V reference) is often required, which means placing the filters and connectors on the opposite side of the reference plane.

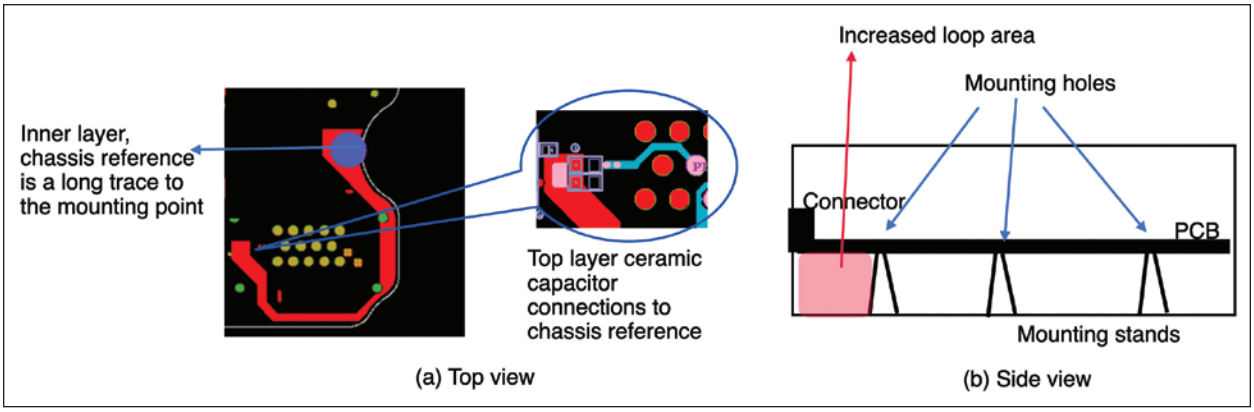


Figure 3: Long connections to the final chassis reference increase impedance

If a perimeter fencing technique is used on the PCB (as shown in Figure 4), the perimeter will then need to have a good electrical connection to the metal enclosure as well. A preferred approach here is to use an EMC gasket and press it against a high-conductivity surface treatment or plating that is galvanically compatible with the EMC gasket material. Clamp the top and bottom chassis traces all around the edge of the board and between two continuous metal walls - one on the top, one on the bottom - a so-called *clamshell* type of construction. This approach benefits significantly from having EMC gaskets on the top and bottom of the board. Otherwise, the EMC performance won't last very long in real life [7].

Ground planning needs to be done at the very early stage of research and development. The number of mounting points not only depends on mechanical requirements but also on EMC requirements. Once a mechanical design is fixed, it cannot be easily changed later in the development stage because of the high cost associated with the tooling fees.

DC LINK CAPACITORS – MORE IMPORTANT THAN YOU THINK

Compared with applications such as grid-tied inverters of motor drives and cascaded mains power supplies like boost-LLC converters, the DC link capacitor of a DC-DC converter doesn't need to have much energy density because power is drawn from a much higher energy density source, i.e., the battery. This explains why electrolytic capacitors are not commonly seen in such applications. DC-link capacitors for DC-DC converters consist of film and ceramic capacitors due to their low ESR and fast energy response characteristics.

The design of a DC link requires careful system analysis, and many factors need to be considered. From the EMC point of view, voltage and current ripples on the DC link are key indicators of how good the design is.

The following process is often recommended when it comes to the DC link design, and a SPICE-based simulation model is often built to assist the analysis.

1. Calculate/simulate the input current under a worst-case load scenario (duty ratio and load impedance

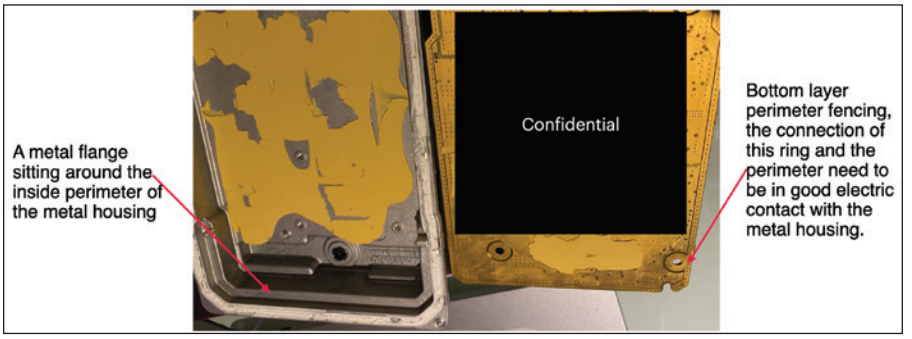


Figure 4: Perimeter fencing needs to have a good electrical contact with the metal housing

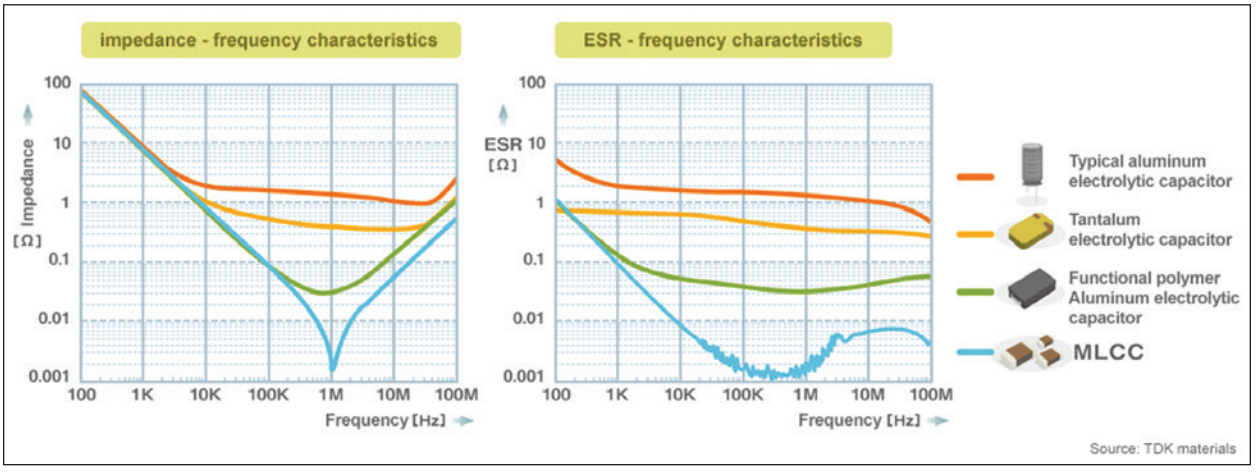


Figure 5: Characteristics of different types of capacitors (Source: TDK material)

dependent) of a DC-DC converter. For this exercise, the voltage source can be treated as an ideal voltage source, i.e., with zero impedance for simplicity.

2. Calculate the source impedance. For a DC-DC converter, this means the battery internal impedance model needs to be obtained. If it is an HV battery pack, then it is the battery pack (number of cells together with their internal connections) impedance that matters.
3. Cable impedance caused by both the cable itself and the wiring harness needs to be correctly modeled [8]. The important factors here are the coupling factor L_{eff}, which is an estimated effective loop inductance per meter and the mutual capacitance between the cables. A simulated result of cable impedance can be seen in Figure 6 on page 36.
4. Once the source impedance and the cable impedance model are obtained, the input current harmonics can then be assessed. The results will then decide how much capacitance and what type of capacitors are needed for the DC link.

It is important to emphasize the necessity of correctly modeling the battery and the cable impedance. Ignoring the accuracy of the model often wrongly leads to the conclusion that a significantly large capacitance value will be needed. This leads to over-engineering and increases the cost and size of the unit. Cable impedance, or more precisely, cable inductance also affects the transient behavior of the system.

Electrolytic capacitors often have larger equivalent series inductance (ESL), which means the impedance starts increasing after 500kHz. Therefore, they are not the best candidates for high switching frequency

converter applications. Another reason that electrolytic capacitors are not preferred is their current ripple handling capability. When the ripple current exceeds the capacitor limit, it can lead to temperature rise and reduce the lifetime of the electrolytic capacitors.

Therefore, the right choice is to have a mixture of film and ceramic capacitors to achieve a low impedance across a wide frequency range (10 kHz – 100 MHz). In order to prevent an undamped system from resonating, damping resistors are often required. Figure 7 shows the impedance characteristics of the DC link by simulation.

Last but not least, the layout of capacitors needs to be carefully considered. When it comes to switched mode converters, the location of the capacitors determines how efficiently energy can be delivered from one side to the other [6]. Connections between the capacitors and the power and ground plane need to be kept short

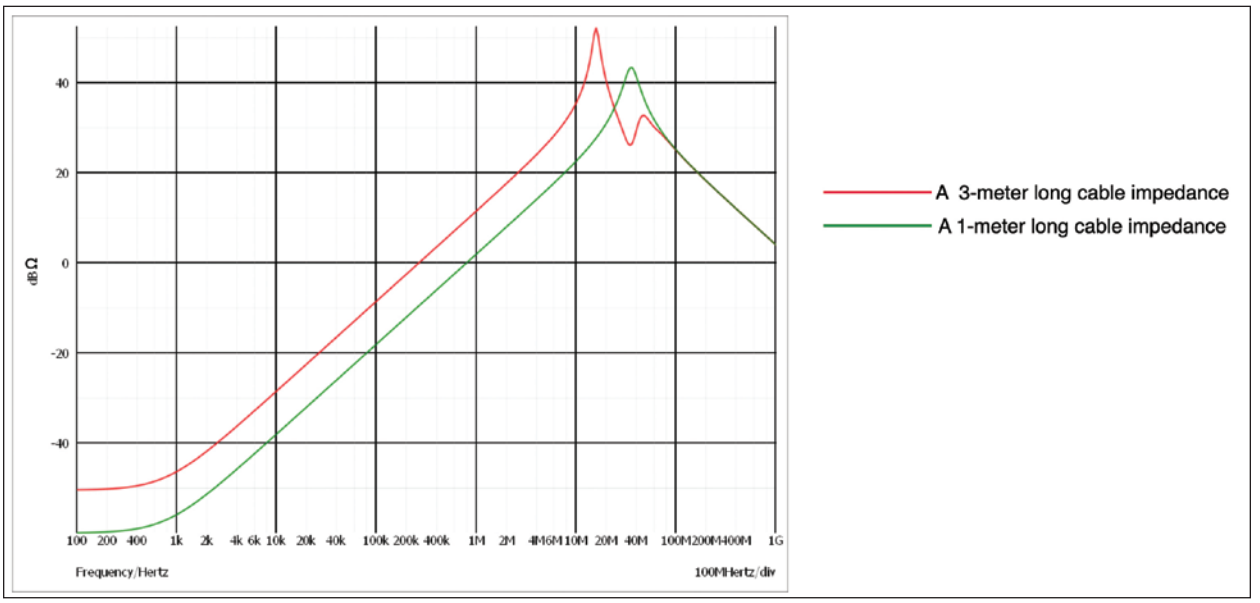


Figure 6: Simulated cable impedance, red trace – 3-meter long, green trace – 1-meter long

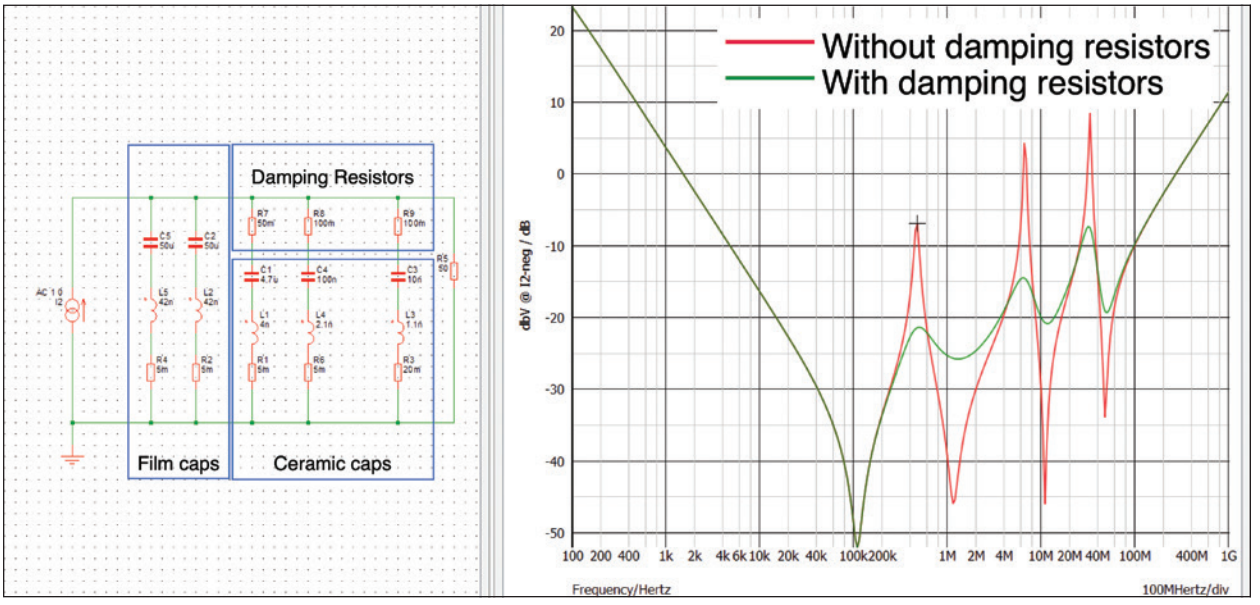


Figure 7: A network of film and ceramic capacitors with damping resistors

so as to minimize the inductance [6]. Depending on the converter topology, hot loop areas need to be identified and minimized to the extent possible.

COMPONENT SELECTION – RETHINK HOW YOU CALCULATE THE BOM COST

For DC-DC converters, power electronics devices such as MOSFET, IGBT, and SiC MOSFET are the key components. With power electronics devices getting faster, the selection of these components becomes important [1].

Design engineers often select a device based on its voltage and current rating, $R_{DS(ON),}$ diode reverse recovery charge, avalanche, and thermal performance. Cost is also a key factor in making a decision since automotive manufacturing is a high-volume manufacturing business.

From an EMC point of view, we often focus on:

1. The capacitance of the device (mainly output capacitance Coss)
2. Reverse recovery charge of the body diode
3. Gate drive circuit performance
4. Parasitic inductance caused by device package
5. Temperature, deadtime impact

Capacitance of the Device

The parasitic capacitance is associated with the device package and the way the device is mounted on the PCB. Generally speaking, the parasitic capacitance due to the mounting (around 100 pF) is at least one order of magnitude less than that of the device itself (around a few nF). The capacitance of the device needs to be considered because it generates the ringing of a switching event together with the parasitic inductance.

Reverse Recovery Charge

The EMC impact of reverse recovery charge of a body diode is discussed in detail in [9].

Gate Drive Circuit Performance

A weak gate driver circuit can affect the switching performance of a converter. The miller capacitance of a device means a gate driver circuit should be designed to quickly charge and discharge the gate to source capacitance. A weak driver circuit often slows down the switch. This is bad news for system efficiency (as the

switching loss increases), but often good news for EMC (as the rise/fall time increases). However, under certain circumstances, such as utilizing zero voltage switching (ZVS) of a resonant converter, a weak gate driver circuit slows down the switching. The converter doesn't finish switching until the voltage is too high and, as a result, the ZVS is lost. When this happens, one would expect the EMC performance becomes worse.

Parasitic Inductance Caused by Device Package

The trend from through-hole packages to low-cost surface mounted device (SMD) applications is marked by the improvement of chip technologies. "Silicon instead of heatsink" is, therefore, possible in many cases [10]. There are cases in which through-hole packages such as TO-247 devices were selected for high-voltage, high-power DC-DC converters. There are three main reasons for doing so. First, a through-hole package is a lot cheaper than an SMD type. Second, it makes thermal design a lot easier, as one can put heat sink directly to the devices. Third, it frees the printed circuit board area horizontally, though it does increase the height of the board.

However, a through-hole package is certainly not good for EMC. In fact, it is extremely difficult to contain the noise that is associated with through-hole

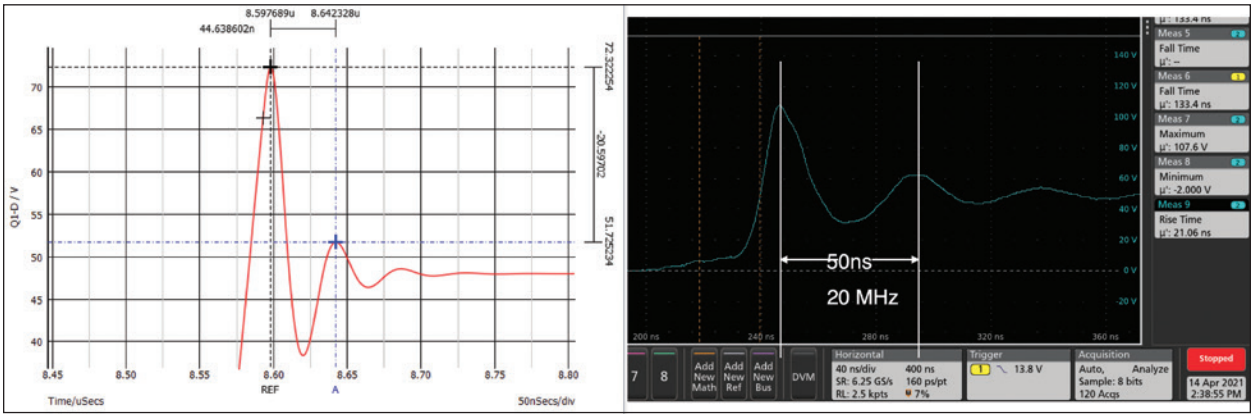


Figure 8: Over-shoot and ringing observed from both simulation and measurement

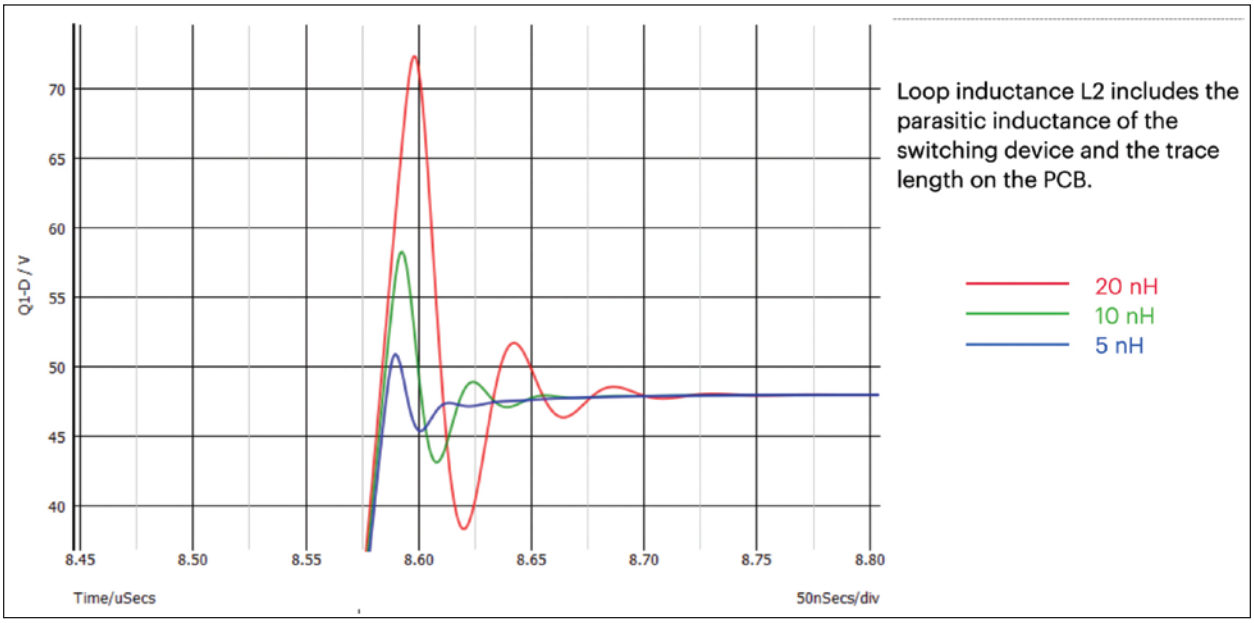


Figure 9: Reducing the inductance in the loop reduces the over-shoot and ringing

devices and design engineers often must deal with the consequences of selecting through-hole devices as the main converter switches. To start with, the long lead of the package easily introduces an extra 10 nH inductance. This parasitic inductance, together with the parasitic capacitance of the device, causes over-shoot and ringing when the device is switched at a fast speed.

To demonstrate this, a SPICE-based simulation model result, together with the measurement of a TO-247 MOSFET switching is shown in Figure 8. As can be seen in Figure 9, the over-shoot and ringing are reduced by reducing the parasitic inductance.

The fact that a TO-247 device can be directly mounted with a heatsink could also cause EMC problems depending on the size of the heat sink, the connections, and other factors [11]. Each device that stands on the board acts like a little antenna. If the board heat sink is not bonded correctly, each device could also increase the radiation emissions.

The layout of the devices can also pose challenges. If the through-hole devices are located near the edge of the PCB (as they often are for better thermal performance), they tend to radiate a lot more than when they are located in the middle of the PCB.

If you think selecting through-hole devices would make your bill of materials cost look better, then think again. The total number of the main power stage switching devices per DC-DC converter is not big. If an SMD package cannot achieve the same level of thermal performance compared with a through-hole package, one could always use two devices in parallel to share the current. Doubling the number of devices also means doubling the cost. But the fact that

SMD packages have much better EMC performance could mean that one or two filter components can be omitted from the converter filter design.

For HV high-power converters, magnetic components such as common mode chokes (CMC) are bulky, heavy, and expensive. Adding one or two of these to the design will significantly increase the weight and the cost. To make matters worse, there is often no space to put a CMC due to the compact design of the converter. There's no worse situation than finding yourself in a late design stage where you need to put in heavy EMI filters.

Now, knowing this, would you still choose a TO-247 package?

Temperature, Deadtime Impact

We would like to mention the impact of temperature and deadtime because we were involved in a case where significant low-frequency noise (150 kHz-10 MHz) was observed in the conducted emissions originating from an HV-LV DC-DC converter. The DC link capacitor selection and design were good where expensive high-voltage, high-volume film capacitors were selected, and the DC link bus bar meant that minimum impedance between the DC link and the switches was achieved.

But the fact that the noise was at low frequency and in differential-mode suggested that the DC link was not good enough. It turned out that the deadtime of the converter was set too small. The switching devices, in this case, were IGBTs and tail current was not accounted for when setting up the deadtime [12]. A short deadtime can lead to shoot through of a converter. Shoot through will cause a very high, short-duration current to be drawn from the DC link. This is most likely to happen when one of the devices has a long tail current. The tricky thing here is that tail current time is also related to temperature. In this case, the emission problem only got worse after the converter had been running for a while, which made the troubleshooting process to identify the problem a challenging task.

CONCLUSION

In this article, we've discussed three important EMC design aspects in a DC-DC converter that design engineers need to get right to avoid multiple iterations in the later stage of a design. Early ground planning, the careful choice of switching devices, and a precise DC link analysis can help ensure that your DC-DC converter design meets the automotive EMC standards.

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EVALUATION OF EMC EMISSIONS AND GROUND TECHNIQUES ON 1- AND 2-LAYER PCBs WITH POWER CONVERTERS

Part 7: AC/DC Converter Design with EMC Considerations

By Bogdan Adamczyk, Scott Mee, and Nick Koeller

This is the seventh column in a series devoted to the design, test, and EMC emissions evaluation of 1- and 2-layer PCBs that contain AC/DC and/or DC/DC converters and employ different ground techniques [1-6].

Figure 1 shows the functional blocks of the PCB assembly [1].

This column is devoted to the design of the AC/DC Off-Line Flyback Converter. We present a schematic and PCB layout along with the EMC considerations and supporting design documentation.

1. AC/DC CONVERTER SCHEMATICS AND DESIGN REQUIREMENTS

Figure 2 shows the block-diagram AC/DC converter schematic.

The detailed schematic of the converter is shown in Figure 3.

The AC input filter consists of a common-mode choke (L3), line-to-ground Y-caps (C13, C1, and C14, C17 and C18), and line-to-line X-caps (C15 and C16).

The filtered signal is fed to the full-wave bridge rectifier, which produces a pulsating positive AC waveform. This waveform is smoothed by the LC filter consisting of L1, C2, C3, and R2 (R2 damps the antiresonant behavior of the filter). The output of the filter is a DC signal of the value $115 \times \sqrt{2} \approx 162$ V. This signal is fed to the primary winding of the flyback transformer. R1 and C1 on the primary side constitute a protective circuitry for the primary winding when the MOSFET switches off. R14 and D5 constitute a protective circuitry for the MOSFET. R17 and C27 constitute a snubber across the MOSFET.

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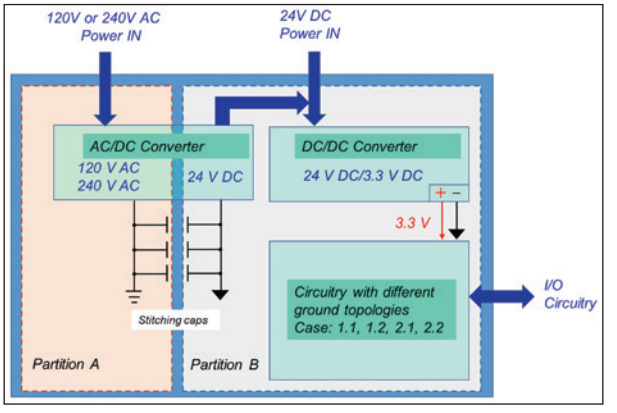

Figure 1: Top-level schematic – functional blocks

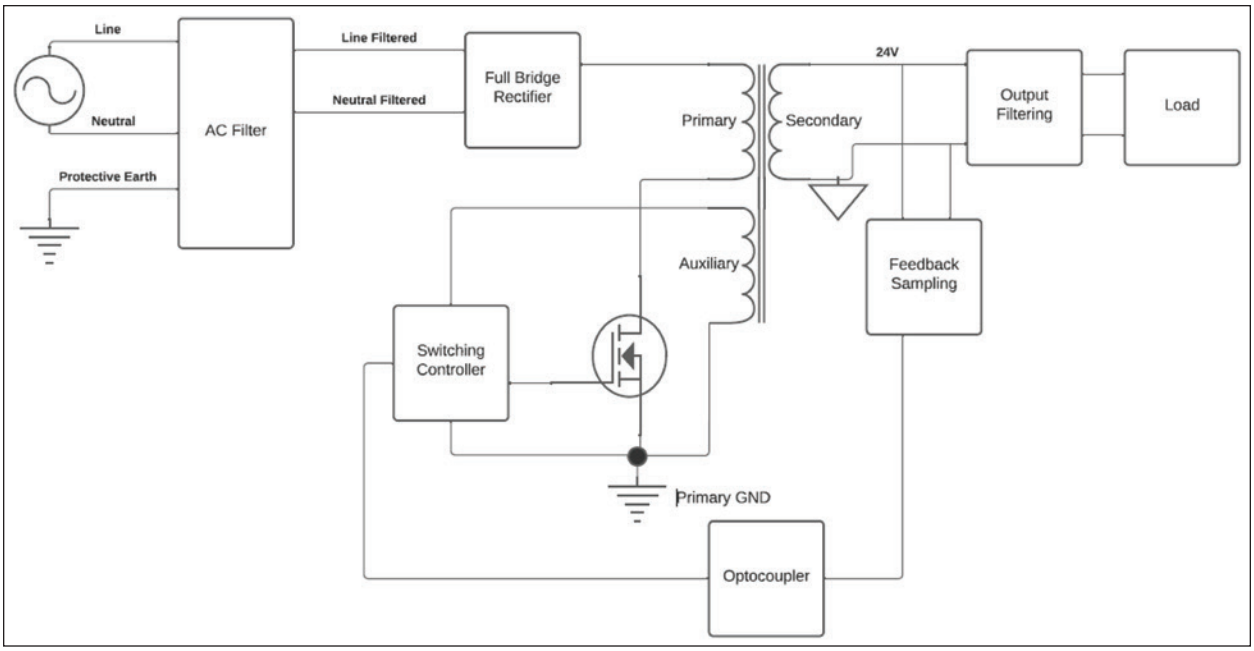

Figure 2: AC-DC converter block-diagram schematic

PWM Transistor Q1, controlled by U3 [7], opens and closes the connection to the transformer primary. This switching of the line voltage generates a current on the secondary side and on the auxiliary winding. The winding ratios of the transformer were chosen to generate 24V on the secondary side and 19V on the auxiliary winding. Auxiliary voltage powers U3. Inductor FB2 and C7 on the auxiliary side provide filtering.

Series combination of R3 and R5 constitutes a start-up resistor that charges a reservoir capacitor C7. VCC is internally regulated down from VIN. It is decoupled to ground with a capacitor C9. VIN is provided by the auxiliary winding of the transformer. Initially, both VIN and VCC are 0V. After the line voltage is applied, the current flowing through the start-up resistor charges capacitor C7. Subsequently, the internal regulator charges capacitor C9 (at this point the switching transistor is off and, thus, the auxiliary winding voltage is zero). Charging of C9

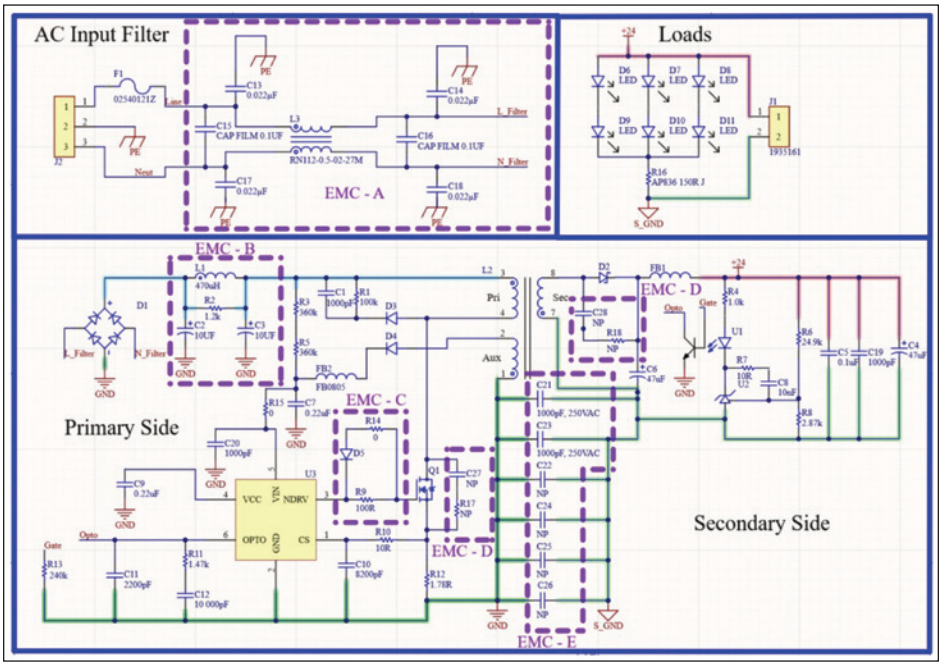

Figure 3: AC-DC converter detailed schematic

stops when VCC reaches approximately 9.5v, while the voltage across C7 continues rising until it reaches the wakeup level of 24V. Once VIN exceeds the Undervoltage Lockout (UVLO) wakeup level of 24V, NDVR begins switching MOSFET providing energy to the secondary and auxiliary windings. If the voltage on the auxiliary winding builds up to higher than 10V (UVLO lower threshold), then the start-up has been accomplished and sustained operation commences. To sustain the operation of the IC, VIN voltage must be in the range of 11–28V. In our design, we chose 19V. This voltage is provided by the auxiliary side of the transformer and is determined by the winding ratio between the primary and auxiliary sides. Decoupling capacitor C20 is connected to VIN.

The primary and secondary side grounds are connected through the Y-rated stitching capacitors C21 and C23.

The voltage on the secondary side is sampled for feedback to U3 through the optocoupler U1. The output voltage set point is determined by the shunt regulator U2 and resistor divider, R6 and R8. The output voltage is given by the following equation

$$V_{OUT} = V_{ref}\left(1 + \frac{R_6}{R_8}\right) \quad (1)$$

where V_{ref} = 1.24 V. R7 and C8 constitute a snubber across the regulator.

Output voltage filtering is provided by C5, C19, and C4. Lastly, there is a bank of 6 LEDs and a 150 Ω resistor to load the output, and there is a 2 pin screw terminal so any other load can be added. This amounts to 3 Watts of power dissipated in the load.

The top layer of the PCB used to create the AC/DC converter is shown in Figure 4, while the bottom layer is shown in Figure 5.

Figure 6 shows the AC/DC PCB converter populated with the components.

2. EMC CONSIDERATIONS

Similar to the DC-DC converter discussed in Part 2 of this series [2], provisions were added to this design

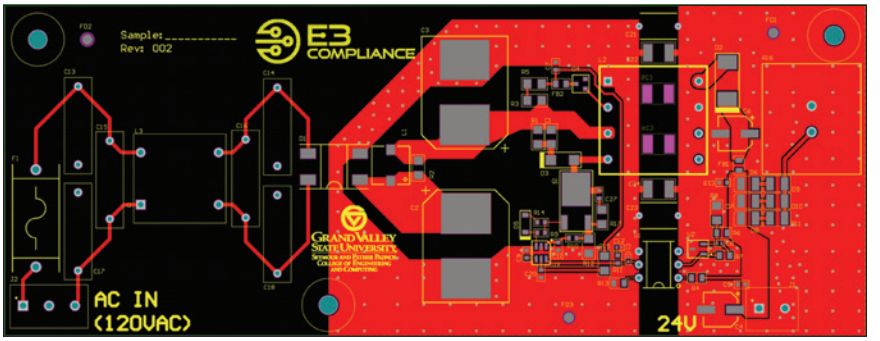

Figure 4: Top layer of the PCB

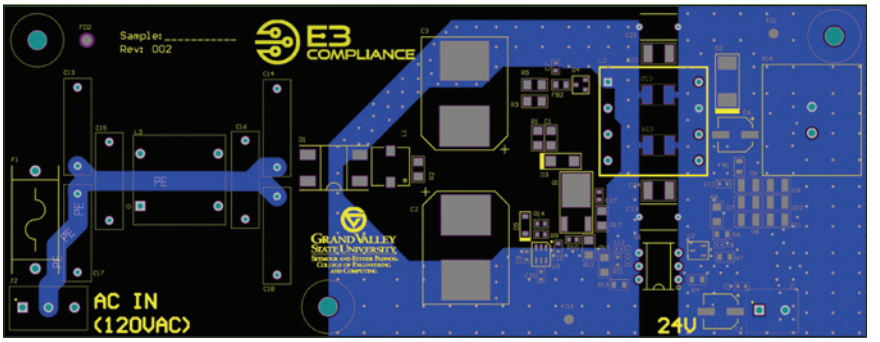

Figure 5: Bottom layer of the PCB

Figure 6: AC-DC converter PCB with components

that allow us to add/change components with the goal of improving the EMC performance of the design. These EMC considerations are shown in dashed boxes, labeled A through E in Figure 2.

These considerations are addressed below.

EMC-A: Provisions for an AC input filter were added to the input of this device. This filter consists of a common mode choke (L3), 0.1uF X-capacitors (C15 and C16), and 0.022uF Y-Capacitors (C13, C14, C17, and C18). The goal of this filter is to filter out the noise generated by the switching circuit and propagating out onto the power cord of the device.

EMC-B: A PI-filter was added right after the full bridge rectifier, this filter serves the purpose of smoothing out the rectified AC voltage, but this also provides some additional input filtering. This filter is comprised of a 470uF inductor (L1), a 1.2kΩ resistor (R2), and two 10uF capacitors (C2 and C3).

EMC-C: A pair of gate drive resistors (R9 and R14) and a diode (D5) were added in series with the connection between pin 3 of the switching controller (U3) and the N-Channel MOSFET (Q1). These components allow us to separately control the rise and fall times of this gate drive signal to allow us to slow down the rise and fall times of the signal, thus reducing the high-frequency content of the signal. The diode allows us to control the rise and fall times separately to ensure that the rise and fall times are equal.

EMC-D: Snubber circuits were added to both the N-Channel MOSFET (Q1) and the catch diode (D2). The snubber circuit on the N-Channel MOSFET, comprised of C27 and R17, is used to control the ringing from the MOSFET that results from the step response to the RLC network. The snubber circuit on the catch diode, comprised of C28 and R18, is added across the catch diode to reduce ringing across the diode junction.

EMC-E: Place holders for stitching capacitors (between primary and secondary ground) are added (C21 through C26). These allow us to evaluate the number, placement of capacitors as well as different types of capacitors.

For the next column, we will perform baseline radiated and conducted EMC emissions measurements with a minimal number of EMC components populated. Based on the measurement results, we will investigate EMC countermeasures needed to pass; this will be discussed in the subsequent column.

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USE OF HBM AND CDM LAYOUT SIMULATION TOOLS

By Dolphin Abessolo-Bidzo for EOS/ESD Association, Inc.

WHY IS THE USE OF THESE ESD LAYOUT SIMULATION TOOLS NECESSARY?

Electronic Design Automation (EDA) ESD verification tools have become instrumental to the design and verification flow of integrated circuits (ICs). This trend has been mostly driven by the extraordinary development and increasing complexity/technology scaling of ICs in the past few years. Furthermore, increasingly demanding product performance with necessary ESD reliability requirements makes it very challenging to achieve first-time-right silicon for both functional and ESD performance. In that context, the use of ESD verification tools to derisk IC designs before tape-out or for debugging purposes has become critical. In this article, the methodology of the state of the art of HBM and CDM layout simulations tools is described. Two real-life case studies are presented briefly, and the outlook towards future developments is discussed.

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METHODOLOGY OF THE ESD SIMULATION TOOLS

The simulations are typically performed at top-level IC design. Figure 1 describes a simplified simulation flow of the HBM and CDM layout check tools. The design input used is a post-LVS (layout versus schematic) database. In addition, the ESD device characteristics are required and integrated as piecewise linear (PWL) or SPICE models. Also, technology files containing process information related to devices layers and metallization stack, typically from the process development kit (PDK) are included in the simulation setup. Finally, the backend ESD current density rules, gate oxide,

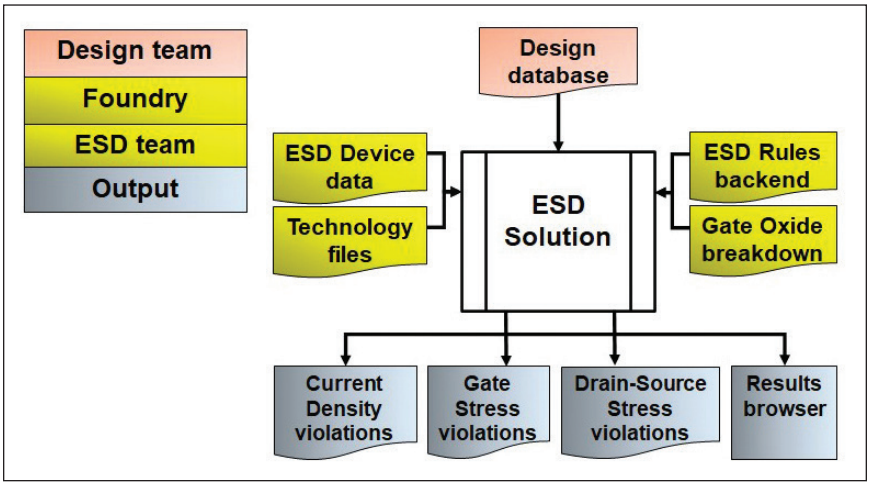


Figure 1: A simplified simulation flow of the HBM and CDM layout check tools.

Within the past 18 years, many studies exploring 3 µm to 7 nm technologies have demonstrated the excellent correlation of CC-TLP with CDM in terms of stress current failure threshold as well as electrical failure and physical damage signature.

and drain-source breakdown voltage stress are added as inputs to the ESD solver. Note that both ESD and victim devices characteristics are determined by means of transmission line pulse (TLP) and/or very fast (VF)-TLP characterizations. The main outputs from the ESD simulator are the ESD current density, gate stress limit violations, drain-source stress violations, and the overall ESD zaps results.

DESCRIPTION OF THE ESD LAYOUT CHECK TOOLS

The ESD layout check tools verify using HBM and CDM model source stimuli. The HBM check verifies that ESD design guidelines are fulfilled and met at full-chip level by performing pad-to-pad simulations. In addition, it highlights weak areas of the design, reports current density (CD) violations, and paths with high point-to-point (P2P) resistance. The CDM check is run to identify and localize overstressed gate oxide and drain-source of MOS devices due to CDM stress. Individual pin CDM stress discharge currents are simulated for all IC pins. A predictive CDM SPICE circuit simulation method based on the tester, package, and full IC modeling approach is presented in Figure 2 where the RLC network is extracted using the Time Domain Reflectometry (TDR) method [1]. This type of tool is especially useful in checking the V_{GS} voltages of internal core NMOS and PMOS receivers of intra- or cross-power ground domain and comparing the values to their gate oxide breakdown voltages.

ESD LAYOUT SIMULATION PREREQUISITES

The main required technology files for ESD layout simulation are the interconnect technology describing the backend layer stack and the layer setup or mapping file. The ESD devices or protection circuits are either SPICE simulated or described as PWL models extracted from TLP and/or VF TLP data. The ESD RC-clamps are directly simulated using the SPICE model. The other types of clamps and ESD devices are essentially PWL modeled. This includes

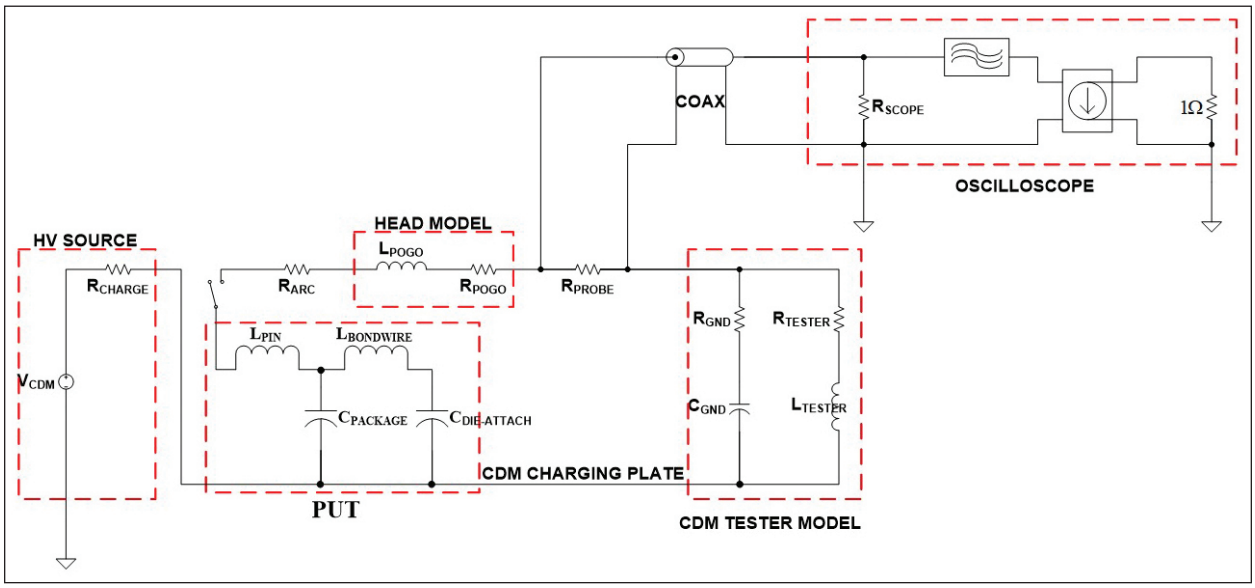
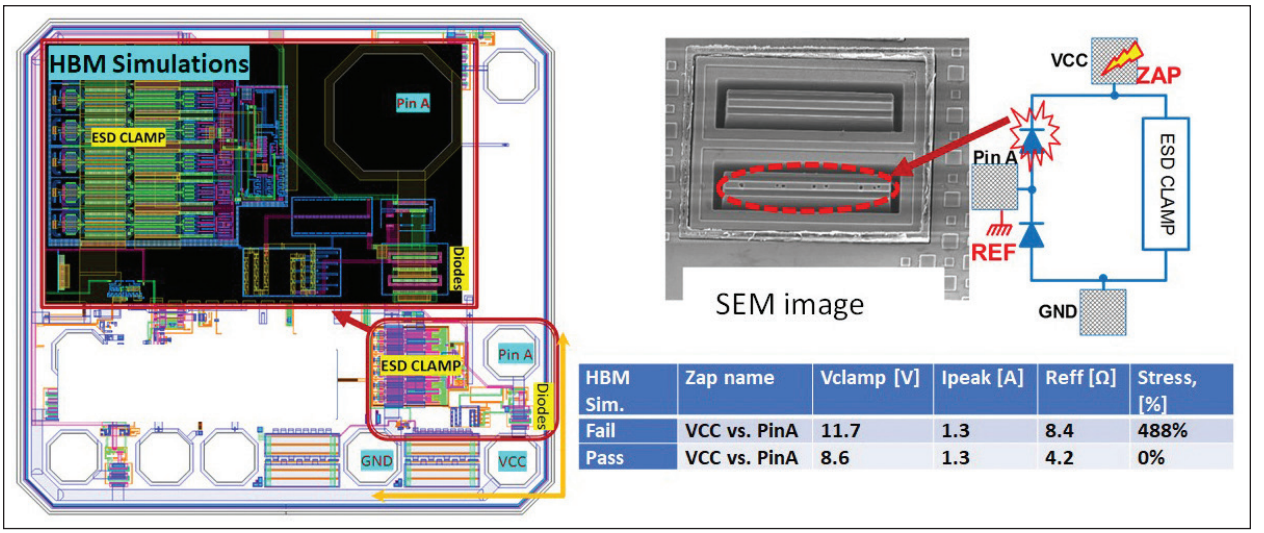


Figure 2: SPICE Model of the CDM Discharge Setup including the CDM Tester and PUT Parasitics [2].

but is not limited to ESD diodes, silicon controlled rectifiers (SCRs), grounded gate NMOS (ggNMOS), gate coupled PMOS (gcPMOS) transistors, and vertical latch-back NPN and PNP bipolar transistors. Further ESD characterizations are also required on the backend metal stack structures with the purpose of determining the ESD robustness of the metal interconnects and vias under ESD phenomena. Separate HBM and CDM time-domain current density rules are derived from those data.

EXAMPLES OF ESD SIMULATIONS

As an illustration, the use of ESD simulation check tools is demonstrated for two case studies, one on a complex RF product and the second on a mixed-signal integrated circuit. The ESD simulation tools were used in these cases to verify the implemented ESD fixes before tape out of IC design revisions, and the ESD qualification results of the new silicon in each case confirmed the passing of the ESD requirements for those devices.



HBM Sim.	Zap name	Vclamp [V]	Ipeak [A]	Reff [Ω]	Stress, [%]
Fail	VCC vs. PinA	11.7	1.3	8.4	488%
Pass	VCC vs. PinA	8.6	1.3	4.2	0%

Figure 3: HBM Simulations of an RF Product reproducing a 2kV HBM Failure Mechanism [3].

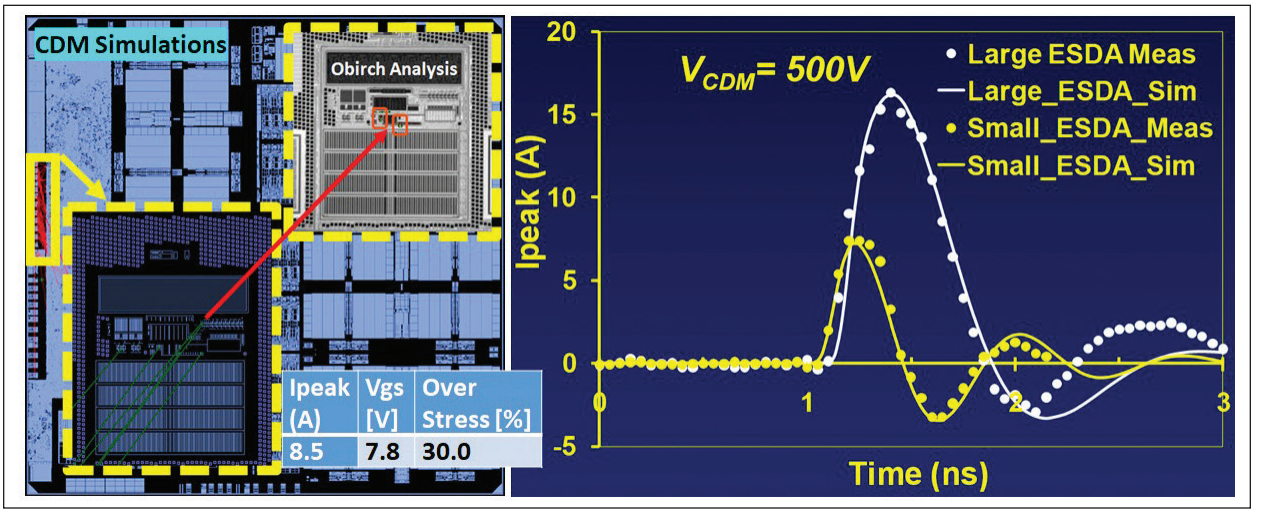


Figure 4: CDM Simulations of a mixed-signal product reproducing the 500V CDM failure mechanism [3]. Simulated and measured CDM waveforms from the JS-002 verification modules are also shown.

Figure 3 and Figure 4 show 2kV HBM simulations and 500V CDM simulations results of those ICs respectively. The simulation results fully correlate with the actual failure mechanism observed in both the RF (Figure 3) and the mixed-signal (Figure 4) ICs. Also, a very good correlation is found between the CDM simulation and measured CDM waveforms from the JS-002 verification modules. These modules correspond to the so-called ESDA small *coin* (with a capacitance of about 4.0pF) and large *coin* (with a capacitance of about 30.0pF). They both make use of the FR-4 material.

CONCLUSION AND OUTLOOK

This article has demonstrated the usage and benefits of HBM and CDM ESD layout simulations tools. The ESD layout simulation procedure typically consists of several steps. The benefits include the detection of risky ESD configurations and sites, the identification of ESD failure mechanisms, and the verification of the proper implementation of the overall ESD protection strategy of the IC design. The ESD layout check tools are typically silicon calibrated and integrated into the ESD design flow to catch ESD risks prior to tape-out. Further developments are expected in the mixed-mode ESD simulations combining TCAD and transient SPICE simulations to improve the predictability of the ESD robustness of integrated circuits.

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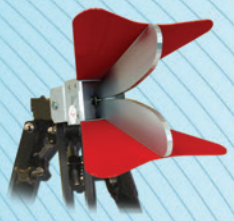

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