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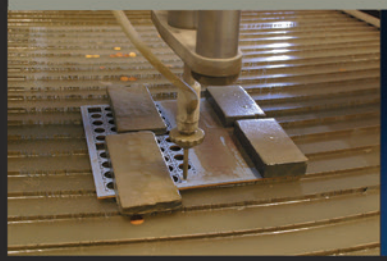

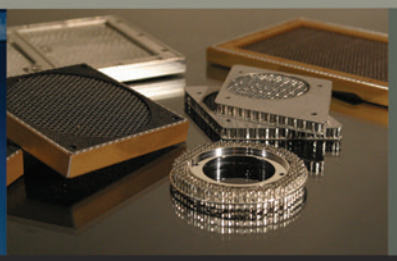

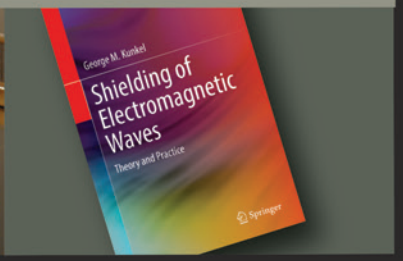

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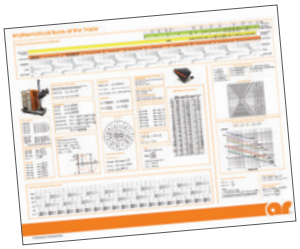

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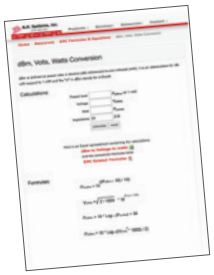

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CONTENTS

Amateur Radio Operator Fined for Interfering with Fire Suppression Communications

The U.S. Federal Communications Commission (FCC) has proposed a record fine against an amateur radio operator for interfering with radio communications supporting fire suppression efforts in a 2021 massive wildfire in an Idaho national forest.

According to a Notice of Apparent Liability (NAL) for Forfeiture, Jason M. Frawley of Lewiston, Idaho used his amateur hand-held radio to intentionally interfere with radio communications directing fire suppression aircraft that were combatting the "Johnson Fire," a 1000-acre wildfire near Elk River, Idaho. Frawley allegedly transmitted multiple times over two separate days on frequencies expressly allocated and authorized for government use, causing harmful interference with essential emergency communications.

The FCC has proposed a monetary forfeiture of $34,000, the maximum fine allowable in such cases. Frawley will be given an opportunity to respond to the FCC's NAL before a final Commission action is determined.

EU Commission Seeks to Expand Scope of REACH

The Commission of the European Union (EU) is reportedly seeking to expand the provisions of the EU's chemical restriction regulations to include the use of lead and lead compounds in polyvinyl chloride (PVC) polymers and copolymers.

According to a Notification filed with the World Trade Organization (WTO), the Commission has issued a Draft Commission Regulation that would amend a portion of Annex XVII of Regulation (EC) No 1907/2006, "Registration, Evaluation, Authorization and Restriction of Chemicals," also known as the REACH Regulation. The specific changes proposed in the Draft Regulation would prohibit the use of lead and lead compounds in PVC articles and prohibit the placing on the market of PVC articles containing a concentration of lead equal to or greater than 0.1% of the PVC.

According to the Notification filed with the WTO, the Commission estimates that the Draft Regulation will be adopted in late 2022, with an application of the restrictions deferred until late 2024.

FCC Steps Up Notices to Pirate Radio Broadcasters

The U.S. Federal Communications Commission (FCC) has recently issued notices to several individuals as part of its ongoing effort to restrict unlicensed radio operations and illegal, so-called pirate, radio broadcasts.

Officials of the FCC's Enforcement Bureau issued two separate notices to individuals linked to illegal pirate radio broadcasting, one for an unlicensed FM broadcast station operating from a location in Newark, NJ, and the other for an unlicensed broadcast traced to a location in Queens, NY.

In a separate case, the Enforcement Bureau issued a notice to a car service operator in Far Rockaway, NY for continuing to operate under the terms of a land mobile radio station license that had expired and was not renewed.

In the pirate radio cases, the recipients of the notices were reminded that they face financial penalties of up to $2 million for failing to cease their illegal broadcasts. The car service operator was instructed to immediately cease their unlicensed radio operation and to respond to the FCC's notice within 10 days with any evidence of their authority to continue operations.

Correction *In our July issue, our news item "EU Commission Updates Harmonized Standards for Certain Electrical Equipment," incorrectly refers to Directive 2014/35/EU as the Radio Equipment Directive (RED). Directive 2014/35/EU is the EU's Directive on electrical equipment designed for use within certain voltage limits, also known as the Low Voltage Directive (LVD). We apologize for the error.*

MIT Researchers Develop AI Chip That Can Reduce Electronic Waste

Researchers at the Massachusetts Institute of Technology (MIT) have developed a unique approach to configurable technology chipware that could help reduce electronic waste, partially adopting a model used in a universally popular children's toy.

According to an article posted on the website of Interesting Engineering, the researchers explored the idea that electronic chips could be connected without hardwiring but instead with stackable and reconfigurable connections similar to those used in LEGO-style building bricks. Their design experiments included alternating layers of sensing and processing elements, combined with light-emitting diodes (LEDs) that allow different chips to interact optically.

The use of LEDs to transmit data between chips in a given configuration would enable developers to swap out legacy chips and reinstall newer chip technology without the need to rewire the design. Ultimately, this approach could increase the useful life of many chip-based technologies and reduce the amount of waste generated from the disposal of outdated electronics.

Ukraine Revises Toy Safety Regulations to Align with the EU

The war in Ukraine goes on. But the process of governing in that country continues apace, as evidenced by a recent action to amend Ukraine's toy safety regulations.

According to a news item recently posted on the website of SGS, the Ukraine government issued Resolution No 557. The Resolution revises Annex 2 of that country's Technical Regulations on the Safety of Toys to better align its regulations with those detailed in the European Union's (EU's) Directive 2009/48/EC, which addresses toy safety.

Most notable among the changes detailed in the revision is the restriction on the use of aniline in toys that are intended for use by children under 36 months of age, and in other toys that are intended to be placed in the mouth. In addition, the revision incorporates the allergenic fragrance limits set forth in the Directives (EU) 2020/2088 and (EU) 2020/2089.

The changes to Ukraine's Technical Regulations on the Safety of Toys will enter into force on November 14, 2022.

NASA SPACE SHUTTLE'S RETURN TO FLIGHT:
THE UNTOLD ELECTROMAGNETIC BACKSTORY

How Applied Electromagnetics Guided the 22 Post-*Columbia* Shuttle Missions

Dr. Brian M. Kent is an independent aerospace consultant with 43 years' experience in electromagnetic analysis and radar signature measurement technology. During his 37-year career as a US Air Force Career Civilian, Kent co-served the Technical Staff of the Columbia Accident Investigation Board (CAIB) from 2003-2009, and later served as a technical radar consultant for the Space Shuttle Requirements Change Board (PRCB). He is a Life Fellow of the IEEE and is the recipient of the Presidential Rank Award from the Secretary of the Air Force in 2009. Kent can be reached at brian.kent.phd@gmail.com.

by Brian M. Kent

Editor's Note: *This article was originally published in the June 2019 issue of* In Compliance Magazine. *We are pleased to reprint Brian Kent's article in honor of his keynote presentation at this year's EMC + SIPI Conference, to be held in Spokane, Washington, August 1-5.*

DEDICATION

With deepest respect, this article is dedicated to the extended families and friends of the astronauts lost on Columbia's *final Shuttle mission.*

On February 1, 2003, NASA's Space Shuttle Orbiter *Columbia* broke apart upon re-entry into the earth's atmosphere, tragically ending the lives of seven highly-trained and experienced astronauts. This accident not only personally affected the extended families of the astronauts, it permanently changed the trajectory of the U.S. manned space program. After a lengthy accident investigation and root cause analysis, the Shuttle successfully flew again on July 26, 2005. The Shuttle's subsequent 22 missions made possible the completion of the assembly of the International Space Station (ISS) and provided a final service call for the Hubble Space Telescope, before the Shuttle fleet was retired in 2011.

While much has been written about the Shuttle program, this specific article will focus on a very little-known element of the Shuttle's return-to-flight (RTF) story. Beginning with the *Columbia* investigation and ending with the creation and deployment of the NASA Ascent Debris Radar (NDR) System, this article will cover the "Electromagnetics (EM) Backstory" that was instrumental in allowing the Shuttle to safely fly again.

THE COLUMBIA ACCIDENT INVESTIGATION AND THE FLIGHT DAY 2 OBJECT: A BRIEF RECAP

On February 1, 2003, the nation witnessed in real time the disintegration of the Shuttle Orbiter *Columbia* as it attempted to re-enter the atmosphere after its 15-day mission. Within hours, the formal *Columbia* Accident Investigation Board (CAIB) began its work. Over the next several months, the CAIB gathered evidence to determine root cause of the accident, which included recovering and analyzing fallen debris articles from every state overflown by *Columbia's* final de-orbit trajectory.

Summarizing the CAIB's final [1] report, we quickly home in on the root cause sequence. During *Columbia's* ascent on January 16, 2003, the left main tank bi-pod ramp insulation foam broke off the external tank about 81.9 seconds into the flight and struck *Columbia's* left wing (an image from a NASA launch camera is shown in Figure 1). Unbeknownst to NASA Mission Control or the astronauts on board,

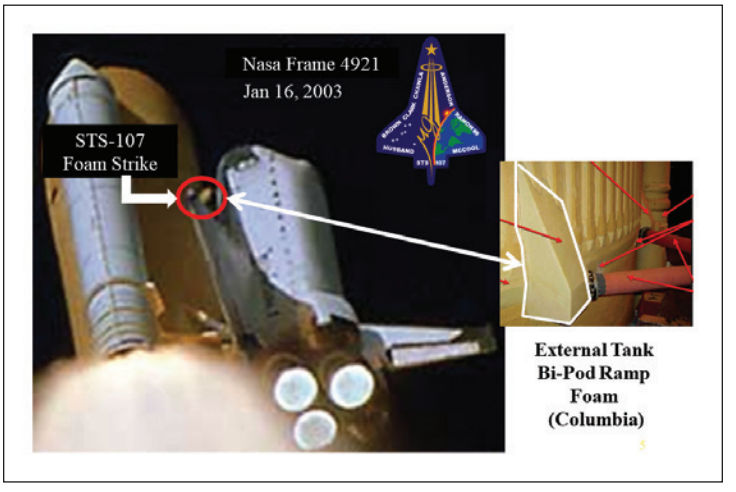

Figure 1: Bipod ramp foam striking *Columbia's* left wing during launch ascent on January 16, 2003

the strike damaged and left a hole in the reinforced carbon-carbon (RCC) leading edge around panel 8 of the left wing. The RCC is considered "hot structure" and the RCC protects the interior aluminum wing structure from the frictional heat of re-entry.

Note that Figure 1 is a highly enhanced image produced *after the accident*, and was *not available* during the actual mission. In addition, due to the positions of ground cameras and those available on orbit, there was not a clear line of sight to the damaged wing area. NASA material engineers estimating the physics of the kinetic impact suggested a possibility of RCC edge damage. Sadly, there was a lack of program-wide consensus that the wing RCC edge was compromised until the fatal re-entry day.

Through an exhaustive process, the CAIB was able to determine the RCC edge failure as the root cause through three independent investigative paths. First, Columbia's equivalent of a flight data recorder was recovered in the fallen debris. An analysis of the combined 600 plus temperature, pressure, and vibration sensors verified that the 2000° F re-entry plume entered the left wing at panel 8 and slowly melted the interior structure of the left wing. The wing eventually collapsed and the vehicle disintegrated. Second, the CAIB conducted a series of "air cannon impact tests" in June and July of 2003, wherein pieces of insulation foam were repeatedly fired at various angles and velocities to prove that the foam likely punched a hole in the RCC edge from the Figure 1 wing strike. [2,3]

The third and most circuitous path was the EM investigation into the mysterious so-called "flight day two" (FD2) object. During its second day in orbit, when the *Columbia* was flying in an upside down and backward direction relative to its orbital velocity vector, *Columbia* performed a slight yaw maneuver to calibrate an on-board navigation sensor, then re-maneuvered to return to its base orbit. Right after this maneuver, low frequency USAF space monitoring radars automatically detected the departure of a small debris piece from *Columbia*, as shown in the tracking radar data in Figure 2.

This object was tracked for three days, after which it disintegrated in the atmosphere due to aerodynamic drag. The object was reacquired on multiple days, and the radar data automatically recorded by the source radars. Unfortunately, this data was not known to NASA nor the Air Force until weeks after the accident. In fact, such data was not "knowable" in real time due to the automated nature of the space radar recorders.

As a radar signature expert, I must explain that every radar target has a property called "radar cross section" (RCS) that is a measure of how an object scatters radar energy in all directions. Generally RCS is denoted by the symbol σ, with SI units of m^2 or dB_{sm}. RCS generally varies with the frequency of the radar and 32the orientation of the target with respect to the radar. Since the FD2 object tumbled in space, ground radar sensors saw a varying RCS versus time.

After the CAIB investigation began, U.S. Air Force Space Command (AFSPC) analysts determined the aeronautical ballistic coefficient (B_n) from the shape of the ballistic re-entry profile in Figure 2. This meant

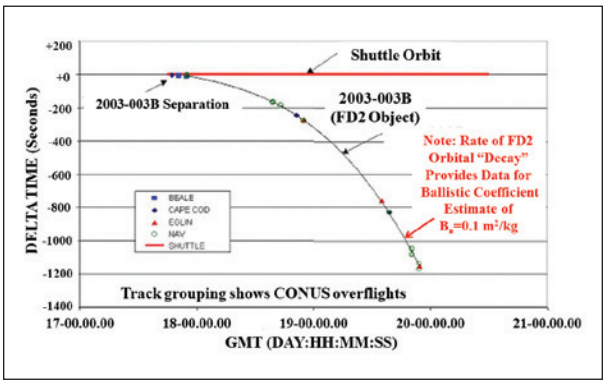

Figure 2: FD2 Radar track separating from *Columbia's* orbital path versus time [4]

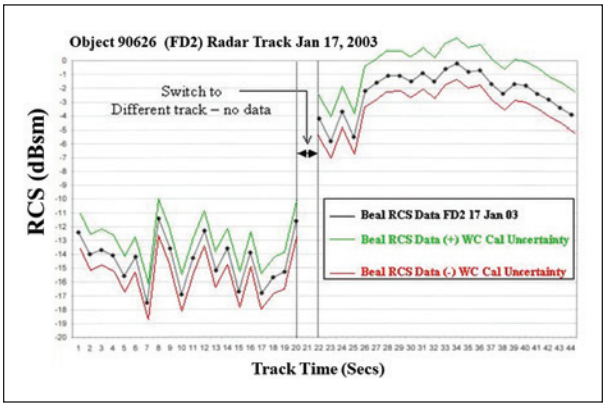

Figure 3: Maximum on-orbit measured RCS of FD2 object on 17 Jan 2003 tracked by Beal UHF Radar [3]

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NASA now had two pieces of technical information about the FD2 object: 1) the RCS at 433 MHz of the object varied between -1 and -20 dB_{sm} +/- 1.33 dB; and 2) its average ballistic coefficient, B_n = 0.1 m^2/kilogram +/- 15%. What we *didn't know* was FD2's *absolute* size as we did not have access to the actual FD2 object itself.

Nonetheless, Air Force Research Laboratory (AFRL) was contacted and I was assigned to investigate whether it was possible to narrow down the potential material candidate of the FD2 object to determine if the FD2 object was relevant to the CAIB investigation.

By February 12th, 2003, I was paired up with Steve Rickman of NASA-JSC, then Chief of the Thermal Design Branch. Rickman's organization was home to subject matter expertise and had responsibility for the Space Shuttle Orbiter Thermal Protection Subsystem (TPS), and the RCC Leading Edge Structural Subsystem (LESS). His team also was familiar with the Thermal Control System (TCS) materials present on the inside of the payload bay.

Rickman's team worked with our AFRL team to analyze 24 different potential Shuttle material candidates and provided AFRL with representative samples of all 24 materials. AFRL conducted subsequent RCS measurements in a laboratory called the Advanced Compact Range (ACR) which precisely measured the RCS of these material targets at 433 MHz (see Figure 4). The AFRL team quickly built up a database of possible material RCS characteristics, while NASA independently calculated the area to mass or B_n ratio values for these same materials. Our hope was to reduce the possible number of potential Shuttle material candidates.

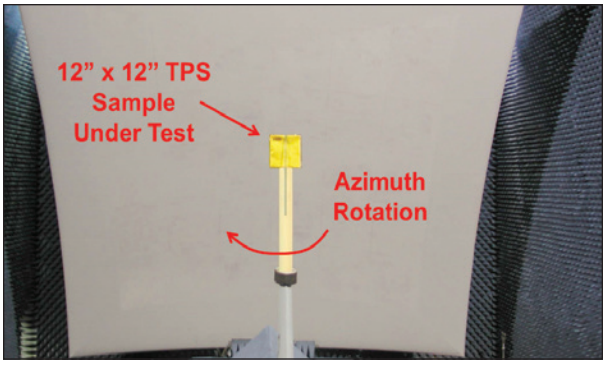

Figure 4: AFRL ACR facility for measuring RCS with 12" x 12" TPS sample shown mounted [3]

To our team's collective astonishment, the *initial* RCS and B_n data analysis definitively eliminated 21 of the original 24 materials, leaving only *3* remaining Shuttle materials candidates.

During this on-going FD2 RCS analysis, NASA mission specialists mentioned that, in previous Shuttle flights, maintenance tools inadvertently left in the payload bay had floated away. To include the possibility that a lost maintenance tool could have floated out of the payload bay, the CAIB audited the tool record logs for *Columbia's* three previous pre-flight maintenance cycles. The CAIB found that only three tools (a screwdriver, a snap crimping tool, and a specialized fastener tool) were unaccounted for. This didn't mean the tools were necessarily on-board *Columbia*, but only that they were not accounted for in the ground maintenance logs. Nevertheless, AFRL obtained copies of these three tools, and performed RCS tests that definitively eliminated these tools from consideration as the FD2 object.

After compiling our test results, the AFRL-NASA FD2 team briefed the CAIB in private testimony on April 13, 2003, then publicly on May 6, 2003. This was weeks before the definitive July 7, 2003 Southwest Research Air Cannon test. [3] The remaining three material candidates included: 1) a fractured "acreage" piece (Figure 5) of the RCC edge segment of at least 90-140 in^2 originating from RCC panels 8, 9, or 10, panels which are thicker than the other 19 RCC edge sections and whose acreage pieces would be too light to meet the B_n test criteria; 2) an "RCC "tee seal" that fills the joints between wing edge segments had some initial test ambiguities and wasn't immediately

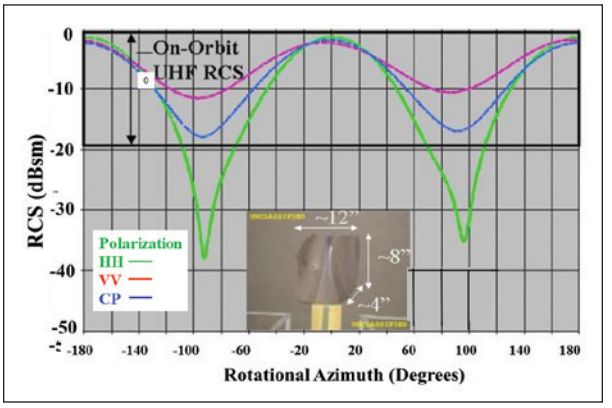

Figure 5: RCS of ~96 in^2 fractured panel 8 RCC edge acreage piece at 433 MHz vs Azimuth [3]

eliminated; and 3) a large piece of Incoflex "ear muff" spanner beam insulator composed of a cerachrome alloy that was present between the RCC edge and the aluminum spar of the leading edge.

Within weeks of the May 6, 2003 CAIB briefing, AFRL executed a complex computational electromagnetics (CEM) RCS analysis of all 26 Orbiter tee seal geometries (in whole or in fragments) and definitively showed through this analysis that the tee seal *could not be the FD2 object* (see Figure 6). Finally, subsequent forensic analysis of fractured left wing edge debris pieces recovered from the multi-state debris field showed significant cerachrome alloy melted onto surrounding recovered edge fragments, so therefore the

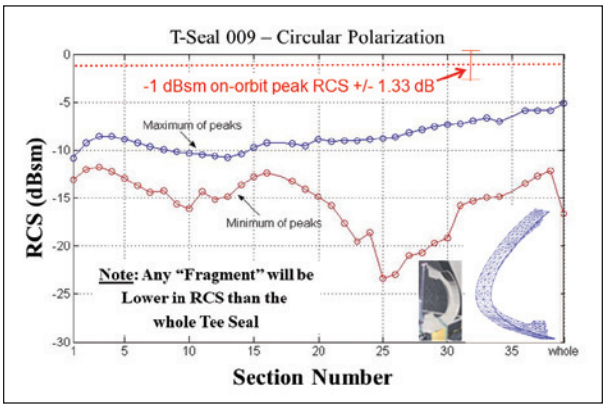

Figure 6: CEM analysis *eliminates* RCC tee seal as FD2 object as RCS *is too low* [5]

spanner-beam insulator was present during re-entry. This meant the *only material* that could meet all the criteria of the FD2 object was *a fractured piece of RCC edge originating from panel 8, 9, or 10 on the left wing of at least 90 in²* in area. *None* of the other 23 materials fit the combined exclusionary criteria of having the correct RCS, B_n, and also be forensically supported by other evidence. Hence, through careful EM analysis and high-quality RCS testing, AFRL provided critical EM data supporting the *Columbia* accident root cause, both of which were cited in the CAIB main report and technical Annexes. [1]

SHUTTLE RETURN-TO-FLIGHT – THE "WAR" ON ASCENT DEBRIS

Within a week of the CAIB report's publication, I was re-engaged through a phone call from NASA-JSC's Anthony D. Griffith. A long-time NASA space operations specialist, Griffith had been assigned the problem of detecting any undesired liberated debris from the Shuttle stack during the critical ascent stage. Griffith was a member of a much larger engineering team chartered by John Muratore, then Shuttle Chief Engineer, who had declared a "war" on future unintentional Shuttle ascent debris releases.

Muratore had three areas of emphasis; 1) study all previous historical Shuttle launches prior to *Columbia* to assess any and all previous debris releases and their potential sources, 2) re-examine the Shuttle stack

design elements (Orbiter plus 2 booster rockets plus the entire external tank) from first principles with an emphasis to change designs that reduced debris events; and 3) put together a safety net of optical and radar sensors that closely monitored the Shuttle during the launch and ascent phases to definitively detect/capture debris releases. This information would promptly be provided to the Mission Control flight director on *any* perceived safety hazards due to liberated debris striking the Shuttle stack.

I assisted with the historical study of radar debris tracks and also provided technical assistance on the new debris radar sensors. By September of 2003, Griffith and I recruited a diverse team of EMI/EMC, radar and weather experts from NASA-JSC, the U.S. Navy (USN), MIT Lincoln Laboratory, Mission Research Corporation, and the Air Force. The radar team had two primary duties. We first worked to support Muratore's thrust of pouring over archived tracking radar from previous Shuttle flights prior to *Columbia*. In the process, we discovered both optical and radar records of debris separation events especially near, during, or shortly after solid rocket booster separation. Figure 7 shows legacy radar debris data from a low-resolution tracking radar at NASA-KSC. Since the radar resolution was ~+/-150 meters, this tracking radar didn't give insight into the debris environment, especially debris considered "normal."

However, the tracking radars consistently demonstrate that, during the solid rocket booster (SRB) separation period, the entire RCS of the Shuttle increased dramatically. The radar team was asked to figure out the physics of this RCS bloom phenomena. After

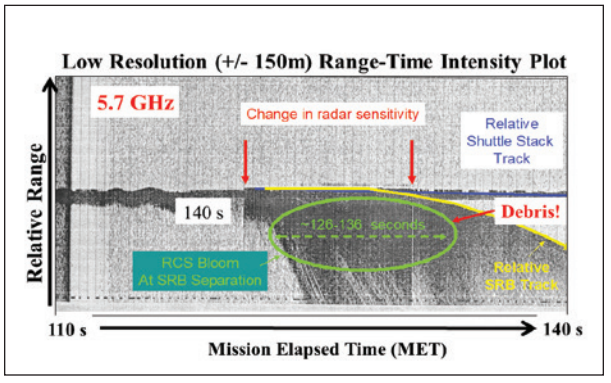

Figure 7: Low resolution USAF tracking radar ascent debris as recorded during a pre-Columbia mission

studying the propulsive design, we speculated that the burned $AlCl_3O_{12}$ (aluminum perchlorate) solid rocket propellant present in the main boosters *and* the 16 small, quick-firing booster separation motors (BSM) were the cause. The 16 BSM boosters (four at both the top and the bottom of each booster), each kicked out 20,000 pounds of thrust for 0.8 seconds, which pushed the expended main boosters away from the Shuttle stack after the booster net propulsive force turned to net drag. The burned propellant residual was Al_2O_3, a highly reflective smoke residual, as shown in Figure 8. In addition, the Shuttle's two main booster rocket engines generated literally tons of both gaseous and liquid Al_2O_3 "slag" which left a wake in the airstream behind the whole Shuttle stack. But how could we prove this theory?

Working with the USN, NASA and AFRL devised a plume RCS test by firing a series of six individual BSM motors on a captive engine stand at China Lake while measuring the plume and debris signatures. Figure 9 shows the test set-up and Figure 10 shows

Figure 8: Shuttle ascent surrounded by Al_2O_3 smoke during BSM firing preceding booster separation

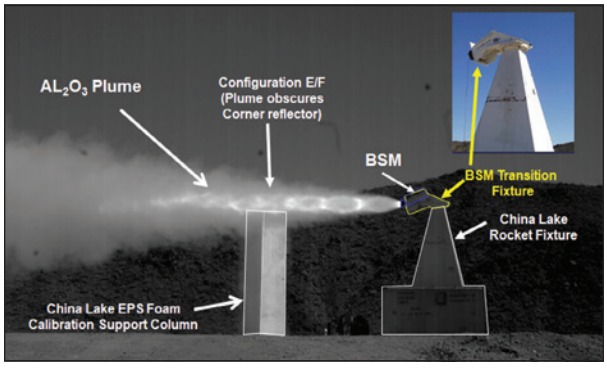

Figure 9: China Lake BSM plume RCS test 2004 [6]

a sample of dynamic plume data. Indeed, the smoke cloud filled with particulate Al_2O_3 acted like a giant radar chaff cloud for a few seconds. It also explained why it was going to be nearly impossible to transmit any radar energy directly up to and through the rear end of the Shuttle Al_2O_3 plume during ascent to "detect" unwanted ascent debris events within the Shuttle stack.

Any potential NASA debris radar (NDR) sensor had to be sited to get a lateral side view of the ascending Shuttle, which ultimately eliminated all possible radar sites southwest of the Shuttle launch pads 39A and 39B, where all current USAF tracking radars were located. The NDR team needed a site to the northwest of the cape, potentially on the grounds of a U.S. Park Service National Wildlife Refuge. How was *that* going to happen?

SELECTING AND SITING THE NASA DEBRIS RADAR (NDR) SYSTEM

After obtaining the critical plume RCS data, the NDR team briefed NASA on April 4th, 2004. The team recommended that NASA acquire and employ a combination of a DoD C-band (5.45-5.95 GHz) high resolution imaging radar combined with upgraded commercial versions of an X-band (10 GHz) high resolution Doppler radar. Although NASA concurrently planned significant visual camera enhancements, radar sensors were absolutely necessary because the remaining Shuttle launch manifest included several night launches where the cameras would have highly degraded performance.

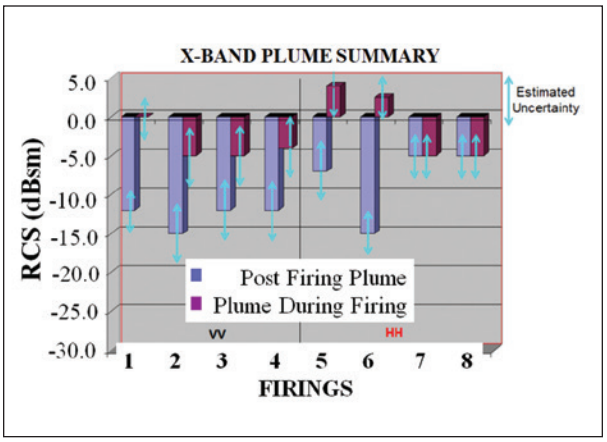

Figure 10: RCS peak for 1 BSM plume (5.4 GHz) [6]

The technology recommended by the radar team was already deployed on USN ship platforms for monitoring western pacific test launches of mobile ICBMs. Furthermore, the USN had recently decided to relocate a $50 million C-band radar from Puerto Rico and were looking for a replacement site in Bermuda or Florida. The USN also supplied technical contacts in Denmark for a Weibel high resolution Doppler radar that worked in the velocity range needed during Shuttle ascent.

The USN's Charlie McSorley, Mike Hardman, and Marty Stuble jointly spearheaded efforts between the Navy and NASA to get the C-band radar moved. Ultimately, NASA executed a joint agreement with the USN to relocate the C-band radar near Kennedy Space Center. Recall that our plume RCS results required us to site the USN C-band radar for a lateral launch view. Since all big projects need at least some luck, the NDR team finally got a break. We found a small fenced-off 0.5-acre plot on Merritt Island sited to the NNW of Pad 39A. This plot formerly sited a thunderstorm research radar for the National Center for Atmospheric Research (NCAR). The NCAR radar was long gone, but the perimeter fenced land still belonged to NCAR even though it was now on a National Wildlife Reserve. NASA and NCAR quietly and efficiently transferred the property to NASA on permanent loan, and NDR had its radar site!

The photo sequence in Figure 11 shows the original 2004 NCAR site and its transformation to its present form. Figure 12 shows the combined "field of view" of the ascending Shuttle as seen from the fixed C-band NCAR site plus the two, ship-deployed X-band Doppler radar sites. Figure 13 shows the two Dutch-made Weibel Doppler radars deployed downrange on the NASA SRB recovery vessel *Liberty Star* and on a U.S. Marine Runnymede class LCU.

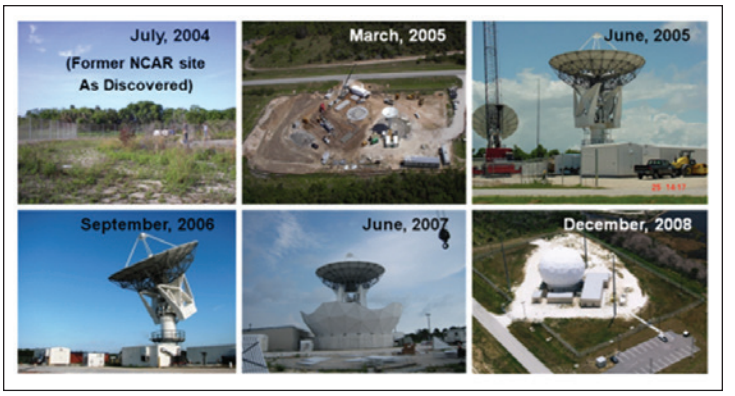

Figure 11: NDR site July 2004-December 2008

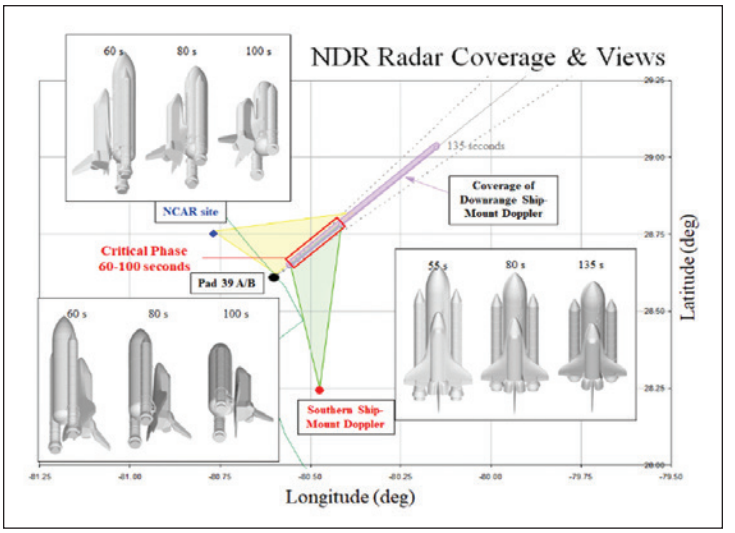

Figure 12: Combined NDR radar coverage from NCAR radar site plus 2 ships with Doppler sensors

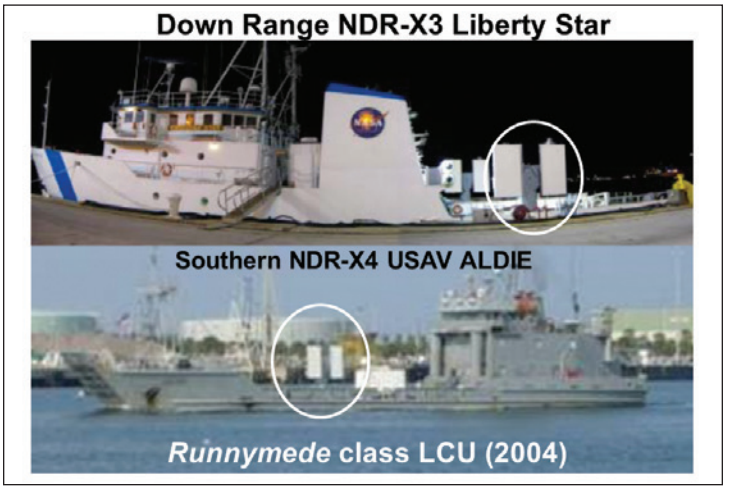

Figure 13: Sea-based NDR Weibel Doppler radars

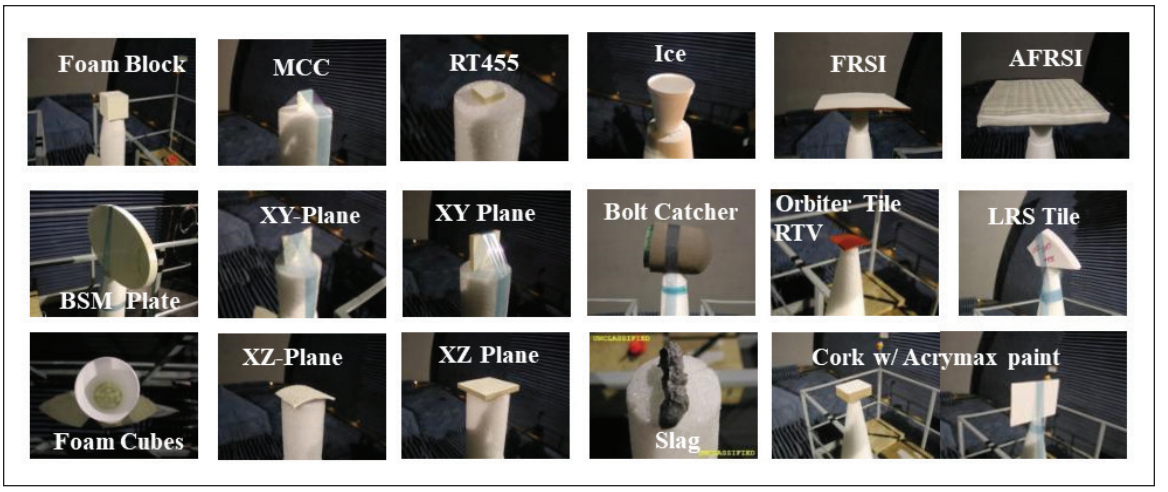

Figure 14: Debris samples under ACR RCS testing

CHARACTERIZING TYPICAL ASCENT DEBRIS RCS AND BALLISTIC PROPERTIES

With the type and locations of the NDR radars fixed, AFRL, NASA and the USN now collaborated to create a massive theoretical and empirical database of typical Shuttle debris pieces based again on RCS and B_n coefficients. NASA's debris team had identified hundreds of legacy debris sources from previous Shuttle flights. These debris materials could have originated anywhere on the Shuttle stack or from the Shuttle solid rocket propulsion subsystems. A lengthy list of items was created, and NASA decided to return to AFRL's compact range to conduct RCS measurements at C and X band for every debris candidate.

Meanwhile, NASA-JSC created a database of matching ballistic coefficient, B_n, for each candidate. This involved hundreds of RCS measurements of everything from various pieces of tank foam, cork insulation, space-qualified RTV sealant and so forth. Each sample was measured from 2-18 GHz, 360° in azimuth, and for three X-Y-Z orientations. The observable signatures were medianized over observable tumbling angles (like liberated debris in free stream air) and their corresponding B_n numbers included. Figure 14 shows a small sample of materials whose RCS was characterized in the ACR.

After compiling data on hundreds of sample combinations, yet another "realism" test was executed. The US Navy loaded up about one-third of the heavier samples, and ejected them from a C-130 Hercules at 10,000-foot altitude. The debris pieces were tracked and RCS characterized with Doppler instrumentation radars out of Patuxent River, MD. Figure 15 shows 4 samples whose dynamic tumbling signatures were measured. This also help correlate the B_n analysis for each sample.

At the conclusion of these RCS tests, we had a very good feel for the combined RCS and B_n for nearly every Shuttle material. What we didn't know was

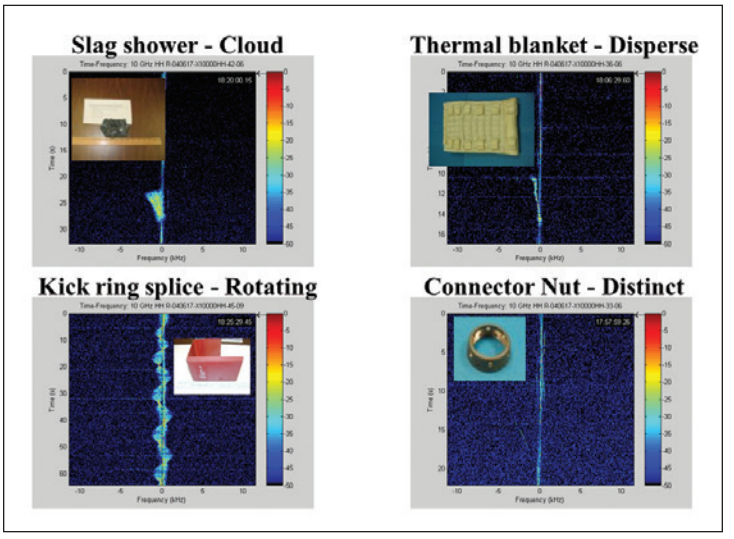

Figure 15: USN C-130 dynamic debris data samples

whether the NDR system radars, which operated at fairly high powers, would interfere with the operational Shuttle systems during launch and ascent. It was a safety concern that NASA demanded be addressed before return to flight.

THE *DISCOVERY* EMI/EMC SAFETY OF FLIGHT TEST

Historically, basic NASA range tracking radars operated on every Shuttle launch. Conventional USAF range safety radars have been in existence for over 35 years and typically operate in C-band at two specific frequencies, 5.69 GHz and 5.8 GHz. NASA needed to better understand the behavior of the radar signatures from debris shedding off the Shuttle during the ascent phase in order to monitor potentially dangerous debris shedding events.

After the acquisition of the NDR system was approved, Shuttle EMI engineers realized these three new monitoring radars would emit frequencies to which the Shuttle had not been exposed during previous launch and ascent operations. The new "debris" radars were to operate in two specific frequency bands, with the C-band radar emitting an FM sweep continuously from 5.45 GHz to 5.95 GHz, and the new X-band "Weibel" Doppler radars tunable to any fixed frequency between 10.0 GHz to 10.55 GHz. Clearly, it became imperative to verify that the new C-band and X-band debris radars would not interfere with any existing Shuttle system during the ascent phase. Since the aft bay of the Shuttle houses the critical Space Shuttle Main Engine (SSME) controllers, NASA was particularly concerned about RF exposure of sensitive equipment inside the aft bay to exterior radar RF levels from outside the aft bay. Fundamental knowledge of the RF shielding characteristics was required before *Discovery* could be certified for safe flight.

The purpose of the EMI test was to provide NASA an accurate estimate of the RF attenuation at specific radar frequencies of the Orbiter Aft engine bay, including an estimate of measurement uncertainty. The measurements had to be performed while the Shuttle was contained in a hangar-like facility called the orbiter processing facility (OPF). The relative geometry of the Shuttle and the OPF high-bay (HB) 3-door area along with the test receiver is shown in Figure 16. (Note the Shuttle *Discovery* was located *inside* OPF 3, and the hanger doors were opened so that the RF attenuation measurements could be made *outside*.)

During the test, the target was static with all normal work stands in place. The translator platforms behind

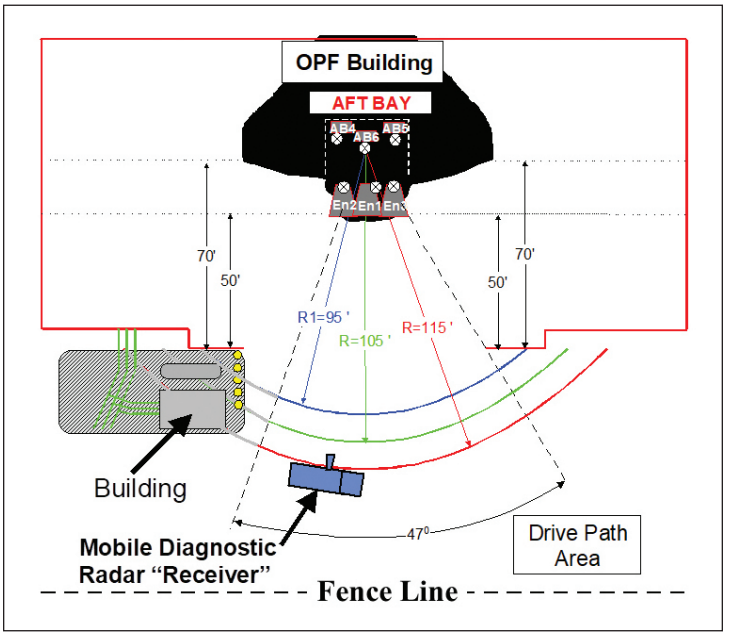

Figure 16: Orbiter *Discovery* RF attenuation measurement diagram.

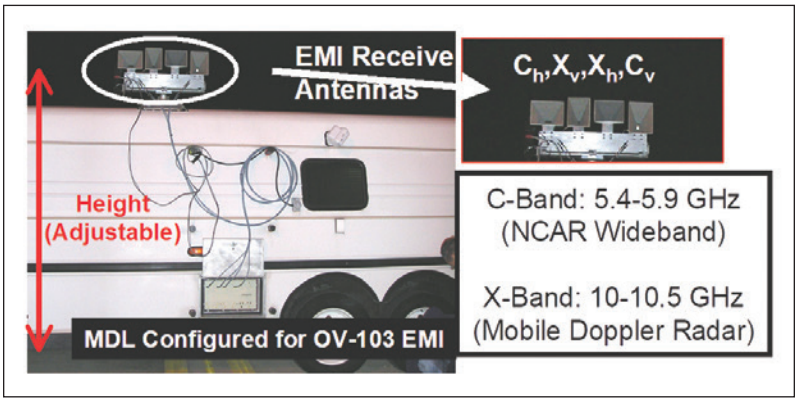

Figure 17: Side of MDL showing receive EMI antennas with a pneumatic mast height adjustment

the aft section of the Shuttle were moved completely to the side to avoid line-of-site blockage between the aft bay and the receiver. In order to achieve the test objectives, the Orbiter was placed in as near-flight condition as possible to simulate ascent attenuation characteristics. Three semicircular drive paths represent a constant mean range between the Orbiter aft bay centroid and the receive antennas during the RF attenuation tests. Attenuation data was obtained for three separate ranges (95, 105, 115 ft) and multiple receive antenna heights (10, 15, 20 and 25 ft). The Cross-X's in Figure 16 represent six Vivaldi broadband antennas inserted inside the aft bay, three by the rear avionics bay wall and one next to each of the Shuttle's main engine computers.

The orbiter *Discovery* was in preparation to launch around mid-July 2005. To assure this RF attenuation measurement data was flight representative, AFRL needed the Orbiter in the closest possible state to flight. It was essential that the AFRL MDL EMI/EMC test did not impact *Discovery's* flight schedule. For this reason, we came up with a reasonable test configuration that minimally impacted the Orbiter schedule. Since EM reciprocity allows one to interchange source and receive antennas in a one-way RF measurement, we decided to place the RF radiators *inside* the Aft engine bay, then measure the RF leakage with a passive receiver positioned *outside* the vehicle. Since the aft engine bay is physically large, the test team decided to place six, dual-polarized radiating antenna elements inside the aft bay, all connected together with a commercial off-the-shelf (COTS) RF feed network.

To receive the energy, AFRL positioned their mobile diagnostic laboratory (MDL) [7,8] in a receive-only mode as indicated earlier. To help reduce unintentional local electromagnetic interference (EMI) during the RF attenuation measurements, we used the existing MDL radar as the exciter, running a long, fixed cable between the transmitter and the aft bay emitters. During a typical RF attenuation measurement, the MDL was driven along a fixed radius circle relative to a point in the center of the aft bay. The receiver was triggered at regular intervals along the radius, and measurements were performed for all radar bands and polarizations, three ranges and four antenna heights. C-band data was acquired from 5.45-5.95 GHz, while X-band Data was acquired from 10.0-10.5 GHz. Figure 17 shows the MDL receive antennas on the side of the MDL.

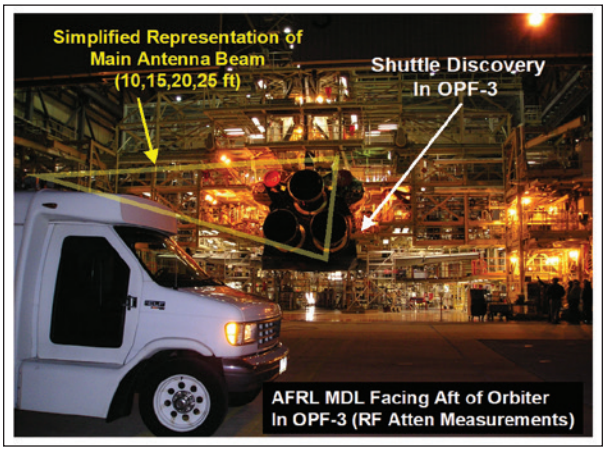

Figure 18: MDL at *Discovery's* EMI test Jan 17 2005

The MDL drove along the three drive paths for each antenna height. Figure 19 shows the network used, while Figure 20 shows one of the six interior dual-polarized exciters used. AFRL performed pre-test and post-test network analyzer measurements with MDL pointed at the *Discovery* during one of its drive paths. AFRL performed pre-test and post-test network analyzer measurements to assure the RF network didn't change during the test. We also characterized every one of the six distinct RF pathways through the network.

The entire data acquisition was completed in 4.5 hours, and the overall aft bay modification/de-modification for this test was completed in one 16-hour shift. NASA's Robert Scully co-analyzed the EMI/EMC test data and ultimately certified the results to the Shuttle PRCB, which adopted his recommendations.

In the end, the aft bay EMI attenuation experiment was successful, and the corresponding C-band attenuation data is shown in Figure 21. This attenuation data was combined with a NASA susceptibility analysis. NASA determined that neither the NDR C-band or X-band radar waveforms would create any EMI/EMC disruption of critical Shuttle systems during ascent.

EM SIMULATION BEFORE *DISCOVERY* RETURN-TO-FLIGHT

With the overall NDR system under construction and sited, it was clear the large 50 ft diameter C-band mid-course radar (MCR) would not be ready by *Discovery's* first flight in July 2005. Fortunately, the USN had a similar ship-based radar system called the Navy missile imaging system (NMIS) which operated over the same frequency band but at slightly lower radiated power. The USN had the NMIS system temporarily installed at the NCAR site side-by-side with the larger MCR under construction, providing an operational NDR system from the very first return to flight mission.

However, in order to train the radar operators, NASA needed a true C-band radar simulation of the Shuttle fly-out. This meant calculating the scattered field and RCS of the entire Shuttle stack, properly oriented in space and time relative to the NCAR site. The model had to include the period before SRB staging, SRB staging, and after SRB staging.

AFRL was again called to help, and through the technical leadership of Drs. Kueichien Hill and Tri Van, a viable solution was found. First, Hill and Van created an extremely detailed geometric grid of

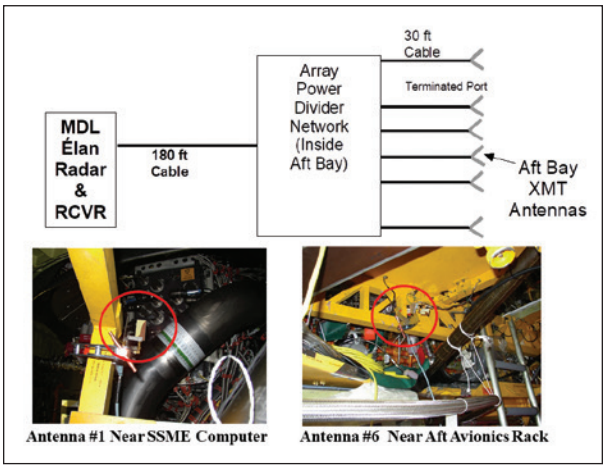

Figure 19: RF network used in *Discovery* EMI test

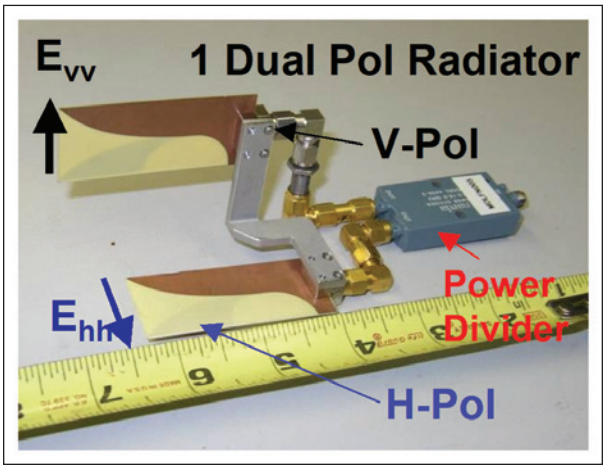

Figure 20: EMI dual-polarization exciter antennas

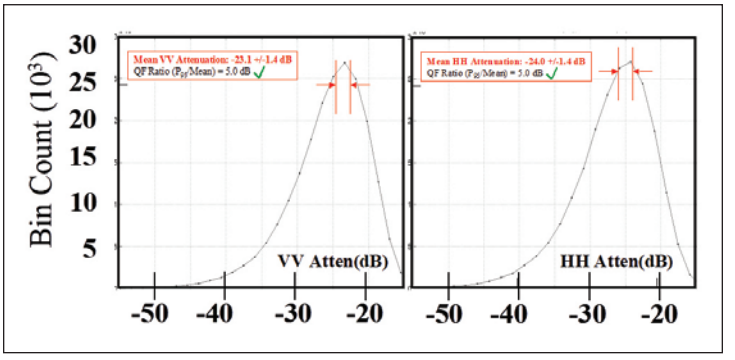

Figure 21: C-band VV/HH aft bay attenuation

the entire Shuttle stack. NASA then provided three precise Shuttle-to-ISS fly-out launch trajectories over the five-minute launch window. The geometric grid was then coded into a physical optics-ray tracing RCS code called "X-Patch" and run on the U.S. Army's best (2005 era) supercomputer.

The Shuttle geometry had over 1.2 million facets. The RCS was calculated at 2048 frequencies, from 5.45-5.95 GHz, for every 1/3rd of a second, and for 302 seconds of mission elapsed time (MET). Given the three trajectories, the overall run-time was over two months of CPU time! The representation of the geometry is shown in Figure 22, and the constructed range-time intensity (RTI) data provided from X-patch is shown in Figure 23 on page 22.

If NASA understood what basic scattering structure *should be* in the Shuttle radar returns, undesired departing debris separating from the *real* RTI plots generated by the radar would be very visible. Although the RCS simulations were calculated every 1/3rd of a

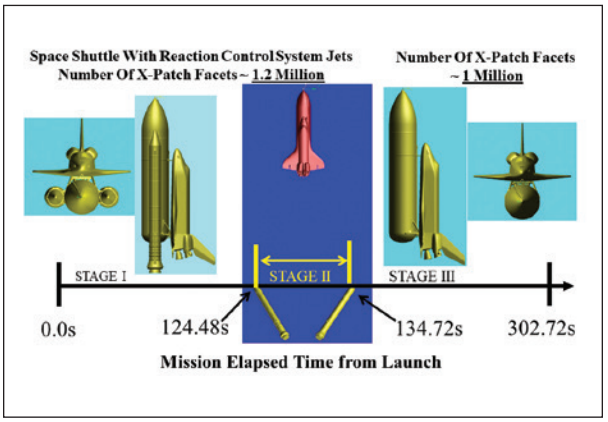

Figure 22: X-Patch geometry used for predicting C-band NDR radar fly-out range-time-intensity (RTI)

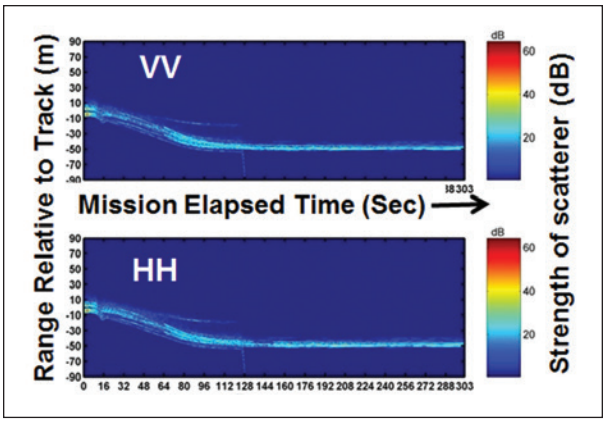

Figure 23: Supercomputer RTI calculations for one of *Discovery's* possible launch trajectories.

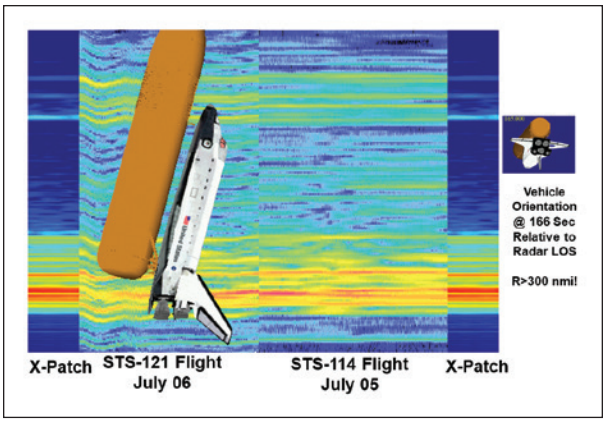

Figure 24: Comparing AFRL Xpatch and actual flight RTI data at 165 seconds mission elapse time

second, the real NDR created RTIs at a rate of 160 times a second, making ascent debris much easier to spot as it departed the Shuttle stack. Figure 23's predicted RTI data nearly overlaid measured RTI data from the Shuttle stack structural scattering. For validation purposes, Figure 24 shows a later comparison at MET = 165 seconds (post staging of SRB's) of the AFRL predicted (far left and far right) and actual RTI data from two Shuttle flights. (Note the vehicle is nearly 300 nautical miles downrange at this point!) While the plume was not modelled, these calculations provided crucial insight into the Shuttle stack scattering under the orbiter, well ahead of the plume.

PRACTICE MAKES PERFECT

With the NDR infrastructure constructed and staffed, and Discovery's July 2005 mission approaching, NASA wanted the NDR to simulate and practice their mission operations. Fortunately, there were several unmanned space launches out of the Kennedy Complex, and the NDR team "shadowed" several launches to learn real-time and post launch debris identification and reporting processes.

The most notable mission was the August 3, 2004 launch of a Delta-2 rocket carrying the NASA Mercury *Messenger* deep space probe. The Delta 2 was a great target to watch because it had nine strap-on solid rocket motor (SRM) boosters that used the same aluminum perchlorate propellant as the Shuttle SRBs. In addition, six of these boosters lit at lift off, burned for 60 seconds and were then ejected. The remaining three boosters then lit off, burned for another 60 seconds and were also ejected. In short, Delta-2 rockets generate lots of "normal debris" during a typical successful launch.

Figure 25 shows visual images of a daytime (not-Messenger) Delta 2 launch from an onboard and off-board camera, showing the moment of 3 air-ignited SRM's separating from the Delta 2 at MET = ~120 seconds. The *Messenger* launch was at 2:00 am, so we had no such visual camera support, making the *Messenger* mission a perfect night

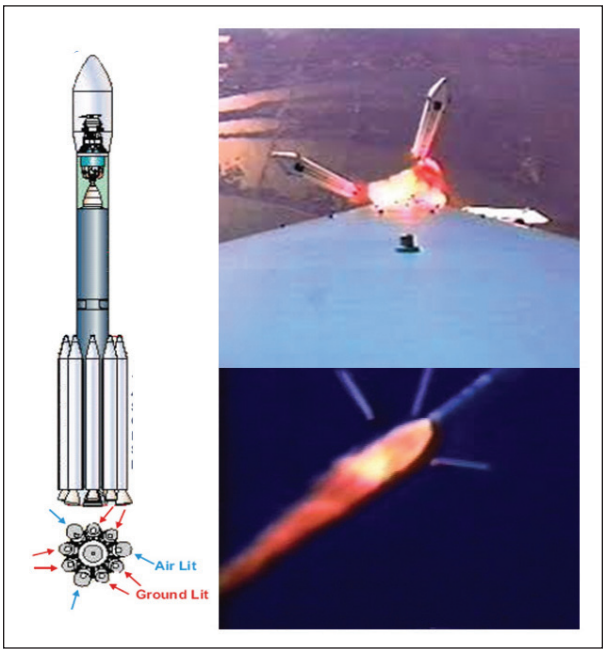

Figure 25: Air-lit SRM Separation from a typical Delta-2 Mission (Courtesy Space.com) [11]

launch dress rehearsal. The mission was successfully conducted, and the combined RTI and Doppler data processed overnight with clear and stunning results. During the period of six ground-lit SRM's separating from MET 88-98 seconds, we saw very dim and low-level debris events, including particulate Al_2O_3 "slag" ejecting from the tumbling but spent SRM booster rockets. [10]

This mission was so crucial to RTF that the NDR team got an unexpected visit from the seven astronauts of the STS-114 crew the following afternoon after the Delta-2 mission. Based on this success and several other unmanned launches prior to July 2005, the NDR was approved for use on the very first RTF mission, STS-114 *Discovery*.

STS-114 RETURN TO FLIGHT AND NASA'S FINAL TRIAD OF DEBRIS DETECTION

As the NDR awaited the first Shuttle launch, NASA was exercising for the first time a completely new 3-tiered debris safety protocol for STS-114 and all Shuttle launches to follow. First, during the launch and ascent phase, the NDR radar system and upgraded ground camera systems would monitor the Shuttle stack for launch debris. The most critical periods of the launch were near 62 seconds when the vehicle breaks the speed of sound, and at about 120 seconds when the two SRB boosters are separated. After 300 seconds, the vehicle is largely out of the atmosphere, so debris releases were of much lesser concern.

The powered flight mission lasts about 8.6 minutes, after which the NDR ground radar teams and photo teams go to work, pouring over all data to detect ascent debris events. NASA's debris teams were especially concerned about any liberated debris that had a secondary collision with the orbiter itself. Radar could see such "ricochet" events as debris tracks that suddenly changed trajectory. In addition, we had installed trajectory overlay software that allowed a 3-dimensional Shuttle to be overlaid with range-time-intensity radar plots, as shown previously in Figure 24. The radar and photo teams had precisely 24 hours to report their findings to Mission Control in Houston.

In the meantime, once in orbit, the Shuttle deployed a second-tier inspection tool on the end of the payload bay boom to self-inspect its entire thermal protection system. Any inspection results would be correlated with the debris events recorded by the combined radar and optical debris teams. Lastly, as the Space Shuttle approached the ISS, the third tier required the Orbiter to perform a full pirouette tumble maneuver before docking, allowing ISS astronauts to photograph the entire Shuttle surface area at close range. This photographic data was also downloaded to a dedicated damage assessment team comprised of subject matter experts who assessed the health of the TPS to determine its adequacy for safe Shuttle re-entry.

At the conclusion of mission, and normally after undocking with the ISS, the Shuttle would again deploy their tier 2 inspection tool in orbit to assure themselves that the TPS system had not be struck by *orbital debris* during its time on orbit. If all systems showed no damage, the Shuttle would reenter the atmosphere and land. Of course, in the event anything was damaged beyond the ability to repair on orbit, The Shuttle would simply re-dock with the ISS and await a second Shuttle for the ride back to earth.

July 26, 2005 dawned warm and clear at the NCAR sight of the NDR radar system. Nearly a dozen radar technicians and data processing experts were awaiting the launch of *Discovery* at 10:49 EDT. The launch window was a very narrow 5 minutes long. The launch occurred right on time, and the NDR acquired the Shuttle shortly after it cleared the launch tower. We had excellent tracks for both the C and X band NDR radars, and data was acquired without a hitch.

Then the bedlam of data analysis started. To speed things up, we parsed the mission radar data with parallel teams working 20 second segments of the flight from launch to 450 seconds. The optical teams, working independently at first, were doing the same with nearly 50+ optical HD movie cameras. Our debris event report was due to Mission Control leadership within 24 hours of launch, and the clock was running!

Almost immediately, we got our first challenging debris release. The external tank for the STS-114 return to flight system had been modified to remove much of the foam pieces that had a history of liberation in previous flights. But the first completely new tank design would not be delivered to NASA for three more flights, so everyone expected some foam debris events. One foam

release was detected by the on-board external tank camera (inset of Figure 26) which raised immediate concerns. It was a very small piece of foam debris, a tiny fraction of the size of *Columbia's* bipod ramp foam release. The camera clearly saw it depart and fly between the orbiter and tank, striking nothing. Despite its small size and very small corresponding RCS, the NDR not only detected this piece, but another smaller foam release the camera could not see. On its very first operational mission, the NDR proved that it could accomplish the debris detection and identification of material based on a combination of RCS, the location of the release, and its ballistic properties, B_n. So the ID strategy that effectively worked in the *Columbia* FD2 object investigation worked for Return to Flight ascent debris.

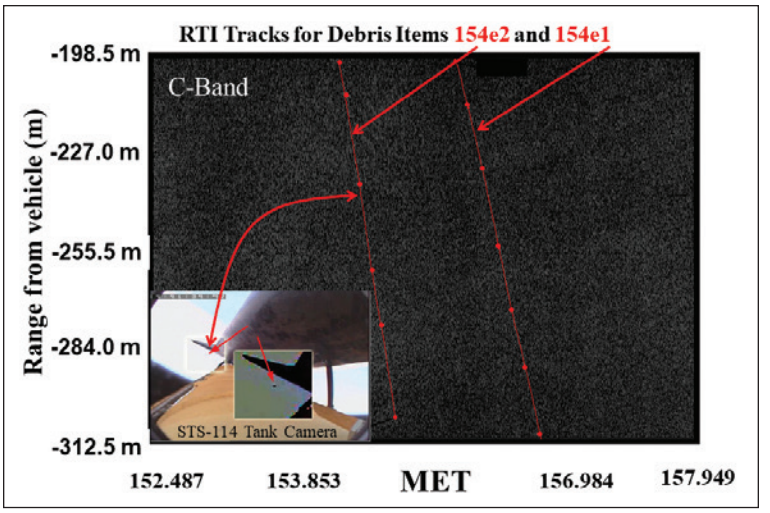

Figure 26: Radar and optical tracks of STS-114 PAL ramp foam debris liberation at MET=154 s

EPILOGUE – THE NDR'S 22 SHUTTLE MISSIONS

As I worked on the NDR console for the first four RTF missions, NDR evolved operationally. The downrange and in-range ship based Doppler radars, combined with the NCAR C-band site, now gave NASA a nearly 360° view of the Shuttle during launches. STS-117 (the fifth RTF mission) flew the first redesigned external tank. AFRL's Christopher Thomas and USN's Hardman and Stuble led mission debris analysis efforts and ultimately created automated software (later patented) which catalogued even harmless and miniscule debris events. Over time, NDR sensors revealed Shuttle's "war on ascent debris" had been won. The number and size of liberated particles went down dramatically during the critical first 300 seconds of powered flight. Fewer and fewer external tiles required repair after missions. NASA never wavered from their new safety protocol, and the 3-tiered ascent debris inspection protocol was used for the rest of the remaining Shuttle flights.

The Shuttle ultimately completed the ISS and was retired in 2011. As long as the ISS remains in operational service, NASA can proudly point to its completion in the Shuttle's storied legacy. In the end, NASA recognized those responsible for the myriad of EM analysis, EMI/EMC, and RCS measurements whose backstory played a huge but unseen role in Shuttle's return to flight.

ACKNOWLEDGEMENTS

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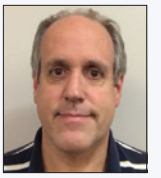
REDUCING BATTERY LIFE RISK IN MISSION CRITICAL IOT DEVICES

How Artificial Intelligence (AI) and Battery Emulation Can Help Reduce Risk

Brad Jolly received his B.S. in Mathematics from the University of Michigan. He has been with Keysight Technologies (previously Hewlett-Packard and Agilent Technologies) for more than 25 years, including roles in software R&D, UI design, learning products, application engineering, product support, training, product marketing, and product management.



By Brad Jolly

The Internet of Things (IoT) is quickly being adopted for use in mission-critical applications for several reasons. First, the IoT now incorporates increasingly sophisticated technologies, such as artificial intelligence (AI), augmented reality, edge computing, sensor fusion, and mesh networking to tackle problems of increasing difficulty and importance. Second, as recent supply chain challenges have demonstrated, margins for error and delay are slim at best. Third, the demand for increased healthcare, combined with resource scarcity, means many medical services must decrease in cost and become more efficient. Finally, the desire to conserve resources means devices must last longer and perform more reliably.

These trends present numerous business opportunities in fields that serve human health, safety, food production, environmental protection, and other key aspects of human flourishing. As technical challenges grow, each of the 5 Cs + 1 C of the IoT becomes more important. Some of these can use artificial intelligence (AI) as part of the solution.

THE 5 Cs + 1 C OF THE IoT

The term 5 Cs + I C of the IoT refers to the key characteristics that apply to all types of devices that utilize the IoT for transmitting and receiving data, as follows:

- **Connectivity**—Refers to a device's ability to create and maintain reliable connections, even during roaming. Mission-critical applications cannot accept delayed or lost data.
- **Compliance**—Means a device meets regulatory requirements for market access. Compliance problems must not delay implementation or lead to a product recall.
- **Coexistence**—A device's ability to perform properly in crowded RF bands. Mission-critical devices must avoid packet loss, data corruption, and retries that drain battery charge.
- **Continuity**—The ability of a device to operate without battery failure. Manufacturers must ensure long battery life, especially in implanted devices and emergencies where AC power is unavailable.
- **Cybersecurity**—IoT devices and infrastructure must be strong and resilient against cyber threats, including denial of service, contaminated data, or interception of sensitive information. Product development teams can use AI to simulate a variety of malware techniques based on exploits that have revealed vulnerabilities in the past.
- **Customer Experience**—Ideally, this means that customers enjoy a flawless, optimized experience with intuitive applications that operate seamlessly from end to end on multiple platforms. The challenge is that the number of possible paths through a series of related software applications is virtually limitless, far too many to test comprehensively. Fortunately, AI can once again guide automated test systems based on how recently code has been added, how many defects have been found in particular code sections, and other pertinent factors.

Increasing Demands on Device Batteries

Ensuring that IoT devices sufficiently address each of these key characteristics increases the demands on batteries. Previously, a simple sensor device might wake up, take a few measurements, transmit data to a hub or access point, and return to sleep. Today's mission-critical devices might incorporate multiple sensors, microcontrollers, numeric processors, six-axis accelerometers, sensor fusion logic, voltage converters, power management systems, image processors, microphones, multiple radios, memory, encryption processors, and other hardware components that drain battery life.

Furthermore, operating environments are increasingly challenging, with temperature changes, irregular duty cycles, and electromagnetically crowded spectrum. Some operate in locations that are difficult or hazardous to access, and some operate inside animal or human bodies. These factors place unprecedented demands on device batteries.

For medical devices, the quality of a device's battery life often has health implications. Even in non-critical applications, premature failure can lead to complaints in post-market surveillance monitored by regulatory agencies. Complaints that become excessive or increase patient risk can have huge costs for the manufacturer.

CHALLENGES FOR BATTERY TEST DURING PRODUCT DEVELOPMENT

Battery testing presents several challenges during product development. Using real batteries might seem ideal, but there are limitations associated with real batteries.

Difficulty in Determining Initial State of Charge

Batteries may be fully charged at the factory, but the minute they leave the charger, they begin discharging due to internal resistance. This self-discharge rate varies by battery technology; lithium-ion cells have a lower self-discharge rate than nickel-cadmium (NiCad) or nickel metal hydride (NiMH) batteries.[1] The discharge rate varies as a function of time and temperature, and this performance loss is sometimes referred to as calendar fade.[2] An engineer cannot assume that a new battery is at precisely 100% state of charge.

Variation Within and Across Manufacturing Lots

Like any manufacturing process, battery manufacturing has normal variations. Even within a given lot or date code, batteries vary. There is often additional variability across different factories. This does not mean that manufacturers release batteries that are out of specification, but the tolerances are there for a good reason. Battery run-down tests should be conducted with batteries from different lots acquired at different times.

Variation Due to Recharging

A re-charged battery has different discharge characteristics than a new battery. This effect, known as cycle fade, is due to mechanisms that affect the cathode or anode. For example, in a lithium secondary cell, the anode ages due to graphite exfoliation, electrolyte decomposition, and lithium plating that leads to corrosion. Similarly, the cathode undergoes aging due to several factors, including binder decomposition, oxidation of conductive particles, micro-cracking, and structural disordering.[3] You can limit this variability by ensuring that the battery is fully charged and using a battery cycler that conditions the battery by cycling it from fully discharged to fully charged.

THE IMPORTANCE OF BATTERY EMULATION

Some test engineers attempt to use a basic DC power supply to emulate a battery for battery run-down test. This can be accurate, but only if the engineer uses a specialized battery emulator that models its output according to a battery profile. A standard power supply does not perform like a battery, but a battery emulator uses specialized features such as programmable output resistance and fast transient response to emulate a real battery.

For example, a test engineer can use an advanced battery test and emulation solution to quickly and easily profile and emulate a battery's performance. The engineer can then use this solution to charge or discharge a battery of any chemistry to create a

State of Charge(%)	Open Circuit Voltage(V)	Internal Resistance(ohm)
100.00	9.609423	7.544065
99.50	8.828673	3.889564
99.00	8.645126	3.791465
98.50	8.516480	3.767940
98.00	8.411436	3.780916
97.50	8.320710	3.804418
97.00	8.240466	3.840828
96.50	8.167970	3.886445
96.00	8.102751	3.927822
95.50	8.043658	3.971063
95.00	7.990255	4.014665
94.50	7.942882	4.057762
94.00	7.899871	4.098643

Figure 1: The first few lines in a battery model with 200 data points

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battery model of up to 200 points, with each point including the battery's open circuit voltage (Voc), series resistance (Ri), and state of charge (SoC).

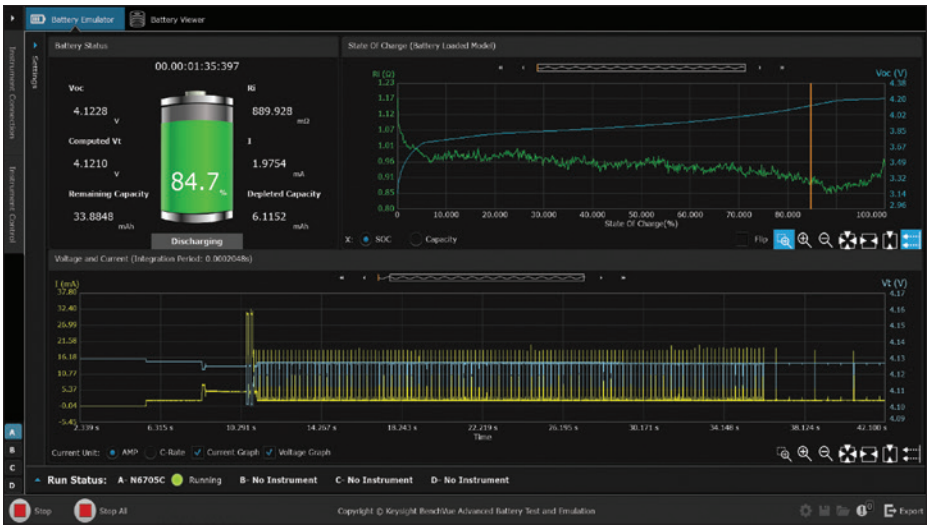

Figure 2: An example of an advanced battery test and emulation software display

Battery emulation is especially important when the test engineer is changing the device's hardware configuration or firmware program. Without a consistent battery emulation, the engineer cannot know whether the variation in run-down time is due to the intentional modifications or variability in the batteries used to perform the run-down test, as described above. Because battery life is closely related to the other "Cs" of the IoT, any AI techniques that improve overall device operation can also have a positive impact on battery life.

By using such a profile with a battery emulator, the engineer can avoid needing to use an actual battery, thereby eliminating the associated uncertainty and variability. In addition, a battery emulator lets the user quickly set the SoC to any point in the model at the beginning of a test.

For example, the engineer may want to see how the device behaves near the end of battery life by starting the test with the SoC set to 15%. To use an actual battery, one would have to discharge an actual battery to 15% and verify that it was at that level. This poses at least three challenges. First, one would have to discharge a battery to the desired SoC. This could take hours on a real battery, but one can set the SoC on a battery emulator in a fraction of a second. Second, the engineer would have to somehow determine the SoC of the battery. Third, every time you charge or discharge a battery, you change the battery behavior due to the cycle fade mentioned previously.

USING THE RESULTS

The engineer can use the information at states of charge near the end of battery life to thoughtfully degrade device performance and extend device runtime. For example, the engineer could choose to transmit data half as often as usual. In addition to extending battery life, this would alert the user that the battery is running out. The engineer could also decide to transmit only minimum and maximum data values or to only transmit when values change by more than some amount. The engineer could also choose to refuse firmware updates once the SoC falls below a small percentage. There would be little point in having a device battery fail during the middle of a firmware update.

CONCLUSION

Battery life is becoming increasingly important as the IoT moves into more mission-critical applications, including connected medical devices. Using real batteries to test these devices leads to many problems during the product development process. Test engineers can use advanced battery test and emulation solutions to create detailed, high resolution battery profiles. They can then use these profiles to emulate the battery and get fast insights into battery performance at various states of charge and then modify firmware to optimize device performance.

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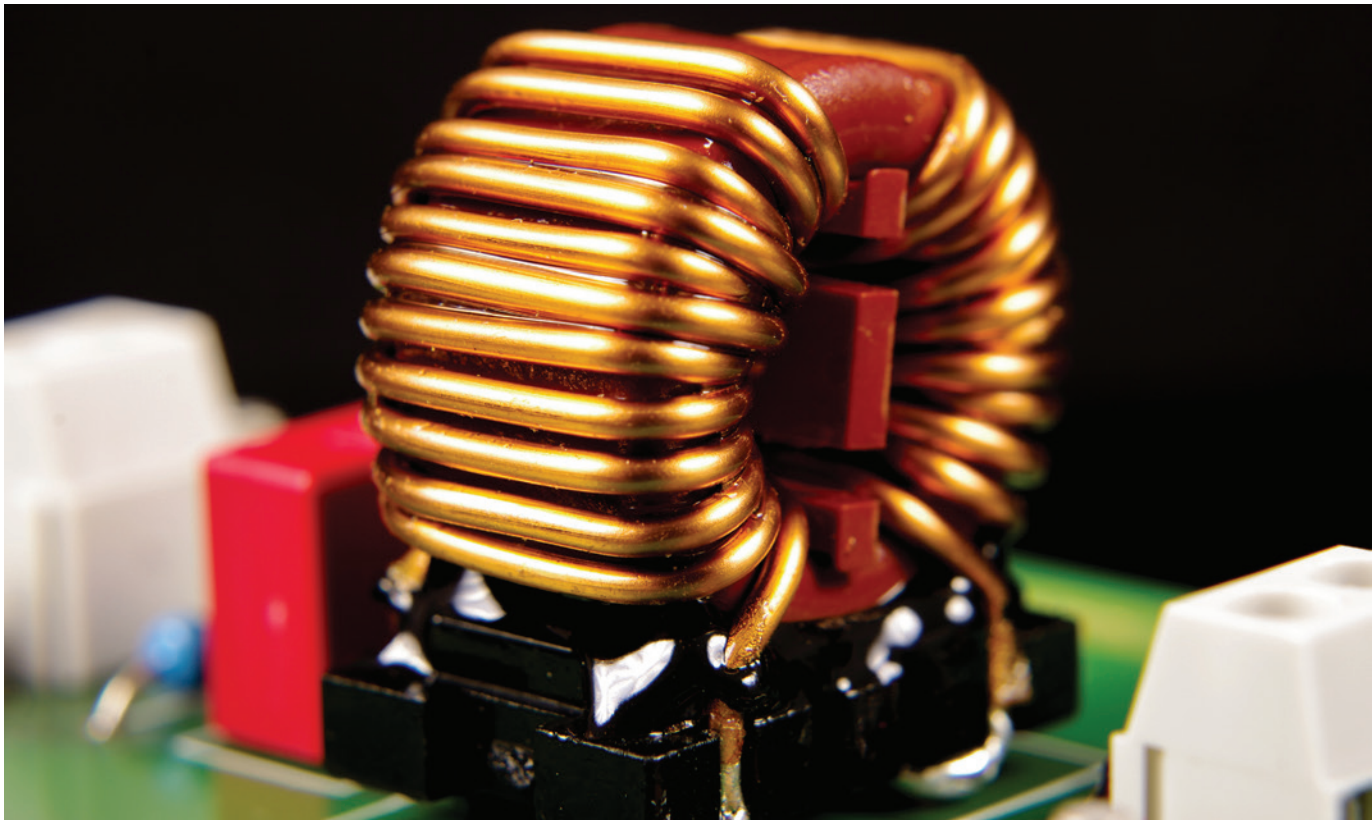
COMMON MODE FILTER DESIGN GUIDE



The selection of component values for common mode filters need not be a difficult and confusing process. The use of standard filter alignments can be utilized to achieve a relatively simple and straightforward design process, though such alignments may readily be modified to utilize pre-defined component values.

GENERAL

Line filters prevent excessive noise from being conducted between electronic equipment and the AC line. Generally, the emphasis is on protecting the AC line. Figure 1 shows the use of a common mode filter between the AC line (via impedance matching circuitry) and a (noisy) power converter. The direction of common mode noise (noise on both lines occurring simultaneously referred to as earth ground) is from the load and into the filter, where the noise common to both lines becomes sufficiently attenuated. The resulting common mode output of the filter onto the AC line (via impedance matching circuitry) is then negligible.

The design of a common mode filter is essentially the design of two identical differential filters, one for each of the two polarity lines with the inductors of each side coupled by a single core (see Figure 2).

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By Leonard Crane

For a differential input current ((A) to (B) through L1 and to (A) through L2), the net magnetic flux which is coupled between the two inductors is zero.

Any inductance encountered by the differential signal is then the result of imperfect coupling of the two chokes. They perform as independent components with their leakage inductances responding to the differential signal, and the leakage inductances attenuate the differential signal.

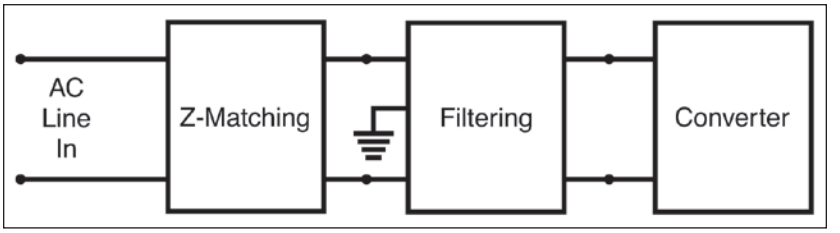


Figure 1: Generalized line filtering

When inductors L1 and L2 encounter an identical signal of the same polarity referred to ground (common mode signal), they each contribute a net, non-zero flux in the shared core. The inductors thus perform as independent components with their mutual inductance responding to the common signal: the mutual inductance then attenuates this common signal.

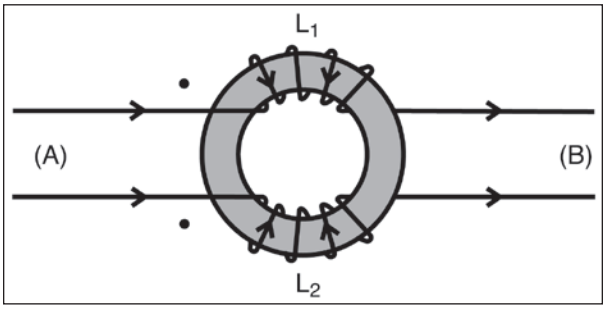


Figure 2: The common mode inductor

THE FIRST ORDER FILTER

The simplest and least expensive filter to design is a first order filter. This type of filter uses a single reactive component to store certain bands of spectral energy without passing this energy to the load. In the case of a low pass common mode filter, a common mode choke is the reactive element employed.

The value of inductance required of the choke is simply the load in Ohms divided by the radian frequency at and above which the signal is to be attenuated.

For example, attenuation at and above 4000 Hz into a 50Ω load would require a 1.99 mH (50/(2π x 4000)) inductor. The resulting common mode filter configuration is shown in Figure 3.

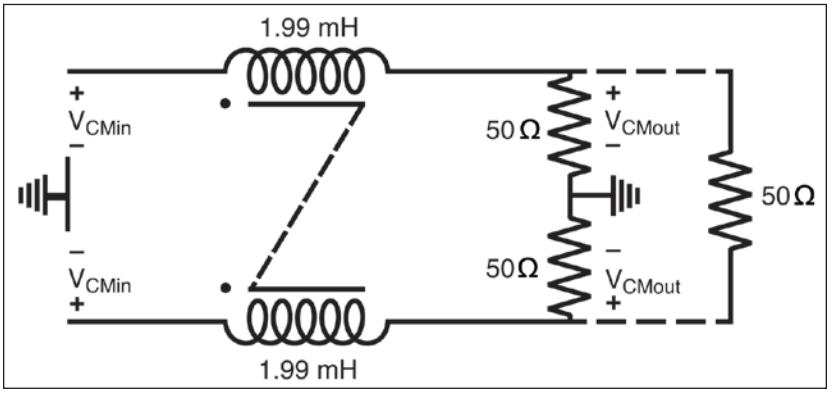


Figure 3: A first order (single pole) common mode filter

The attenuation at 4000 Hz would be 3 dB, increasing at 6 dB per octave. Because of the predominant inductor dependence of a first order filter, the variations of actual choke inductance must be considered. For example, a ± 20% variation of rated inductance means that the nominal 3 dB frequency of 4000 Hz could be anywhere from 3332 Hz to 4999 Hz.

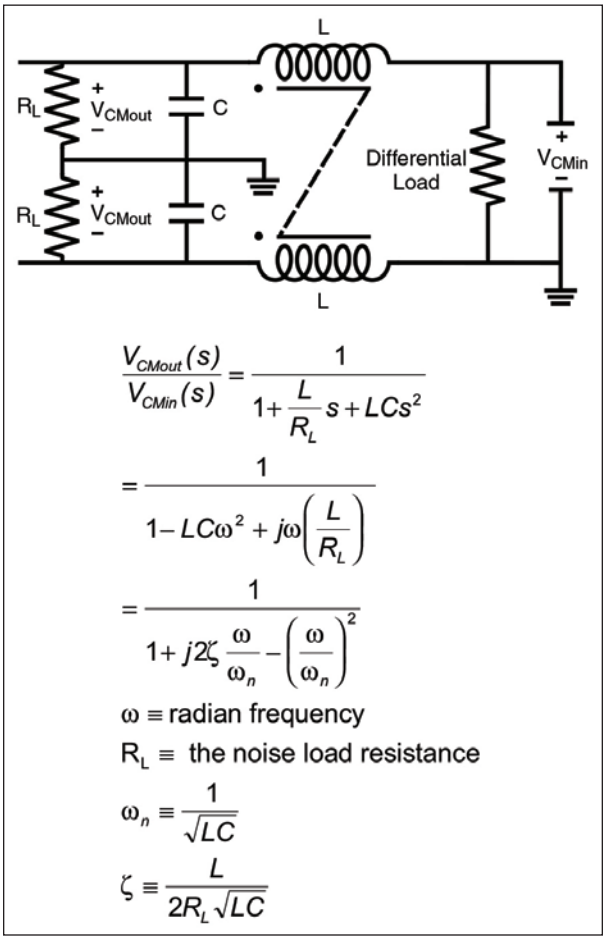
It is typical for the inductance value of a common mode choke to be specified as a minimum requirement, thus ensuring that the crossover frequency not be shifted too high. However, some care should be observed in choosing a choke for a first order low pass filter because an inductance with a much higher than typical or minimum value may limit the choke's useful band of attenuation.

SECOND ORDER FILTERS

A second order filter uses two reactive components and has two advantages over the first order filter. Ideally, a second order filter: 1) provides 12 dB per octave attenuation (four times that of a first order filter) after the cutoff point; and 2) provides greater attenuation at frequencies above inductor self-resonance (see Figure 4).

The design of a second order filter requires more care and analysis than a first order filter to obtain a suitable response near the cutoff point, but there is less concern needed at higher frequencies, as previously mentioned.

One of the critical factors involved in the operation of higher order filters is the attenuating character at the corner frequency. Assuming tight coupling of



$$\frac{V_{CMout}(s)}{V_{CMin}(s)} = \frac{1}{1+\frac{L}{R_L}s+LCs^2}$$

$$= \frac{1}{1-LC\omega^2+j\omega\left(\frac{L}{R_L}\right)}$$

$$= \frac{1}{1+j2\zeta\frac{\omega}{\omega_n}-\left(\frac{\omega}{\omega_n}\right)^2}$$

$\omega \equiv$ radian frequency

$R_L \equiv$ the noise load resistance

$$\omega_n \equiv \frac{1}{\sqrt{LC}}$$

$$\zeta \equiv \frac{L}{2R_L\sqrt{LC}}$$

Figure 4: Analysis of a second order (two pole) common mode low pass filter

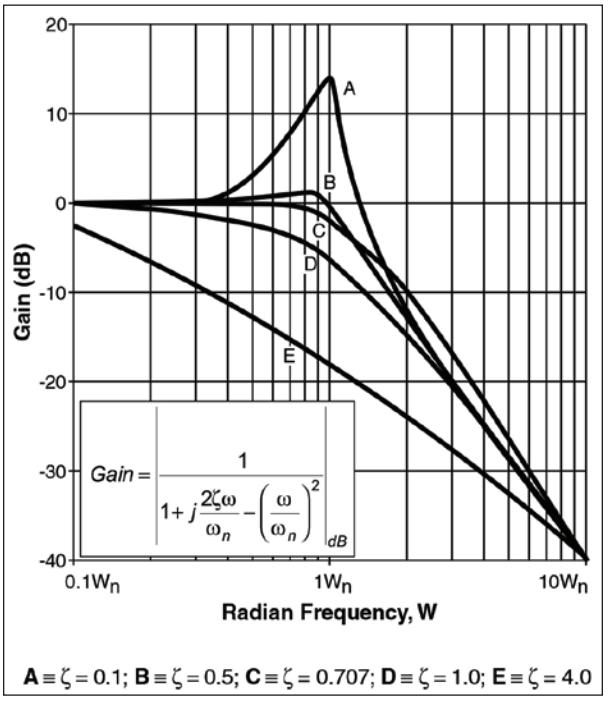


Figure 5: Second order frequency response for various damping factors (ζ)

the filter components and reasonable coupling of the choke itself (conditions we would expect to achieve), the gain near the cutoff point may be very large (several dB). Moreover, the time response would be slow and oscillatory. On the other hand, the gain at the crossover point may also be less than the presumed -3 dB (3 dB attenuation), providing a good transient response, but frequency response near and below the corner frequency could be less than optimally flat.

In the design of a second order filter, the damping factor (usually signified by the Greek letter zeta (ζ)) describes both the gain at the corner frequency and the time response of the filter. Figure 5 shows normalized plots of the gain versus frequency for various values of zeta.

As the damping factor becomes smaller, the gain at the corner frequency becomes larger, and the ideal limit for zero damping would be infinite gain. The inherent parasitics of real components reduce the gain expected from ideal components but tailoring the frequency response within the few octaves of critical cutoff point is still effectively a function of ideal filter parameters (i.e., frequency, capacitance, inductance, resistance).

For some types of filters, the design and damping characteristics may need to be maintained to meet specific performance requirements. However, for many actual line filters, a damping factor of approximately 1 or greater and a cutoff frequency within about an octave of the calculated ideal should provide suitable filtering.

The following is an example of a second order low pass filter design:

1. *Identify the required cutoff frequency*—For this example, suppose we have a switching power supply (for use in equipment covered by UL 478) that is 24 dB noisier at 60 kHz than permissible

for the intended application. For a second order filter (12 dB/octave roll-off), the desired corner frequency would be 15 kHz.

2. *Identify the load resistance at the cutoff frequency*—Assume R_L = 50 Ω
3. *Choose the desired damping factor*—Choose a minimum of 0.707, which will provide 3 dB attenuation at the corner frequency while providing favorable control over filter ringing.
4. Calculate required component values using the following equations:

$$\omega_n = 2\pi f_n = 94248 \text{ rad / sec}$$

$$C = \frac{1}{L\omega_n^2}$$

$$\zeta = 0.707 = \frac{L\omega_n}{2R_L}$$

$$L = 750\mu H$$

5. Choose available components as follows:

   C = 0.05 µF (Largest standard capacitor value that will meet leakage current requirements for UL 478/ CSA C22.2 No. 1: a 300% decrease from design)

   L = 2.1 mH (Approximately 300% larger than design to compensate for reduction or capacitance)

6. Calculate actual frequency, damping factor, and attenuation for components chosen using the following equations:

$$\frac{1}{2\pi\sqrt{LC}} = 15532 \text{ Hz (very nearly 15 KHz)}$$

   ζ = 2.05 (a damping factor of about 1 or more is acceptable

   Attenuation = (12 dB/octave) x 2 octaves = 24 dB

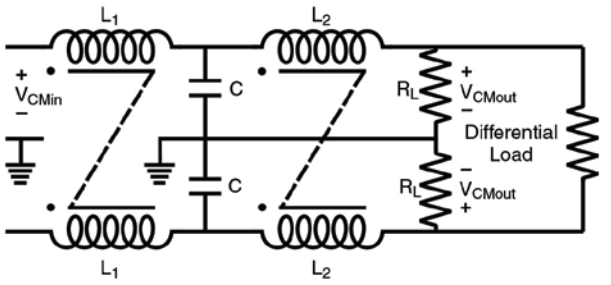
7. The resulting filter is that of Figure 4 with: L = 2.1 mH; C = 0.05 µF; R_L = 50 Ω

Note: Damping factors much greater than 1 may cause unacceptably high attenuation of lower frequencies, whereas a damping factor much less than 0.707 may cause undesired ringing and the filter may itself produce noise.

THIRD ORDER FILTERS

A third order filter ideally yields an attenuation of 18 dB per octave above the cutoff point (or cutoff points if the three corner frequencies are not simultaneous). This is the prominently positive aspect of this higher order filter. The primary disadvantage is cost since three reactive components are now required. Higher than third order filters are generally cost-prohibitive.

The design of a generic filter is readily accomplished by using standard alignments such as a maximally flat alignment (also known as a Butterworth alignment). Figure 6 shows the general analysis and component relationships to the Butterworth alignments for a third order low pass filter. Butterworth alignments provide an inherent z of 0.707 and a -3 dB point at the crossover frequency. The Butterworth alignments for the first three orders of low pass filters are shown in Figure 7.



$$\frac{VCMout(s)}{VCMin(s)} = \left(\frac{R_L}{R_L + L_2 s}\right)\left(\frac{\frac{(R_L + L_2 s)}{sC}}{\frac{(R_L + L_2 s)}{sC} + R_L L_1 s + L_2 L_1 s^2 + \frac{L_1 s}{sC}}\right)$$

$$= \frac{1}{1 + \frac{L_1 + L_2}{R_L} s + L_1 C s^2 + \frac{L_1 L_2 C}{R_L} s^3}$$

$$\text{Butterworth} \rightarrow \frac{1}{1 + \frac{2s}{\omega_{n1}} + \frac{2s^2}{\omega_{n2}} + \frac{s^3}{\omega_{n3}}}$$

$$\frac{(L_1 + L_2)}{R_L} = \frac{2}{\omega_{n1}} \; ; \; \omega_{n1} = \frac{2R_L}{(L_1 + L_2)}$$

$$L_1 C = \frac{2}{\omega_{n2}^2} \; ; \; \omega_{n2} = \frac{1.414}{\sqrt{(L_1 C)}}$$

$$\frac{L_1 L_2 C}{R_L} = \frac{1}{\omega_{n3}^3} \; ; \; \omega_{n3} = \omega_{n2}^2 \frac{R_L}{2L_2} = \omega_{n2}^2 \omega_{n4}$$

$$\omega_{n4} = \frac{R_L}{2L_2}$$

Figure 6: Analysis of a third order (three pole) low pass filter where ω_1, ω_2, and ω_4 occur at the same -3dB frequency of ω_0

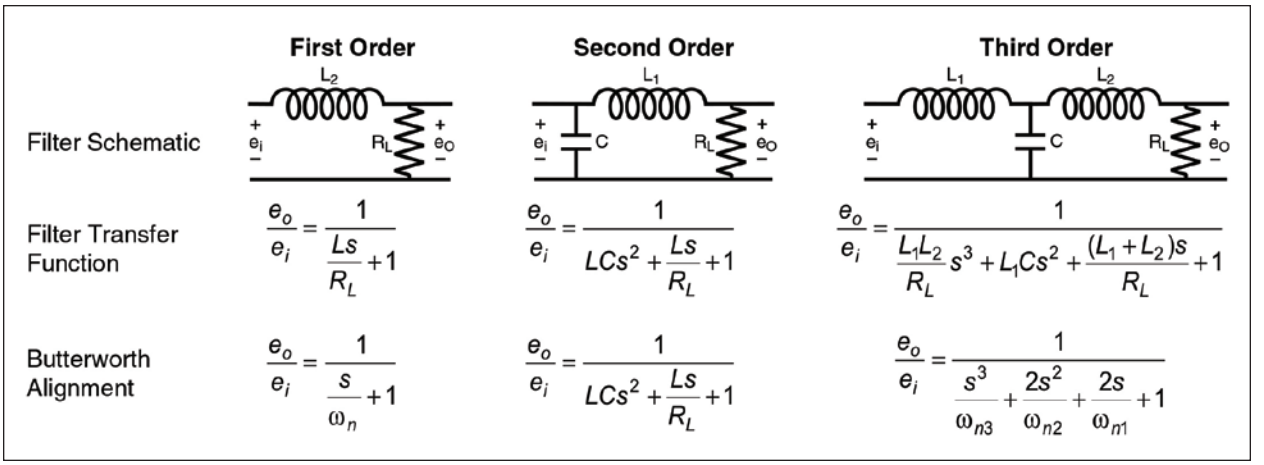


Figure 7: The first three order low pass filters and their Butterworth alignments

The design of a line filter need not obey the Butterworth alignments precisely (although such alignments provide a good basis for design). Moreover, because of leakage current limits placed upon electronic equipment (thus limiting the amount of filter capacitance to ground), adjustments to the alignments are usually required, but they can be executed very simply as follows:

1. First design a second order low pass with $\zeta \geq 0.5$;
2. Add a third pole (which has the desired corner frequency) by cascading a second inductor between the second order filter and the noise load so that:

   $L = R/(2\pi f_c)$

   Where f_c is the desired corner frequency.

DESIGN PROCEDURE

The following example determines the required component values for a third order filter (for the same requirements as the previous second order design example):

1. List the desired crossover frequency, load resistance:

   Choose f_c = 15000 Hz

   Choose R_L = 50 Ω
2. Design a second order filter with ζ = 0.5 (see second order example above)
3. Design the third pole:

   $R_L/(2\pi f_c) = L_2$

   $50/(2\pi 15000)$ = 0.531 mH
4. Choose available components and check the resulting cutoff frequency and attenuation:

   L2 = 0.508 mH

   $f_n = R/(2\pi L_1)$ = 15665 Hz

   Attenuation at 60 kHz: 24 dB (second order filter) + 2.9 octave × 6 = 41.4 dB
5. The resulting filter configuration is that of Figure 6 with:

   L_1 = 2.1 mH

   L_2 = 0.508 mH

   RL = 50 Ω

CONCLUSIONS

Specific filter alignments may be calculated by manipulating the transfer function coefficients (component values) of a filter to achieve a specific damping factor.

A step-by-step design procedure may utilize standard filter alignments, eliminating the need to calculate the damping factor directly for critical filtering. Line filters, with their unique requirements, yet non-critical characteristics, are easily designed using a minimum allowable damping factor.

Standard filter alignments assume ideal filter components, but this does not necessarily hold true, especially at higher frequencies.

THE IMPACT OF TIN WHISKER FORMATION ON VEHICLE ELECTRONICS

Editor's Note: *The paper on which this article is based was originally presented at the 2019 IEEE International Symposium on Product Safety Engineering held in San Jose, CA in May 2019. It is reprinted here with the gracious permission of the IEEE. Copyright 2019, IEEE.*

INTRODUCTION

Tin whiskers are small, typically hair-like structures that can form naturally from the surface of tin components in electronic devices (Figure 1). Tin whisker formation is a well-documented phenomenon that has been studied for decades. Throughout this time, little consensus has been reached regarding the particular mechanisms behind tin whisker formation. Whisker formation is believed to be a diffusion-controlled process motivated by stresses, both internal and external; however, the wide range of factors that may produce material stresses makes it exceedingly difficult to identify or isolate individual factors.

Previously, the use of lead-based alloys in electronic components and finishes mitigated the formation of tin whiskers. This protective mechanism was lost for many classes of devices with the passing of the Restriction of Hazardous Substances Directive 2002/95/EC by the European Union - followed by the adoption of similar restrictions in many other countries and regions – in which the requirement to use lead- free materials in electronic components and

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By Michelle Kuykendal, Daniel Kingsley, and Ashish Arora

devices became mandatory. Tin-alloys offer a cost-effective alternative with high solderability and good corrosion resistance. The market choice to use tin-based alloys for solder connections and finishes has led to the reemergence of issues regarding tin whisker formation.

The consumer electronics market has grown exceedingly rapidly in recent decades, which has driven the development of faster and smaller electronics technologies. As the demand for faster processing and smaller packaging has increased, the vulnerability of highly compact semiconductor devices and shortened interconnect spaces has also increased. Electronics are embedded in countless devices across products and industries, and similarly countless automated systems depend on their precision and reliability. These competing drivers must be factored into a wide range of engineering considerations for the design and operation of modern electronic devices.

ADAS and Autonomous Driving Systems

Electronics failures in non-safety critical systems are inarguably a nuisance. In contrast, for safety-critical systems strategies must be in place for error handling and failure mitigation when a problem arises. These types of control systems are critical to the safe operation of systems in aviation, military applications, and the automotive industry. Even what the layperson thinks of as a traditional vehicle on the road today is dependent on a broad range of interwoven electronic systems. These systems include:

- Powertrain and chassis control
- Engine, transmission, hybrid control
- Steering, brake, suspension
- Integrated systems/services
- Multimedia (infotainment) applications
- Car audio, traffic information
- Body electronics
- Instrument panel, key, door, window, lighting
- Air bag, seat belt

Adoption of new driver assist technologies requires an extensive infrastructure building on those electronic systems listed above. Electronically controlled features of autonomous vehicles expand the above list to more sub-systems including, but not limited to:

- Parking assistance
- Lane departure warning and lane keeping assistance
- Electronic stability control
- Forward collision warning
- Automatic emergency braking
- Dynamic cruise control
- Car navigation and position sensing
- Vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communications
- Driver alertness monitoring

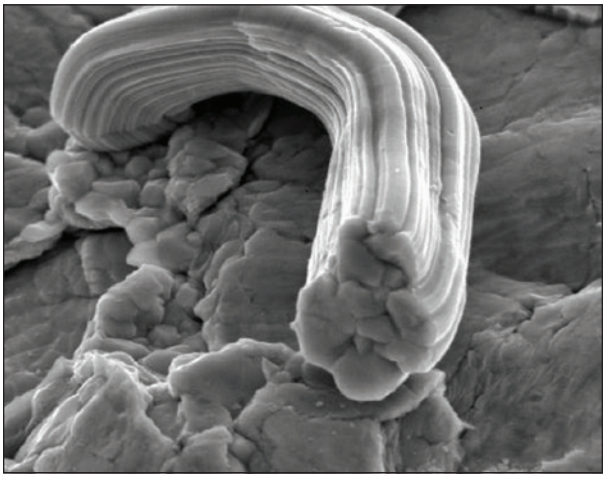

Figure 1: A straited tin whisker [1]

Many of the essential technologies supporting automotive sensors and electronic actuators used to navigate the complex environment of roads, vehicles, signs, and pedestrians in driver- assistance systems are not fundamentally new; however, the newly developing way in which these devices are used to decide, for example, how a vehicle should traverse an intersection has driven the need to increase the safety and reliability of these systems. Continuous innovation and evolution in system integration and packaging is crucial to achieving such advancement in embedded automotive electronics.

The utilization of components not originally intended for automotive applications has brought about new challenges as these systems are employed in the vastly different automotive environments of temperature and humidity extremes, sand and salt exposure, and vibration and shock, to name just a few. A relatively new entrant into the automotive industry is the use of LIDAR systems to image a vehicle's surroundings, identify detected objects and infer how they might change or move a moment later. A LIDAR technology system that was previously developed for indoor, low-risk consumer electronics applications requires significantly less rigor in its design, documentation, and validation than a LIDAR being used for pedestrian detection in an autonomous vehicle. Every aspect of an electronic system such as this one in an autonomous vehicle is critical to ensuring passenger, pedestrian, and infrastructure safety.

The typical trend in consumer electronics is a steady push for miniaturization of components and increasingly compact packaging. The resulting evolutionary course has allowed for increasingly dense packages capable of higher and higher levels of performance. This trend has been fundamental to the rapid evolution and proliferation of electronics in seemingly all aspects of consumer products; however, the vast majority of these implementations are not designed with consideration for safety-critical operations, as by-and-large they are not intended for such applications. The design paradigms of consumer electronics cannot be applied in their traditional sense to safety- critical applications, as a number of enabling features of low- cost electronics run counter to safety-critical design requirements. High-density arrays of components and electrical circuit traces present multiple mechanisms by which faults may be induced, and packaging of multiple sub-systems into integrated systems may allow for unintended or unmanageable propagation of faults between sub-systems. In effect, as the design space of integrated systems broadens, so too do the potential effects of fault or failure.

With the removal of lead from tin solders and finishes, the importance of addressing and implementing mitigation strategies relating to tin whisker formation has become imperative. Many of the failure modes present in driver assistance-enabled vehicles are the same failure modes of systems in cars today. However, there is a growing trend of greater integration of automotive electronic systems and the diverse electronic components and sub-systems must be interoperable, not only with respect to electrical function, but from physical packaging and positioning requirements.

Development and implementation of a new technology requires extensive safety considerations within the product life cycle. These requirements can lead to unforeseen second and third order effects as the function—or failure—of one component may cascade in numerous ways. With the heavy reliance of autonomous vehicles on electronic systems, including driver assist systems currently available in vehicles on the road today, it is important to understand the implications of tin whisker formation on vehicle electronics.

TIN WHISKER FORMATION AND IMPLICATIONS

Metallic whiskers are electrically conductive structures that can form from a variety of metals, including gold, silver, zinc cadmium, indium, and antimony, but are most often associated with tin. Tin whiskers most often occur where tin has been used as a final surface finish, for example on surface mounted integrated circuit pins (Figure 2). These tin whisker

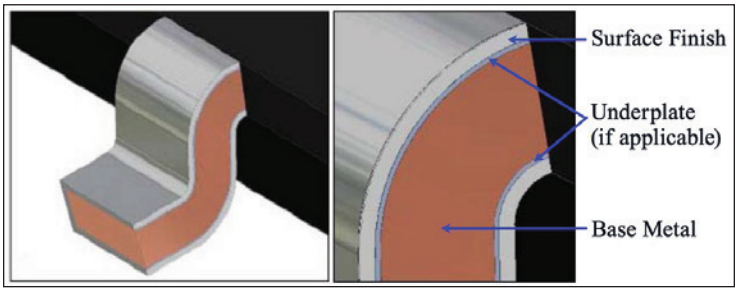

Figure 2: Cross-sectional view of component surface finishes [3]

structures have often observed to have lengths of several millimeters but can grow to lengths in excess of 10mm. [2]

Incubation time for whiskers can be from days to years, meaning that long-term electronics applications are vulnerable to tin whisker growth. Scientists cannot accurately predict whisker formation other than to say whiskers are likely to form on pure tin. Tin whiskers can be hard to detect, especially because of their extremely small cross-sectional dimensions of approximately 1-10um (approximately one tenth the diameter of a human hair) (Figure 3). While these structures are small, due to their electrical conductivity, even microscopic tin whiskers can carry current for a short period of time.

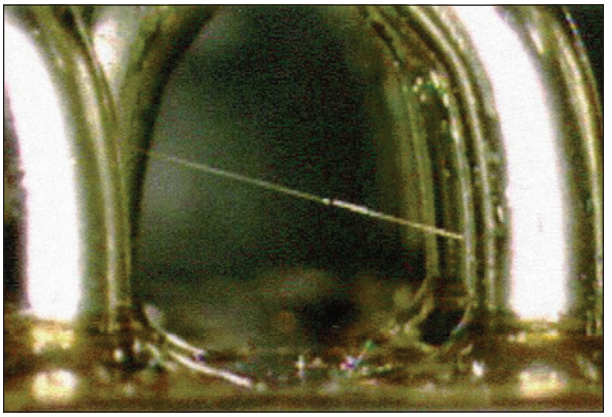

Figure 3: Tin whisker growing between pure Sn plated hook terminals of an electromagnetic relay [6]

A wide range of factors are attributed, but not proven, to cause tin whisker growth, often believed to be a result of direct or indirect contribution to material compressive stresses or promotion of tin diffusion. [4] Factors that may, under certain circumstances, cause tin whisker growth include:

- Temperature
- Humidity
- Surface finish
- Internal stresses
- External stress
- Temperature change
- Vibration
- Lattice structure
- Lattice interstitials
- Magnetic field
- Voltage differential
- Altitude (ambient pressure)
- Manufacturing or process abnormalities or damage

This wide range of contributing factors presents a complex interplay of first, second, and higher-order effects that, to date, have not been fully mapped. It is quite possible that multiple individual factors in combination may be required to achieve whisker growth on a particular electronic component. It is important to note that studying tin whiskers with accelerated life tests has proven challenging because they do not appear to grow any faster or sooner in numerous simulated environments.[5] This implies that certain growth factors, or combinations of factors, may be so poorly understood as to not be properly represented in accelerated life tests. The present consensus in the literature is that conditions that increase the stress in a tin film or promote diffusion tend to induce whisker formation. [6], [7] For example, a mismatch in coefficients of thermal expansion between a tin surface finish and the base material can create stress in the finish as temperature varies. Conversely, stress can be generated from within the tin

surface finish due to variability in the microstructure of the tin surface finish. The Joint Electron Device Engineering Council (JEDEC) notes that:

> *"[T]here is at present no way to quantitatively predict whisker lengths over long time periods based on the lengths measured in short-term tests… [T]he fundamental mechanisms of tin whisker growth are not fully understood and acceleration factors have not been established. Therefore, [accelerated aging testing] does not guarantee that whiskers will or will not grow under field life conditions"* [3]

Induced Faults Resulting from Tin Whisker Formation

The formation of tin whiskers can have detrimental or catastrophic effects on electronic systems through a number of means. Tin whiskers may form across conductors or may break from tin structures and fall onto other conductors thereby forming a conductive bridge. In these scenarios, the conductive whisker may create an electrical connection where one was not intended. If these conductors are of similar voltage potential, then no short circuit current will flow. However, if the conductors are at differing potentials (i.e., between power and ground) then a short circuit current will flow but may be brief as the microscopic tin filament may be consumed by the event. Many electrical circuits in automotive electronics are current limited, and in the event that a tin whisker forms a short circuit across conductors in a current limited circuit, then the short circuit current that flows will be inherently limited by design. In other cases, intermittent short circuits may occur if the whisker is moved into and out of contact by vibration, air currents, or other means. In conditions involving both high currents and voltages, a whisker may be vaporized and form a vapor arc composed of metallic ions; such arcs may sustain very high currents and may cause extreme damage. [8]

Tin whiskers may also severely impact the performance of micro-electromechanical systems (MEMS) and optical devices as a physical contaminant. A tin whisker that grows or falls onto a MEMS structure can interact with that component's operation by significantly altering mechanical properties (e.g., the mass of an accelerometer) and thus alter the overall performance of the device. Likewise, should a whisker become deposited on optical components, it may severely degrade performance, for example, by physically obstructing the lens and therefore the operation of the entire device. Similarly, tin whisker formation on RF components used for communications may have detrimental effects on the functionality and performance of devices due to the tin whisker altering the frequency properties of an antenna used for either transmitting or receiving radio signals. Due to the high precision of many of these electronic and electro-mechanical devices, even subtle alterations that tin whiskers may have on the device's physical and electrical properties should be considered.

Electronic system failure modes can range from anomalous output signals to catastrophic component failure, and these failure modes must be analyzed and understood such that adequate mitigation strategies can be employed. For example, an electrical short circuit across two pins of an automotive sensor connector due to tin whisker growth across the proximal conductive surfaces may result in an incorrect signal being sent to an associated control module. However, mitigation strategies that check and confirm that the sensor output is correct can act to trigger a diagnostic trouble code upon error detection and transition the vehicle into a safe operating mode.

STANDARDS AND GUIDELINES RELATED TO TIN WHISKERS

While the details of tin whisker formation are not fully understood, their detrimental effects are, and some standards have been developed to assess whisker growth and thereby manage the risk presented by whiskers. While these early standards may be limited in scope, it is expected that they will be further matured as understanding of whisker growth mechanisms become better understood.

IEC60068-82-2 – *Environmental Testing Part 2-82: Whisker Test Methods for Electronic And Electronic Components* provides an international standard for ambient environment, elevated temperature and humidity and temperature cycling of electronic components to determine potential for whisker growth. This standard also offers a maximum acceptable whisker length allowable in devices and components following test series. [9]

JESD22-A121A – *Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes* details ambient storage, elevated temperature and humidity, and temperature cycling tests to be performed to as well as inspection

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processes for categorizing tin whisker density. This standard does not provide acceptance criteria. [1]

JESD201A – *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes* describes a methodology for environmental acceptance testing of tin-based surface finishes and mitigation practices for tin whiskers. The standard identifies classes of electronic devices and components based on criticality of their function and associated maximum allowable whisker length following JESD22-A121A testing. [3]

JP002 – *Current Tin Whiskers Theory and Mitigation Practices Guidelines* provides explanation of the theory behind tin whisker formation as of the publication date (03/2006) in addition to mitigation strategies to prevent tin whisker growth and efficacy analyses. [10]

GEIA-STD-0005-2 - *Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High-Performance Electronic Systems* details control levels for tin avoidance and whisker mitigation and risk acceptance for each control level. These control levels are largely similar to those in JESD201. [11]

It is important to note that the testing proscribed in each of these standards is based on environmental conditions; specifically, elevated temperature and humidity and temperature cycling processes. While these conditions are often used for accelerated aging testing of various commercial products, there currently exists no correlation or quantifiable coefficient to directly relate these tests to operating conditions. Specifically, JESD201A elaborates that neither tin whisker growth nor length can be predicted because neither the mechanisms, nor acceleration factors, are as of yet understood. [12] While these standards may be used to gain a gross understanding of the potential for electronic devices or components to form tin whiskers, the current understanding of whisker formation limits the ability of any test series or standard to quantitatively determine the potential for, or severity of, whisker formation outside of analysis of in-service samples.

DESIGN CONSIDERATIONS FOR TIN WHISKER MITIGATION

Because the mechanisms that promote tin whisker growth are largely undefined and poorly understood, the tools available to mitigate both the formation and impact of tin whiskers cover a broad range of design considerations and applications. It is important to understand that due to the enigmatic nature of tin whisker formation, there is no known singular remedy or inhibitor to whisker growth. For this reason, an understanding of the costs and benefits of each design aspect is critical, and trade-offs between cost and benefit may be highly dependent on specific design objectives and requirements. Furthermore, while some design considerations may be taken to inhibit tin whisker growth, there are also design practices that may be undertaken to mitigate the potentially detrimental impact of tin whiskers should they form. Even without a comprehensive understanding of the factors governing tin whisker formation strategies can implemented to handle potential system faults that may occur.

Design Considerations to Reduce Potential for Tin Whisker Growth

Tin whisker growth is correlated with a variety of factors that may occur in the design, fabrication and function of electronic components, MEMS, and optical devices. While no single consideration is assured to prevent tin whisker growth, implementation of one or more consideration may significantly reduce the potential for tin whisker formation. Some of the most readily implemented mitigating design considerations to prevent tin whisker growth are [13]:

- Use of lead/tin solder chemistries, avoid use of pure tin
- Avoidance of electroplated or “bright” tin finishes
- Increase grain size through addition of alloying elements
- Increase grain size through fabrication and manufacturing processes
- Inclusion of vibration isolation elements on circuit board mounting structures
- Separation of circuit board traces and connectors with high voltage differential
- Application of conformal coatings to board surfaces
- Reduction or relief of residual stresses
- Minimize introduction of stress through processing, assembly, and operation
- Maintain process and fabrication control to prevent surface damage or marks, and resulting stress concentration or loss of protective coating (Figure 4)

Whiskers have been observed to form under, and eventually penetrate protective coatings, allowing them to directly interact with other—supposedly isolated—components; [13] however it should be noted that conformal coatings offer two layers of protection between conductors, requiring two points of failure before a whisker can create such a failure. Even in cases where whisker formation does not result in direct electrical contacts, compromise of protective coatings may result in a path for further environmental damage to the underlying electronic components.

Design Considerations to Reduce Impact of Tin Whiskers

While efforts may be undertaken to reduce the potential for tin whisker growth, none of these are assured to fully prevent whisker formation. Further design considerations may be implemented to reduce the impact of tin whiskers should they form. As with whisker formation considerations, these may be used in combination as part of an overall design strategy. Commonly implemented design practices for mitigation of the impact of tin whisker formation include:

- Separation of board traces to reduce the potential of whiskers of sufficient length to bridge the gap
- Implementation of physical barriers to prevent shorts
- Application of conformal coatings, potting materials, or other means of encapsulation
- Shielding or segregation of MEMS and optical devices from electronic elements

Design Considerations for Functional Safety

Numerous efforts can be made to reduce tin whisker growth and to reduce the impact of tin whiskers if they grow; however, ultimately there must be fault handling and mitigation strategies designed into electrical and electronic systems.

Functional safety design concepts outline a method by which hazards and risk are first identified and then the tolerability of those identified risks is evaluated such that the necessary level of risk reduction can be determined. This is a process that is applied across components and systems. A set of safety requirements is defined for each risk reduction target and a safety integrity level (SIL) is assigned to each safety requirement. In every step of the safety life cycle, rigorous documentation is performed in order to catalog the process. Ultimately, a design then incorporates safety functions, which are the means by which the system meets its safety requirements, and extensive validation is performed on the implementation of these functions.

CONCLUSIONS

The propagation of electronic sub-systems and components in automotive systems represents an unprecedented intersection between safety-critical

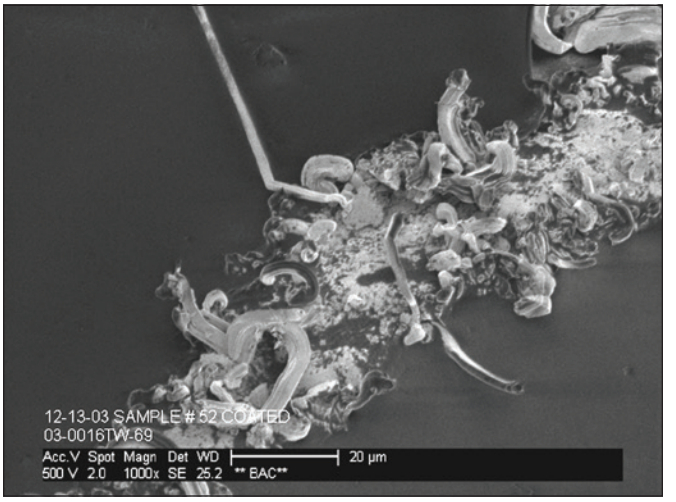

Figure 4: Whiskers forming through scribe mark in coating [13]

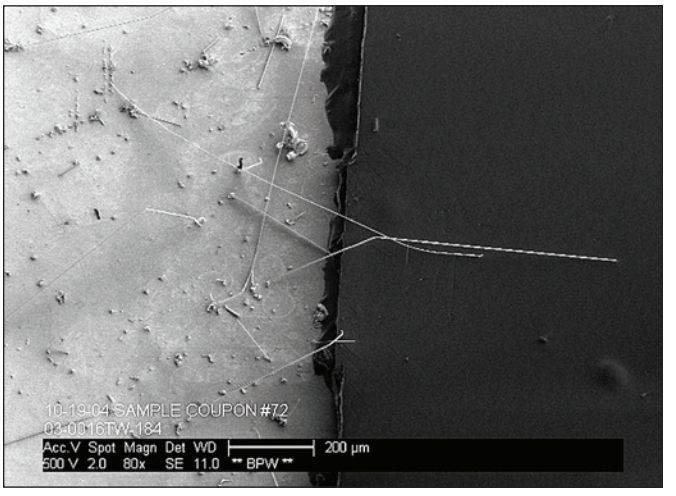

Figure 5: Tin whisker formation between coated and uncoated surfaces [13]

devices and consumer electronics. Never before have electronic devices played such a critical role in systems so ubiquitous. However, related standards - such as those surrounding a subject such as tin whiskers - have failed to fully appreciate the class into which these devices should fall and the associated repercussions of such classification.

Tin whiskers represent a threat to electronic systems that, at current, has poorly understood root causes. To date, no singular mechanism has been definitively proven to directly lead to whisker formation. While the presence of internal or external stresses has been attributed to whisker formation, the vast range of factors that can result in component stresses makes it nearly impossible to eliminate all such sources. While limited and only relatively recently developed, standards exist in industry to assess the potential for tin whisker formation, these standards are, at best, poorly correlated with real-world conditions and do not serve as reliable predictors of whisker formation in nominal operational conditions, as opposed to prescribed test conditions.

Due to the challenges in predicting or quantifying the potential for whisker growth, it becomes necessary to implement a holistic approach to prevention of whisker formation as well as mitigation of the impact that tin whisker formation may have on a system. A comprehensive approach will include design decisions to reduce the potential for, and rate of, whisker formation; mechanisms to mitigate the immediate effects of whisker formation; and system-wide design features to limit the potential damage caused by whiskers.

Implementation of these design considerations may exceed or diverge from existing standards, which at present may not be particularly relevant to assessing or predicting the risk of tin whiskers to a given system design. The design of complex and safety-critical systems should take particular note of the possible contributors to, and effects of, whisker formation and include provisions to protect against this danger.

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PRODUCT Showcase

EYE DIAGRAM
PART 1: FUNDAMENTAL CONCEPTS

By Bogdan Adamczyk, Krzysztof Russa, and Nicholas Hare

This is the first of two articles devoted to an eye diagram. In this article, the fundamental definitions and concepts are presented. The next article will show the impact of driver, receiver, and interconnect properties on signal quality using data eye and data eye mask concepts while evaluating several different HDMI cables.

INTRODUCTION

Consider a digital signal as it travels from a transmitter to a receiver. The quality of the signal arriving at the receiver can be affected by many factors, including the transmitter, cables or PCB traces, and connectors. The signal quality is also referred to as signal integrity. An eye diagram is a graphical tool used to quickly evaluate the quality of a digital signal. The name eye diagram has been coined because it has the appearance of a human eye [1,2]. Eye diagrams are commonly used for testing at both receivers and transmitters.

An eye diagram is basically an infinite persisted overlay of all bits captured by an oscilloscope to show when bits are valid. This provides a composite picture of the overall quality of a system's physical layer characteristics.
This picture covers all possible combinations of variations affecting the signal: amplitude, timing uncertainties, and infrequent signal anomalies.

The eye diagram is created by superimposing successive bit sequences of the data. Consider all possible 3-bit sequences shown in Figures 1a through 1h.

It should be noted that the data sequences in Figure 1

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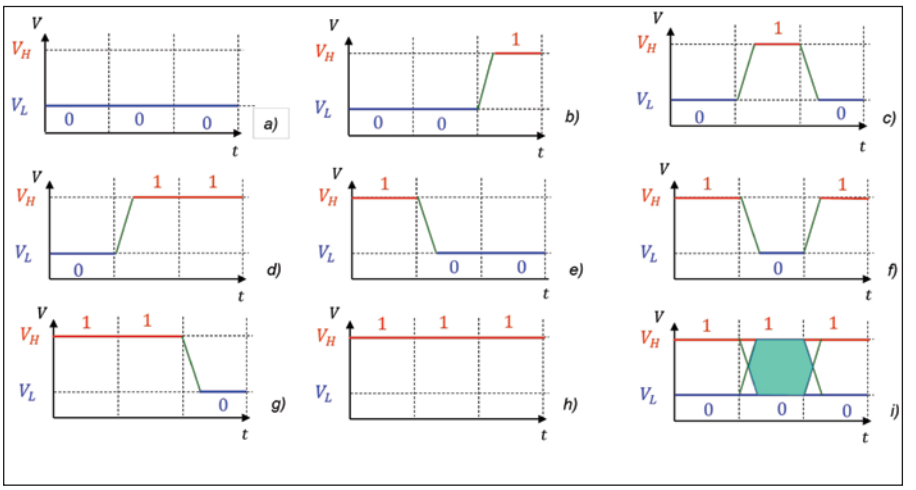

Figure 1: 3-bit sequences (a-h), and eye diagram (f)

and Figure 2a are shown as straight lines; the actual data stream looks like the one shown in Figure 2b.

EYE DIAGRAM PARAMETERS

Ideally, the eye diagram would consist of two parallel horizontal lines and two parallel vertical lines (assuming instantaneous rise and fall times), as shown in Figure 3a. Assuming a more realistic case with finite rise and fall times, the less "ideal" eye diagram would look like the one shown in Figure 3b.

An even more realistic signal would exhibit some degree of amplitude and rise/fall time variation. These amplitude and time variations give rise to several parameters associated with an eye diagram, as shown in Figure 4 on page 50.

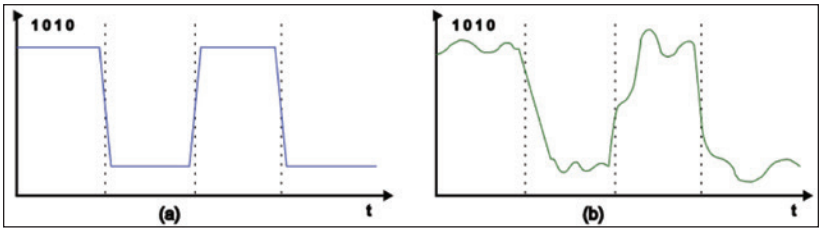

Figure 2: (a) Ideal bit sequences, (b) actual bit sequences

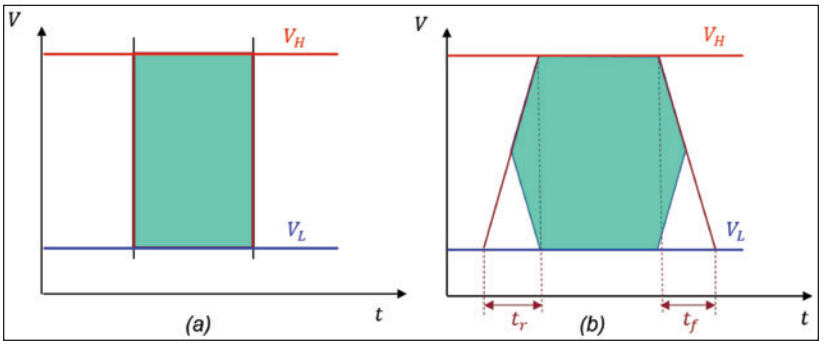

Figure 3: "Ideal" eye diagram – (a) instantaneous rise and fall times, (b) finite rise and fall times

Note that the eye area has been reduced. The eye crossing in Figure 4 is often referred to as a zero crossing since the data used for an eye diagram creation is usually transmitted as a differential pair signal.

The eye diagram shown in Figure 4 is still an "ideal" diagram, as it consists of perfectly straight lines. An actual (real data) eye diagram looks more like the one shown in Figure 5 on page 50.

DATA AND CLOCK DEPENDENCIES

To achieve high reliability of data transfer, a synchronization signal is introduced. This signal is used to trigger data transfer operation. The data transfer occurs when the synchronization signal transitions its state (e.g., the rising edge of a clock signal), at which time the data signal state will be read as either low or high. The high state will be read when the data signal is above a certain voltage threshold level ($V_{IH\,\min}$), and it will be read as low when it is below another voltage threshold ($V_{IL\,\max}$). This synchronization signal is typically referred to as a clock or strobe.

However, data signal voltage levels being below or above a predefined voltage threshold at the time of data transfer is an insufficient condition for reliable data transfer. It is also necessary to meet certain timing dependencies between data and synchronization signals.

To explain those dependencies, let's look at a specific case described in Figure 6 [3]. The synchronization signal, in this case, is the clock and the data is transferred (read) at the rising edge of the clock. We will assume that the clock and data signals are transitioning very quickly.

To guarantee that the proper data will be read, a valid data signal must be present for a certain time duration prior to the clock signal transition. This duration is referred to as a setup time (t_{SETUP}). Additionally, it is also required that the data signal remains valid for a certain time duration after the transition of the clock signal. This duration is referred to as a hold time (t_{HOLD}). Setup and hold times are properties of devices receiving the data and are often referred to as their timing requirements. If the timing requirements are not met, incorrect data can be read by the receiver.

Using midpoint signal levels, the assumption of very fast signal transitions allows us to measure timing dependencies between the data and clock (setup and hold time). In other words, this assumption means we can neglect signal rise/fall time duration if those durations are much shorter than the duration when the data bit is valid. Suppose the clock period gets shorter, and we can no longer neglect signal rise/fall time duration. In that case, the evaluation of timing dependencies between the data and clock (setup and hold time) must account for slow signal transition. Figure 7 illustrates such a case.

The rising edge of the data is still very fast, but the clock transition is much slower. The duration of time between the clock transition from low and high level is now substantial compared to the duration of the data bit. During this long clock transition time the clock state can be either high or low, so we no longer can measure setup and hold time using midpoint levels. This case would require setup and hold time to be measured when the signals are crossing the low or high voltage threshold levels ($V_{IL\,max}$, $V_{IH\,min}$).

Evaluation and visualization of valid signal timing using the setup and hold time shown in Figure 6 is relatively easy, even with the clock and data jitter.

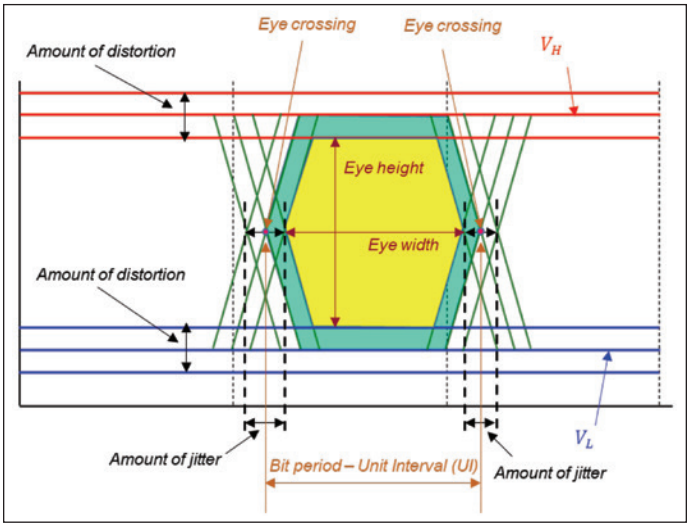

Figure 4: Eye diagram parameters

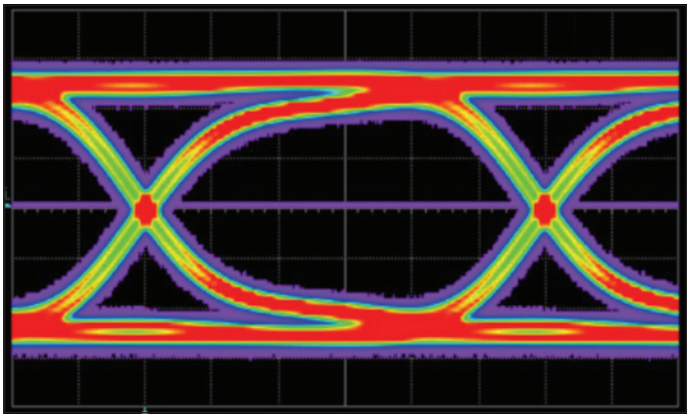

Figure 5: Actual eye diagram

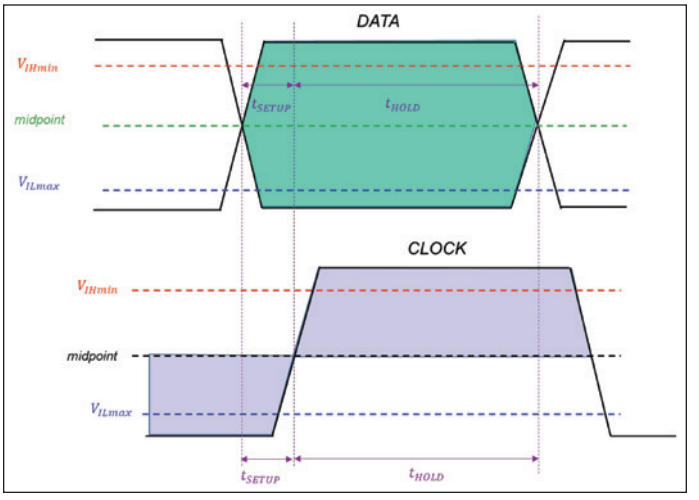

Figure 6: Data and clock synchronization for signals with fast transition times

It is, however, quite difficult for the case shown in Figure 7 when taking jitter into account. That's where the eye diagram can help.

DATA EYE MASK

The concept of a data eye diagram can be used to evaluate the quality of the data signal and whether the signal meets timing requirements. To accomplish this, receiver timing requirements are used to define the horizontal dimension of a region. Voltage level thresholds ($V_{IL\,max}$, $V_{IH\,min}$) are used to define the vertical boundaries of that region. The resulting region is referred to as the data eye mask. A sample of a data eye mask, representing requirements for a video HDMI standards receiver, is shown in Figure 8.

The data eye mask represents the "keep-out" region. Signals at the receiver must not cross the data eye mask region, or a violation of receiver timing requirements occurs. The mask is defined based on receiver properties and can have various shapes (rectangular, triangular, etc.). The data eye mask can be many different shapes, as shown in Figure 9.

FUTURE WORK

The next article will show the impact of driver, receiver, and interconnect properties on signal quality using data eye and data eye mask concepts.

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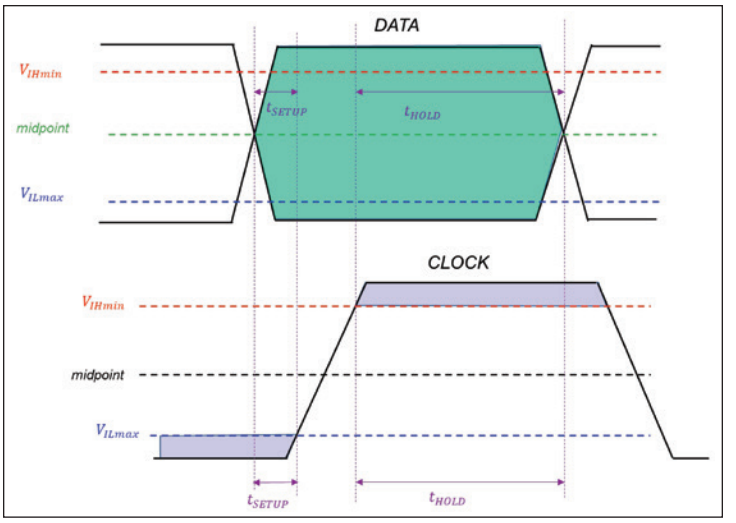

Figure 7: Data and clock synchronization for signals with slow transition times

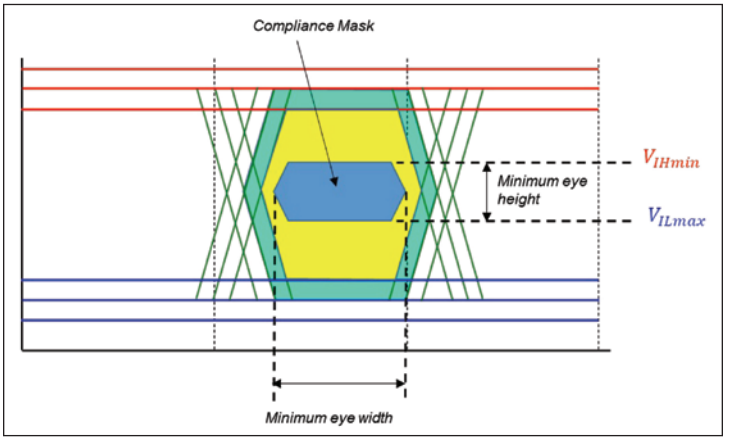

Figure 8: HDMI data eye mask

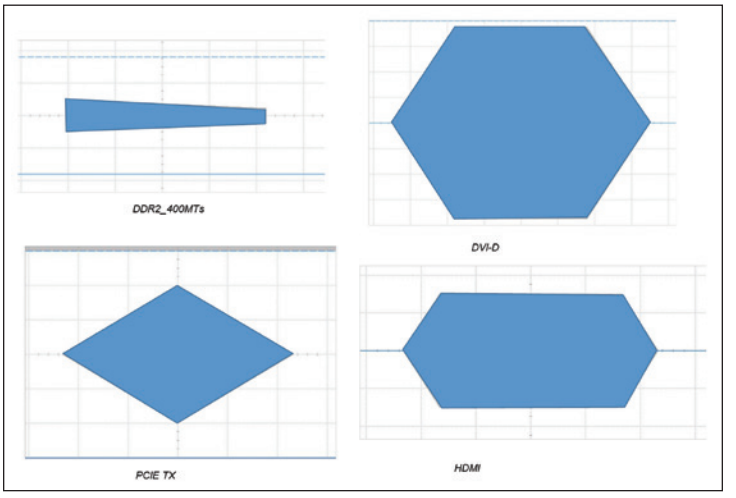

Figure 9: Examples of data eye masks

CHALLENGES OF DESIGNING SYSTEM-LEVEL ESD PROTECTION AT THE IC-LEVEL:

MISCONCEPTIONS REGARDING CURRENT FLOW TO THE IC

By Hans Kunz for EOS/ESD Association, Inc.

There is often confusion about the interaction between IC-level component ESD protection and the appropriately required system-level ESD protection strategy. System-level ESD requirements (like IEC 61000-4-2 [1] and ISO 10605 [2]) are intended for electronic systems, not for individual integrated circuits (ICs). However, it is becoming increasingly common to see supplier claims and customer expectations of system-level ESD performance at the IC-level. While such performance may be desirous to both suppliers and customers, there is significant ambiguity about what such claims and expectations mean. Generally, little information is available about the actual system surrounding the IC. How does the customer interpret an IC-level performance claim without a specific system, and how does a supplier design for and guarantee performance? Certainly, the IC has been tested in some systems to facilitate the datasheet specification, but how did the designer define that system, and how does it compare to the final customer system? This lack of specificity implies that a general capability of the IC applies to a wide range of unique system requirements when, in fact, there are significant challenges to integrating an IC into a single unique system. These challenges extend beyond safely conducting the current during the ESD event—systems are often powered, and the failure criteria can include functional operation during and after the ESD event. But gaps exist that must be considered even if the problem is reduced to a simple guarantee that current can be safely conducted during the ESD event.

Even when only considering safe ESD current conduction, two common misconceptions must be addressed. The first is that if an IC is designed to carry the entirety of the system-level ESD current, it will be able to carry that current when placed in any system. This misconception fails to consider the impact of the full system on the current waveform and to account for modulations to the waveform that make it more severe to the IC. The second is that if an IC has higher intrinsic ESD robustness (even without carrying the full system-level ESD current), then it will be easier to protect than a competing product with lower robustness. This misconception fails to account for how current is shared between system-level and IC-level protection devices. This article will focus primarily on these two misconceptions. A future article will take a more detailed look at the gaps that arise when considering the powered-up testing and the functional failure criteria, and the steps needed to address those gaps.

On the surface, it may seem unlikely, or even impossible, that other components in the system could modulate the current waveform in such a manner that it becomes more severe to the IC. Yet, these issues do occur, creating significant challenges for both the IC designer and the system designer. Two examples of how this can happen are provided—these are by no means comprehensive of all the types of issues that can occur, but rather serve to demonstrate the complexity of the interaction between components in the system and underscore the importance of those interactions in determining the final system-level performance.

Hans Kunz is a distinguished member of the technical staff at Texas Instruments, with 25+ years of experience in the development and application of on-chip ESD protection for analog designs. He is a frequent contributor to ESDA activities, including technical program committees, tutorials, workshops, and presentations for the IEW and the EOS/ESD Symposium.

The first example is a case where a parallel capacitor is placed on the board trace of the pin being stressed. This capacitor will be charged by the ESD event, shunting some of the current away from the IC. But as this capacitor charges, its voltage increases—if the voltage exceeds the trigger voltage of the IC's ESD cell—and that ESD cell has a clamping characteristic that is lower than the trigger voltage (i.e., a snapback device)—then the charge deposited on the capacitor can be discharged into the IC. This second discharge event has very little series impedance and can produce much higher peak currents than expected from the ESD discharge itself [3]. This type of event is highly dependent on the system. If the capacitance is small enough to limit the charge, or large enough to limit the voltage, or if the impedance between the capacitor and the IC is large enough to limit the current, then no failure will occur; if, on the other hand, the conditions are right, the IC will fail. If the IC designer has not considered this scenario and properly designed the ESD cell to account for it, significant variations in system-level results can occur, with seemingly insignificant changes to the overall system.

A second example arises when the IC is placed behind a series common mode choke (CMC). In this case, the ESD event must pass through the CMC to reach the IC, and the series impedance of the CMC could reasonably be assumed to improve the ESD performance of the system. But, as shown in [4], cases of lower-than-expected performance have occurred. Unlike the capacitor example, which produced a higher-than-expected peak current, the CMC distorts the shape and the timing of the ESD event. As described in [5], the CMC can allow current to flow initially, block current for a duration of time, and then allow current to flow again once the CMC coil reaches magnetic saturation. This can result in the creation of two distinct current pulses, separated by a very short period of time, relative to the expected duration of the full pulse; this current waveform is significantly different from the reference waveform in the testing standard. If the ESD cell cannot re-engage adequately within a very short time after turning off, unexpected failures can occur in an otherwise robust ESD solution.

The above examples are by no means a comprehensive list of all the ways the current waveform could be modulated into a shape/severity not anticipated or tested by the IC designer, but rather serve to highlight the reality that such modulations do occur and that they can create nuanced failures in what are thought to be robust ESD designs.

The second misconception that must be addressed is the idea that an IC that has higher ESD robustness is guaranteed to perform better in any system-level solution. In this situation, a board-level ESD protection element is expected to conduct a majority of the system-level current, with the IC expected to share the remaining (or residual) current. In this scenario, the HBM requirement on a sub-set of the IC pins is increased, with an expectation that the IC will be able to conduct more residual current and, therefore, will outperform a competitive product with a lower rating.

When two legs of a circuit are expected to share current in a controlled way, there are important electrical characteristics of the two legs that must be known—and the maximum amount of current that can be allowed in one of the legs is an insufficient

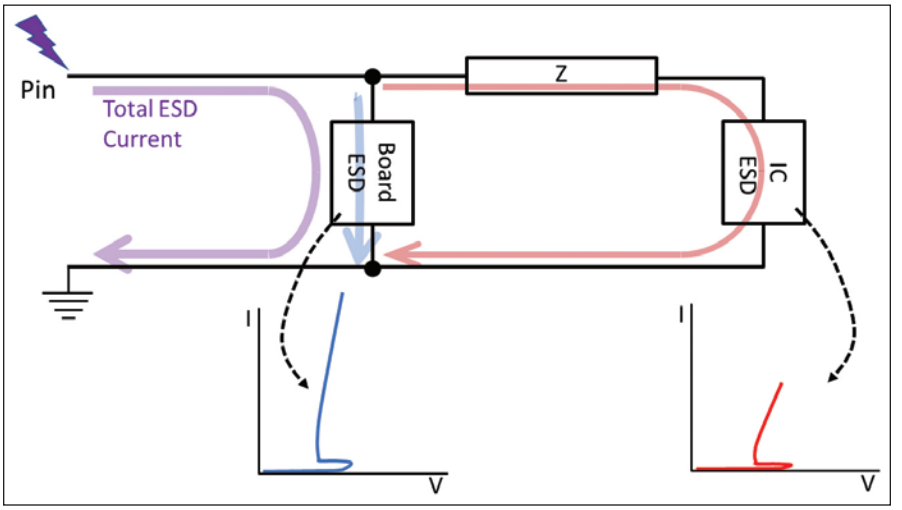

Figure 1: Board-level and IC-level ESD Protection sharing system-level ESD current. Impedance Z serves to limit current into the IC.

amount of information to properly assess the circuit. Consider Figure 1; a board-level ESD Protection is placed between a Pin and Ground; a series impedance, Z, is placed in series with the IC, with its ESD protection tied to the same ground. These ESD protection elements switch from high-impedance to low-impedance at specific bias points. How current is shared between the board and the IC ESD protection will depend on many factors, which cannot be solely deduced from the ESD robustness of the IC. Consider the case where the board-level ESD Protection triggers and clamps the voltage below where the IC protection triggers; little to no current will flow into the IC, and its robustness is inconsequential. Or consider the case where the IC protection triggers and doesn't allow the board-level protection to trigger, resulting in the IC protection conducting the entire event—its robustness is now very consequential but, as already established, insufficient to conduct the full ESD event.

Other parameters, such as the relative on-resistances of the two paths, can steer current such that the current sharing is non-optimal. The System-Efficient ESD Design (SEED) method described in [6, 7] illustrates the type of information that is required to properly design a system to share current between a board-level ESD protection element and an IC. The reader is encouraged to review this methodology for a deeper understanding of how to optimize the integration between the system and the IC. What should be clear, however, is that the robustness of the IC, without the context of the full system circuit and its parameters, is insufficient to gauge system-level ESD performance. It is quite possible to improve the robustness of the IC in a way that lowers the system-level robustness for a particular integration. The misconception that improving the IC robustness automatically leads to better system-level performance has serious consequences—increasing IC cost without guaranteeing improved performance.

This article has only dealt with misconceptions about the severity and shape of current pulses that reach the IC when integrated into a system. These misconceptions arise from a lack of recognition of how other elements in the system modulate the current waveforms delivered to the IC and how other elements in the system share current with the IC. While the ability to conduct the ESD current (whether directly or in conjunction with other elements in the system) is a critical requirement for the IC designer, it is often only the first of many requirements. If the system is powered during the ESD stress, there are added requirements for the IC designer. If that powered system is required to perform functional tasks during or after the ESD stress application, even more requirements are introduced. Future articles will explore some of these requirements in more detail and highlight some of the critical design techniques commonly used to address them.

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CABLE ANTENNAS AND FERRITE CORES

By Dr. Min Zhang

Design engineers who have been to an EMC testing laboratory must be familiar with the large selection of ferrite cores that a test lab often provides. For a product with a mains lead or a system consisting of long cables (HDMI, USB, etc.), the most common EMC failures often include conducted emissions in the frequency range of 9 kHz and 30 MHz and radiated emissions in the 30-300 MHz range. In such cases, cables often become effective antennas, and ferrite cores are generally used to locate and suppress the noise (at least during the troubleshooting stage).

The practice of using ferrite cores on cables is often performed using a trial-and-error approach. Engineers place a ferrite core on one end of a cable and measure the performance. If the noise at the frequency range of interest is reduced with the placement of the ferrite core, this means the approach works. If not, the ferrite core is then removed and placed in another cable.

In this column, I offer a brief summary of a more systematic approach for using ferrite cores on cables. Hopefully, this summary can serve as a "ferrite core checklist" for design and test engineers.

To start with, we need to understand some basics of a cable antenna. For example, a 1-meter-long cable could, depending on its connections, serve as either a half wavelength or a quarter wavelength antenna. If both ends of the cable are fastened to the equipment chassis, chances are that the characteristic impedances at both ends are low, so the cable is a half wavelength antenna. Since 1 meter is a half wavelength for 150MHz signals, this cable will radiate quite efficiently for noise around 150MHz.

However, suppose one end of the cable is fastened to the equipment chassis while the other end is in free space (at a high impedance). In that case, the cable becomes a quarter wavelength antenna (you can treat the equipment chassis as the other half of the antenna). Common mode current at around 75MHz range starts to flow from the low impendence end of the cable to the high impedance end, which translates to radiation at 75MHz.

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Therefore, for a quarter wavelength cable, adding a ferrite (which effectively increases the characteristic impedance) only works if it is placed at the lower impedance end of the cable (often the equipment chassis end). Increasing the impedance at the lower impedance end breaks the boundary condition of a quarter wavelength antenna, which results in less common mode current at the frequency of interest. If ferrite cores are located at the higher impedance end rather than the lower impedance end of a cable, chances are that the ferrite cores will prove ineffective, or in some cases, make the emissions worse. (See my YouTube video at https://youtu.be/HMvpml48v4g that demonstrates the point.)

My first advice for using ferrites is to treat them as a resistive (lossy) rather than as an inductive component. Therefore, when selecting the ferrite grade, it is often more important to aim for maximum resistive loss.

Another part that engineers often overlook is that the impedance provided by a single-turn configuration ferrite core is simply not large enough. When we placed a ferrite core on a cable and saw no impact, we could easily conclude that this approach was ineffective. Checking the datasheet from ferrite manufacturers, one can see that a 1-turn configuration has only 25% of the impedance compared with a 2-turn configuration at its effective frequency range. (Note that, as frequency increases, the impedance of a multi-turn configuration ferrite drops rapidly due to the parasitic capacitance introduced by the turn-to-turn windings. Hence the multi-turn advantage is progressively lost above a certain frequency.)

This suggests that sometimes a single-turn ferrite core solution is not effective enough, and a multi-turn configuration should be tried in such cases. In cases of large diameter cables where bending radius limits a multi-turn ferrite option, we suggest using a few ferrite cores in series to increase its impedance.

Another benefit of placing a ferrite core near the equipment chassis is that it forms an R-L-C filter with the chassis/ground plane within the equipment. Because ferrite material is essentially a ceramic, it has both high permittivity and permeability. Therefore, placing a ferrite near a conductive surface will increase its capacitance. Placing a ferrite core near the equipment chassis will improve the filtering performance compared with using the ferrite in free space.

A short column like this cannot cover every aspect of using ferrites on cables. Secondary effects such as saturation, leakage resistance, etc., are also important. Hopefully, the following checklist can provide effective guidance for engineers who wish to use ferrites as a valuable aid to electromagnetic compatibility.

1. For ferrite cores used as common mode suppressors, saturation is generally not possible. However, if you must place a core around a single conductor, be sure that the current does not exceed the saturation current.
2. Always check the manufacturer's datasheet and select ferrite materials for maximum resistive loss (that is, not for inductance).
3. For a single-turn configuration, long sleeve ferrites are preferred as the impedance is proportional to the length of a ferrite core. The best performance is often achieved if the ferrite fits the cable snugly.
4. For a multi-turn configuration, a fat toroid shape is preferred. Keeping the wires wide apart helps improve the performance at high-frequency range (for the reasons we explained before).
5. Place the ferrite at the lower characteristic impedance end of a cable, e.g., equipment chassis.
6. If possible, place the ferrite on a conductive surface (such as the ground plane of a system).
7. If possible, always try maximum impedance (i.e., multi-turn configuration) first.
8. In rare cases where placing a ferrite could increase emissions of signals at a certain frequency, do not remove the ferrite cores. Instead, place another ferrite at the other end of the cable.

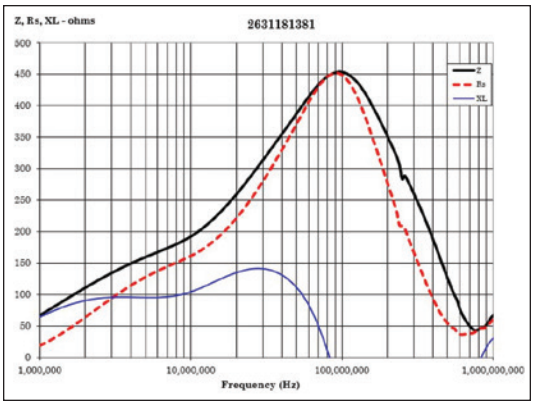

Figure 1a: Choose ferrite grade for maximum resistive loss rather than inductance

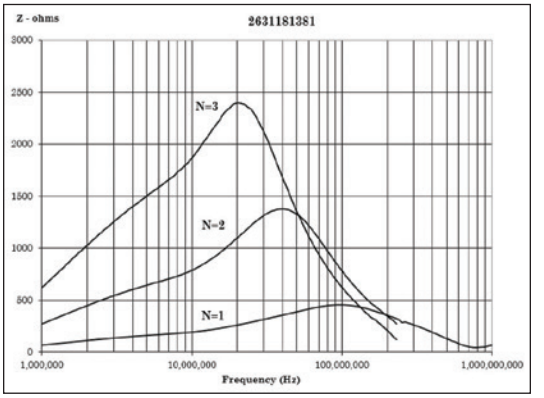

Figure 1b: Multi-turn configuration gives maximum impedance at the frequency range of interest, but this advantage is progressively lost with frequency

Figure 1c: Placing ferrite cores next to equipment chassis effectively forms an R-L-C filter

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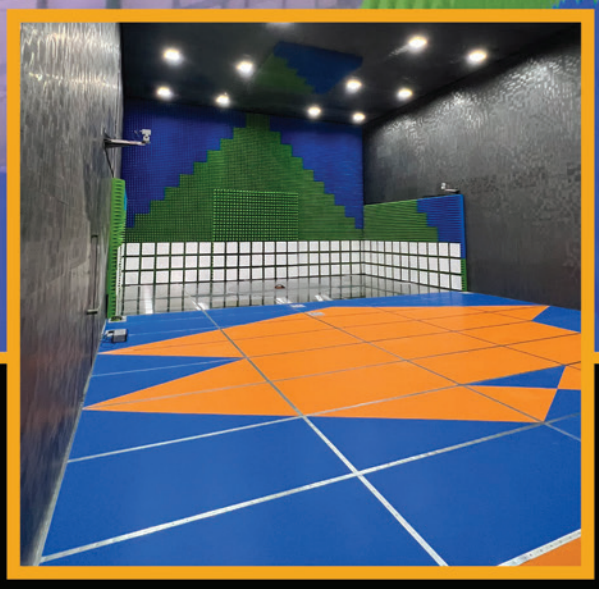

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